AWARD / CONTRACT

1. THIS CONTRACT IS A RATED ORDER UNDER DPAS (15CFR 350)	U ▶	DOA7	PAGE OF PAGES 1
2. CONTRACT (Proc. Inst. Ident.) NO. DABT63-94-C-0017	3. EFFECTIVE DATE	4. REQUISITION/PURCHASE REQUEST/PROJECT NO. RJ1500-4006-0552	

5. ISSUED BY CODE DKO-I

DIRECTORATE OF CONTRACTING
ATTN: ATZS-DKO-I
POST OFFICE BOX 748
FORT HUACHUCA AZ 85613-0748

GLORIA A. BICKLER C12
(602)533-1338

6. ADMINISTERED BY (If other than Item 5) CODE EMPTY

7. NAME AND ADDRESS OF CONTRACTOR (No., street, city, county, State and ZIP Code) Vendor ID: 00017737

BOLT, BERANEK & NEWMAN, INC
ATTN: MS DIBLASIO
10 MOULTON STREET
CAMBRIDGE MA 02138-

CEC:

8. DELIVERY
☐ FOB ORIGIN ☒ OTHER (See below)

9. DISCOUNT FOR PROMPT PAYMENT
00.000% 00 Net 000

10. SUBMIT INVOICES (4 copies unless otherwise specified) TO THE ADDRESS SHOWN IN: ▶ ITEM See Section Para G.2

CODE 26970 FACILITY CODE

11. SHIP TO/MARK FOR CODE DARPA

ADVANCED RESEARCH PROJECTS AGENCY
3701 NORTH FAIRFAX DRIVE
ARLINGTON VIRGINIA 22203-1714

12. PAYMENT WILL BE MADE BY CODE S02086

DEFENSE FINANCE & ACCOUNT SVC
DEFENSE ACCOUNTING OFFICE
DRAWER P
FORT HUACHUCA AZ 85613-6000

13. AUTHORITY FOR USING OTHER THAN FULL AND OPEN COMPETITION:
☐ 10 U.S.C. 2304(c)( ) ☐ 41 U.S.C. 253(c)( )

14. ACCOUNTING AND APPROPRIATION DATA
See Section G. Paragraph G.6

15A. ITEM NO.	15B. SUPPLIES/SERVICES	15C. QUANTITY	15D. UNIT	15E. UNIT PRICE	15F. AMOUNT
	See attached Schedule(s)				

COST PLUS FIXED FEE — 15G. TOTAL AMOUNT OF CONTRACT ▶ $ 685,081.

16. TABLE OF CONTENTS

(X)	SEC.	DESCRIPTION	PAGE (S)	(X)	SEC.	DESCRIPTION	PAGE (S)
		PART I - THE SCHEDULE				PART II - CONTRACT CLAUSES	
X	A	SOLICITATION/CONTRACT FORM	1	X	I	CONTRACT CLAUSES	8
X	B	SUPPLIES OR SERVICES AND PRICES/COSTS	1			PART III - LIST OF DOCUMENTS, EXHIBITS AND OTHER ATTACH.	
X	C	DESCRIPTION/SPECS./WORK STATEMENT	1	X	J	LIST OF ATTACHMENTS	1
X	D	PACKAGING AND MARKING	1			PART IV - REPRESENTATIONS AND INSTRUCTIONS	
X	E	INSPECTION AND ACCEPTANCE	1		K	REPRESENTATIONS, CERTIFICATIONS AND OTHER STATEMENTS OF OFFERORS	
X	F	DELIVERIES OR PERFORMANCE	1				
X	G	CONTRACT ADMINISTRATION DATA	4		L	INSTRS., CONDS., AND NOTICES TO OFFERORS	
X	H	SPECIAL CONTRACT REQUIREMENTS	2		M	EVALUATION FACTORS FOR AWARD	

CONTRACTING OFFICER WILL COMPLETE ITEM 17 OR 18 AS APPLICABLE

17. ☒ CONTRACTOR'S NEGOTIATED AGREEMENT (Contractor is required to sign this document and return 1 copies to issuing office.) Contractor agrees to furnish and deliver all items or perform all the services set forth or otherwise identified above and on any continuation sheets for the consideration stated herein. The rights and obligations of the parties to this contract shall be subject to and governed by the following documents: (a) this award / contract, (b) the solicitation, if any, and (c) such provisions, representations, certifications, and specifications, as are attached or incorporated by reference herein. (Attachments are listed herein.)

18. ☐ AWARD (Contractor is not required to sign this document.) Your offer on Solicitation Number _____ including the additions or changes made by you which additions or changes are set forth in full above, is hereby accepted as to the items listed above and on any continuation sheets. This award consummates the contract which consists of the following documents: (a) the Government's solicitation and your offer, and (b) this award / contract. No further contractual document is necessary.

19A. NAME AND TITLE OF SIGNER (Type or print)
Mark J. Sherman, Sr. Contracts Mgr.

20A. NAME OF CONTRACTING OFFICER
PATRICIA WOZNICK C10 (602)533-1398

19B. NAME OF CONTRACTOR — Mark J. Sherman (Signature of person authorized to sign)

19C. DATE SIGNED 4/5/94

20B. UNITED STATES OF AMERICA BY Patricia Wozniak (Signature of Contracting Officer)

20C. DATE SIGNED 5 Apr 94

NSN 7540-01-152-8069 PREVIOUS EDITION UNUSABLE

25-108

STANDARD FORM 26 (REV 4-85) Prescribed by GSA - FAR (48 CFR) 53.214

310 295 TOTAL P.02

SECTION B

SUPPLIES OR SERVICES AND PRICES/COSTS

ITEM	DESCRIPTION	QUANTITY	U/M	U/P	AMOUNT
0001	The contractor shall provide research entitled "BodyLAN: A Wireless, Body Local Area Network" COST: $634,557 FEE: 50,524 CPFF: 685,081	1	JB	685081.000000	685081.00
0002	Data in accordance with DD Form 1423, Contract Data Requirments List, and DD Form 1556, Data Item Description, identified as Exhibit A CDRL A001: NSP CDRL A002: NSP	1	LT	0.000000	0.00

END OF SECTION B

SECTION G
CONTRACT ADMINISTRATION DATA

G.1 CONTRACT CLAUSE AND SOLICITATION PROVISION NUMBERING FORMAT
(Fort Huachuca Local Clause 52.000-4001)

The following applies to numbering in all sections of this solicitation/contract.

This document is computer generated by the Standard Army Automated Contracting System (SAACONS). The numbering system used by the computer for contract clauses and solications provisions differs slightly from the procurement regulations. It is similar and easily recognizable. The Federal Acquisition Regulation (FAR) numbering format for contract clauses and solicitation provisions is 52.2XX-X, with the specific FAR provision or clause number being a sequence number assigned within each section or subpart 52.2. SAACONS always uses a 9 digit number (e.g. 52.2XX-XXXX).

FAR contract clauses and solicitation provisions are recognized by a "0" in the 6th digit of the SAACONS number. Department of Defense Federal Acquisition Regulation Supplement (DFARS) contract clauses and solicitation provisions are recognized by a "7" in the 6th digit of the SAACONS number. Army Federal Acquisition regulation supplement (AFARS) contract clauses and solicitation provisions are recognized by a "9" in the 6th digit of the SAACONS number. Local clauses created for use ONLY in Fort Huachuca Solicitations/Contracts are designated by a "4" in the sixth position.

Examples of the difference in the numbering are provided below:

	STANDARD NUMBERING SYSTEM:	SAACONS:
FAR	52.227-1	52.227-0001
DFARS	52.243-7000	52.243-7000
AFARS	52.237-9030	52.237-9030
LOCAL	52.200-4001	52.200-4001

(End of clause)

G.2 SUBMITTAL OF REQUESTS FOR CONTRACT FINANCING PAYMENTS
(Fort Huachuca Local Clause 52.200-4007 ALT XX)

a. All requests for contract financing payments shall be submitted in accordance with FAR clause 52.232-25, PROMPT PAYMENT, and will include, as aminimum, the information specified in this clause.

b. All request shall be submitted on Standard Form 1034,

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL. To avoid delay in payment, vouchers shall be submitted to the addresses and in number of copies specified below (if prepared by copying process, one copy shall be marked "original").

(1) For reimbursement of allowable costs, the contractor shall submit five copies of each request for contract financing payment to the cognizant Defense Contract Audit Agency, with one copy each to the COR and the Contracting Officer. DCAA will forward provisionally approved contract financing payment to the designated payment office.

(2) For payment of fee, the contractor shall submit the original and one copy to the Contracting Officer, with one copy to the COR. The Contracting Officer will forward the approved voucher to the desinated payment office.

(3) Designated Payment Office Address:
Finance and Accounting Officer, Drawer P, Commercial Accounts, Fort Huachuca, AZ 85613

G.3 CONTRACT ADMINISTRATION DATA
(Fort Huachuca Local 52.200-4015)

Bidder's/offeror's office which will receive payment, supervise and administer resulting contract:

BBN Systems and Technologies, A Division of Bolt Beranek and Newman, P.O. Box 4340, Boston, MA 02210 _____ _____ _____ _____
(Insert address, city and state and zip code)

Name and address of owner and operator:

_____
(Insert address, city and state and zip code)

G.4 NOTICE OF INCORPORATION OF SECTION K
(Fort Huachuca Local Clause 52.200-4016 ALT I)

The following sections of the solicitation will not be distributed with the contract; however, they are incorporated in and form a part of the resultant contract as though furnished in

full text therewith:

SECTION	TITLE
K	REPRESENTATIONS, CERTIFICATIONS AND OTHER STATEMENTS OF BIDDERS/OFFERORS/QUOTERS

G.5 GOVERNMENT CONTRACT ADMINISTRATOR
(Fort Huachuca Local Clause 52.200-4020)

Administration of this contract shall be performed by:

Directorate of Contracting
ATTN: ATZS-DKO-I
Post Office Box 748
Fort Huachuca, Arizona 85613-0748

Point of Contact: Barbara VanDoren
Telephone Number: (602) 538-0412

G.6 ACCOUNTING CLASSIFICATION
(Fort Huachuca Local 52.200-4083 ALT II)

CLIN	ACCOUNTING CLASSIFICATION	AMOUNT

0001 & 0002 - 97404001301000500505P4T10A841042594000000HJ150040060552JWC90000 2086 IN THE AMOUNT OF $483,684. CLINS 0001 & 0002; 97504001301000 500505T10A841142581000000HJ150043480535JWBL00S02086 in the amount of $ 201,397.00 It is anticipated that the funds currently allotted to the contract will cover the work to be performed through 30 October 1995.

G.7 SF-294 AND SF-295 REPORTING REQUIREMENTS
(FAR 19.704(A)(5) AND 52.219-9)(d)(10))
(Fort Huachuca Local 52-200.4347)

a. SF-294, Subcontracting Report for Individual Contracts, shall be submitted semi-annually by all except small businesses within 30 calendar days after the end of the reporting period to the following addressees:

(1) U.S. Army Intelligence Center and Fort Huachuca, ATTN: ATZS-DKO-I Post Office Box 748, Fort Huachuca, AZ 85613-0748

(2) U.S. Army Intelligence Center and Fort Huachuca,

full text therewith:

SECTION	TITLE
K	REPRESENTATIONS, CERTIFICATIONS AND OTHER STATEMENTS OF BIDDERS/OFFERORS/QUOTERS

G.5 GOVERNMENT CONTRACT ADMINISTRATOR
(Fort Huachuca Local Clause 52.200-4020)

Administration of this contract shall be performed by:

Directorate of Contracting
ATTN: ATZS-DKO-I
Post Office Box 748
Fort Huachuca, Arizona 85613-0748

Point of Contact: Gloria Bickler
Telephone Number: (602) 533-1342

G.6 ACCOUNTING CLASSIFICATION
(Fort Huachuca Local 52.200-4083 ALT II)

CLIN	ACCOUNTING CLASSIFICATION	AMOUNT

0001 & 0002 - 9740400130100050O5P4T10A841042594000000HJ150040060552JWC90000 2086 IN THE AMOUNT OF $483,684. It is anticipated that the funds currently allotted to the contract will cover the work to be performed through 31 March, 1995.

G.7 SF-294 AND SF-295 REPORTING REQUIREMENTS
(FAR 19.704(A)(5) AND 52.219-9)(d)(10))
(Fort Huachuca Local 52-200.4347)

a. SF-294, Subcontracting Report for Individual Contracts, shall be submitted semi-annually by all except small businesses within 30 calendar days after the end of the reporting period to the following addressees:

(1) U.S. Army Intelligence Center and Fort Huachuca, ATTN: ATZS-DKO-I Post Office Box 748, Fort Huachuca, AZ 85613-0748

(2) U.S. Army Intelligence Center and Fort Huachuca,

ATTN: ATZS-DKB (SADBUS), Post Office Box 748, Fort Huachuca, AZ 85613-0748

(3) U.S. Army Training and Doctrine Command, ATTN: ATCS-B (SADBU), Fort Monroe, VA 23651-5000

b. SF-295, Summary Subcontract Report, shall be submitted quarterly by all except small businesses within 30 calendar days after the end of each quarter to the following addressees:

(1) Office of the Deputy Secretary of Defense, ATTN: Director of Small and Disadvantaged Business Utilization, The Pentagon, Washington, D.C. 20301-3061.

(2) Director of Small and Disadvantaged Business Utilization, Office of the Secretary of the Army, Washington, D.C. 20310-0106

(3) U.S. Army Intelligence Center and Fort Huachuca, ATTN: ATZS-DKO-I Post Office Box 748, Fort Huachuca, AZ 85613-0748

(4) U.S. Army Intelligence Center and Fort Huachuca, ATTN: ATZS-DK-SDB (SADBUS), P. O. Box 748, Fort Huachuca, AZ 85613-0748

(5) U.S. Army Training and Doctrine Command, ATTN: ATCS-B (SADBU), Fort Monroe, VA 23651-5000

END OF SECTION G

AMENDMENT OF SOLICITATION/MODIFICATION OF CONTRACT

1. CONTRACT ID CODE	PAGE OF PAGE
U	1 | 2

2. AMENDMENT/MODIFICATION NO.	3. EFFECTIVE DATE	4. REQUISITION/PURCHASE REQ. NO.	5. PROJECT NO. (*If applicable*)
P00001	95 JAN 11	HJ1500-4348-0535	DAR4 A841/14

6. ISSUED BY	CODE	7. ADMINISTERED BY (*If other than Item 6*)	CODE
DIRECTORATE OF CONTRACTING ATTN: ATZS-DKO-I POST OFFICE BOX 748 FORT HUACHUCA, AZ 85613-0748 BARBARA C. VANDOREN (602)538-0412	DKO-I	BARBARA VANDOREN (703) 538-0412	C22

8. NAME AND ADDRESS OF CONTRACTOR (*No., street, county, State and ZIP Code*)	(✓)	9A. AMENDMENT OF SOLICITATION NO.
BOLT, BERANEK & NEWMAN, INC. ATTN: MS DIBLASIO 10 MOULTON STREET CAMBRIDGE, MA 02138		9B. DATED (*SEE ITEM 11*)
	X	10A. MODIFICATION OF CONTRACT/ORDER NO. DABT63-94-C-0017
CODE 269700 FACILITY CODE		10B. DATED (*SEE ITEM 13*) 94 APR 05

11. THIS ITEM ONLY APPLIES TO AMENDMENTS OF SOLICITATIONS

☐ The above numbered solicitation is amended as set forth in Item 14. The hour and date specified for receipt of Offers ☐ is extended, ☐ is not extended.

Offers must acknowledge receipt of this amendment prior to the hour and date specified in the solicitation or as amended, by one of the following methods:

(a) By completing Items 8 and 15, and returning _____ copies of the amendment; (b) By acknowledging receipt of this amendment on each copy of the offer submitted; or (c) By separate letter or telegram which includes a reference to the solicitation and amendment numbers. FAILURE OF YOUR ACKNOWLEDGEMENT TO BE RECEIVED AT THE PLACE DESIGNATED FOR THE RECEIPT OF OFFERS PRIOR TO THE HOUR AND DATE SPECIFIED MAY RESULT IN REJECTION OF YOUR OFFER. If by virtue of this amendment you desire to change an offer already submitted, such change may be made by telegram or letter, provided each telegram or letter makes reference to the solicitation and this amendment, and is received prior to the opening hour and date specified.

12. ACCOUNTING AND APPROPRIATION DATA (*If required*)

SEE SECTION G NET INCREASE: $201,397.00

13. THIS ITEM APPLIES ONLY TO MODIFICATIONS OF CONTRACTS/ORDERS, IT MODIFIES THE CONTRACT/ORDER NO. AS DESCRIBED IN ITEM 14.

(✓)	
	A. THIS CHANGE ORDER IS ISSUED PURSUANT TO: (*Specify authority*) THE CHANGES SET FORTH IN ITEM 14 ARE MADE IN THE CONTRACT ORDER NO. IN ITEM 10A.
	B. THE ABOVE NUMBERED CONTRACT/ORDER IS MODIFIED TO REFLECT THE ADMINISTRATIVE CHANGES (*such as changes in paying office, appropriation date, etc.*) SET FORTH IN ITEM 14, PURSUANT TO THE AUTHORITY OF FAR 43.103(b).
	C. THIS SUPPLEMENTAL AGREEMENT IS ENTERED INTO PURSUANT TO AUTHORITY OF:
X	D. OTHER (*Specify type of modification and authority*) UNILATERAL - FAR 52.232-0022 LIMITATION OF FUNDS

E. IMPORTANT: Contractor ☒ is not, ☐ is required to sign this document and return _____ copies to the issuing office.

14. DESCRIPTION OF AMENDMENT/MODIFICATION (*Organized by UCF section headings, including solicitation/contract subject matter where feasible.*)

a. The purpose of this modification is to provide incremental funding, as follows:

1) PR&C HJ1500-4348-0535, provides funds for obligation in the amount of $201,397.00. The total amount of funds obligated on contract CLIN 0001 is increased by $201,397.00 from $483,684.00 to the full contract value of $685,081.00.

2) It is anticipated that funds presently allotted to the contract will cover performance through the completion date of 30 October 1995.

Except as provided herein, all terms and conditions of the document referenced in Item 9A or 10A, as heretofore changed, remains unchanged and in full force and effect.

15A. NAME AND TITLE OF SIGNER (*Type or print*)		16A. NAME AND TITLE OF CONTRACTING OFFICER (*Type or print*) PATRICIA WOZNICK CONTRACTING OFFICER	
15B. CONTRACTOR/OFFEROR _____ (*Signature of person authorized to sign*)	15C. DATE SIGNED	16B. UNITED STATES OF AMERICA BY Patricia Woznick (*Signature of Contracting Officer*)	16C. DATE SIGNED

full text therewith:

SECTION	TITLE
K	REPRESENTATIONS, CERTIFICATIONS AND OTHER STATEMENTS OF BIDDERS/OFFERORS/QUOTERS

G.5 GOVERNMENT CONTRACT ADMINISTRATOR
(Fort Huachuca Local Clause 52.200-4020)

Administration of this contract shall be performed by:

Directorate of Contracting
ATTN: ATZS-DKO-I
Post Office Box 748
Fort Huachuca, Arizona 85613-0748

Point of Contact: Barbara VanDoren
Telephone Number: (602) 538-0412

G.6 ACCOUNTING CLASSIFICATION
(Fort Huachuca Local 52.200-4083 ALT II)

CLIN	ACCOUNTING CLASSIFICATION	AMOUNT

0001 & 0002 - 97404001301000 5005P4T10A841042594000000HJ150040060552JWC90000 2086 IN THE AMOUNT OF $483,684. CLINS 0001 & 0002; 97504001301000 500505T10A841142581000000HJ150043480535JWBL00S02086 in the amount of $ 201,397.00 It is anticipated that the funds currently allotted to the contract will cover the work to be performed through 30 October 1995.

G.7 SF-294 AND SF-295 REPORTING REQUIREMENTS
(FAR 19.704(A)(5) AND 52.219-9)(d)(10))
(Fort Huachuca Local 52-200.4347)

a. SF-294, Subcontracting Report for Individual Contracts, shall be submitted semi-annually by all except small businesses within 30 calendar days after the end of the reporting period to the following addressees:

(1) U.S. Army Intelligence Center and Fort Huachuca, ATTN: ATZS-DKO-I Post Office Box 748, Fort Huachuca, AZ 85613-0748

(2) U.S. Army Intelligence Center and Fort Huachuca,

,=>

12/02/98 LXG - NSFOP - CLARA BILLOCK PAGE 1
11:59:14 DETAIL

FY	APC	DOCUMENT	OBLIG	ACCRUAL	DISB
EOE	ODC	DF O-DATE D-DATE NAME			
5	JWBL	HJ150043480535	$201,397.00	$182,676.74	$182,676.74
2581	2	97069 96253 4C0017			
TOTAL FY 5					
		*	$201,397.00 *	$182,676.74 *	$182,676.74

18,720.26

MORE ....

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<PF5> NO TOTALS <PF6> STATS <PF7> BACKWARD <PF8> FORWARD
<PF9> GRAPH <PF10> SEND <PF11> LEFT <PF12> RIGHT

cost -
contract. Keeps fees - Bill on final invoice

~~FAX 617-873-3889~~
617-873-3829
BBN.

(E-mailed
by -
what office DCAA
was Audit?)

Marianne Marr
617-873- x 3153
EMAIL DIBIAS10@BBN.COM

please call -
Pat Murphy -
617-873-3056 -
cont Procedures clerk
completion date
7/31/98 -
Left mess - 3.19.99
left mess 3.24.99

2/2/99
ACO
Cecilia Shima
617-753-4186
OR. EX 41190
EX 41190

FAX 617-753-4777
will call Doreen 3/3/99

Contract Audit
DCAA - Office
Suffolk
Audit

ATLAS - DFAS-IN CASSANDRA COOPER

DOC_NO	FAPC	EOE	TA	AMOUNT	ODC	BLK	JULIAN	DOV
HJ150043480535	5JWBL	2581	23	0.00	2	WWB	7069	4C0017
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23: Count = 1

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HJ150043480535	5JWBL	2581	32	438.18	2	X53	6253	
HJ150043480535	5JWBL	2581	32	147.65	2	X48	6248	
			32	1669.88				

32: Count = 3

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HJ150043480535	5JWBL	2581	40	438.18	2	X53	6253	205459
HJ150043480535	5JWBL	2581	40	147.65	2	X48	6248	205185
			40	1669.88				

40: Count = 3

Total records printed: 7

AMENDMENT OF SOLICITATION/MODIFICATION OF CONTRACT

CONTRACT ID CODE	PAGE OF PAGES
U	1 | 2

2. AMENDMENT/MODIFICATION NO.	3. EFFECTIVE DATE	4. REQUISITION/PURCHASE REQ. NO.	5. PROJECT NO. *(If applicable)*
P00001	95 JAN 11	HJ1500-4348-0535	DAR4 A841/14

6. ISSUED BY	CODE	7. ADMINISTERED BY *(If other than Item 6)*	CODE
DKO-I		C22	

DIRECTORATE OF CONTRACTING
ATTN: ATZS-DKO-I
POST OFFICE BOX 748
FORT HUACHUCA, AZ 85613-0748
BARBARA C. VANDOREN (602)538-0412

BARBARA VANDOREN
(703) 538-0412

8. NAME AND ADDRESS OF CONTRACTOR *(No., street, county, State and ZIP Code)*

BOLT, BERANEK & NEWMAN, INC.
ATTN: MS DIBLASIO
10 MOULTON STREET
CAMBRIDGE, MA 02138

CODE 269700 FACILITY CODE

(√)	9A. AMENDMENT OF SOLICITATION NO.
	9B. DATED *(SEE ITEM 11)*
X	10A. MODIFICATION OF CONTRACT/ORDER NO. DABT63-94-C-0017
	10B. DATED *(SEE ITEM 13)* 94 APR 05

11. THIS ITEM ONLY APPLIES TO AMENDMENTS OF SOLICITATIONS

☐ The above numbered solicitation is amended as set forth in Item 14. The hour and date specified for receipt of Offers ☐ is extended, ☐ is not extended.

Offers must acknowledge receipt of this amendment prior to the hour and date specified in the solicitation or as amended, by one of the following methods:

(a) By completing Items 8 and 15, and returning _____ copies of the amendment; (b) By acknowledging receipt of this amendment on each copy of the offer submitted; or (c) By separate letter or telegram which includes a reference to the solicitation and amendment numbers. FAILURE OF YOUR ACKNOWLEDGEMENT TO BE RECEIVED AT THE PLACE DESIGNATED FOR THE RECEIPT OF OFFERS PRIOR TO THE HOUR AND DATE SPECIFIED MAY RESULT IN REJECTION OF YOUR OFFER. If by virtue of this amendment you desire to change an offer already submitted, such change may be made by telegram or letter, provided each telegram or letter makes reference to the solicitation and this amendment, and is received prior to the opening hour and date specified.

12. ACCOUNTING AND APPROPRIATION DATA *(If required)*

SEE SECTION G NET INCREASE: $201,397.00

13. THIS ITEM APPLIES ONLY TO MODIFICATIONS OF CONTRACTS/ORDERS, IT MODIFIES THE CONTRACT/ORDER NO. AS DESCRIBED IN ITEM 14.

(√)	A. THIS CHANGE ORDER IS ISSUED PURSUANT TO: *(Specify authority)* THE CHANGES SET FORTH IN ITEM 14 ARE MADE IN THE CONTRACT ORDER NO. IN ITEM 10A.
	B. THE ABOVE NUMBERED CONTRACT/ORDER IS MODIFIED TO REFLECT THE ADMINISTRATIVE CHANGES *(such as changes in paying office, appropriation date, etc.)* SET FORTH IN ITEM 14, PURSUANT TO THE AUTHORITY OF FAR 43.103(b).
	C. THIS SUPPLEMENTAL AGREEMENT IS ENTERED INTO PURSUANT TO AUTHORITY OF:
X	D. OTHER *(Specify type of modification and authority)* UNILATERAL - FAR 52.232-0022 LIMITATION OF FUNDS

E. IMPORTANT: Contractor ☒ is not, ☐ is required to sign this document and return _____copies to the issuing office.

14. DESCRIPTION OF AMENDMENT/MODIFICATION *(Organized by UCF section headings, including solicitation/contract subject matter where feasible.)*

a. The purpose of this modification is to provide incremental funding, as follows:

1) PR&C HJ1500-4348-0535, provides funds for obligation in the amount of $201,397.00. The total amount of funds obligated on contract CLIN 0001 is increased by $201,397.00 from $483,684.00 to the full contract value of $685,081.00.

2) It is anticipated that funds presently allotted to the contract will cover performance through the completion date of 30 October 1995.

Except as provided herein, all terms and conditions of the document referenced in Item 9A or 10A, as heretofore changed, remains unchanged and in full force and effect.

15A. NAME AND TITLE OF SIGNER *(Type or print)*		16A. NAME AND TITLE OF CONTRACTING OFFICER *(Type or print)* PATRICIA WOZNICK CONTRACTING OFFICER	
15B. CONTRACTOR/OFFEROR *(Signature of person authorized to sign)*	15C. DATE SIGNED	16B. UNITED STATES OF AMERICA BY Patricia Woznick *(Signature of Contracting Officer)*	16C. DATE SIGNED

b. Remove page G-3 and insert revised page G-3 in lieu thereof. Changes are denoted by a verticle line in the left margin of the revised page.

c. This contract is fully funded and the contract value remains at $685,081.00.

NOTE: Funds Status	FROM	BY	TO
Obligated	$483,684.00	$201,397.00	$685,081.00
Unfunded	201,397.00	201,397.00	-0-
TOTAL	$685,081.00		$685,081.00

MEMORANDUM FOR RECORD 11 Jan 95

SUBJECT: Contract DABT63-94-C-0017, Modification P00001, BBN

1. Procurement History:

This contract was awarded on 05 Apr 94 as a Cost Plus Fixed Fee with an estimated value of $685,081.00. This R&D action provided an effort for "BodyLAN: A Wireless, Body Local Area Network" as a result of a Broad Agency Announcement from ARPA.

2. Procurement Background:

At the time of award, the contract was incrementally funded in the amount of $483,684.00 to cover performance through 31 March 95. This action will provide additional funding.

3. Funding:

PR&C HJ154348-0535, dated 16 Dec 94, received 9 Jan 95, provides additional funds in the amount of $201,397.00. $38,969.00 Excess funds were provided.

4. Procurement Situation:

The funds provided will cover performance through 30 October 1995 (contract expiration). The additional funds will fully fund this contract in the amount of $685,081.00.

5. Procurement Action:

Modification P00001 will be issued unilaterally under FAR 52.232-00222, "Limitation of Funds", to increase the obligated funds to $685,081.00 and cover performance through contract completion, 30 October 1995.

Barbara VanDoren, Contract Specialist

AMENDMENT OF SOLICITATION/MODIFICATION OF CONTRACT

1. CONTRACT ID CODE	PAGE OF PAGES
U	1 2

2. AMENDMENT/MODIFICATION NO.	3. EFFECTIVE DATE	4. REQUISITION/PURCHASE REQ. NO.	5. PROJECT NO. (If applicable)
P00002	10/31/95	HJ1500-4348-0535	DAR4 A841/14

6. ISSUED BY	CODE	7. ADMINISTERED BY (If other than Item 6)	CODE
DKO-I		EMPTY	

DIRECTORATE OF CONTRACTING
ATTN: ATZS-DKO-I
POST OFFICE BOX 12748
FORT HUACHUCA AZ 85670-2748
BARBARA VANDOREN C22(520) 533-1549

8. NAME AND ADDRESS OF CONTRACTOR (No., street, county, State and ZIP Code) Vendor ID: 00017737

BOLT BERANEK & NEWMAN INC
MARGUERITE DIBLASIO
10 MOULTON STREET
CAMBRIDGE MA 02138

CODE 26970 FACILITY CODE

(X) | 9A. AMENDMENT OF SOLICITATION NO.: 1
9B. DATED (SEE ITEM 11):
X | 10A. MODIFICATION OF CONTRACT/ORDER NO.: DABT63-94-C-0017
10B. DATED (SEE ITEM 13): 94 APR 05

11. THIS ITEM ONLY APPLIES TO AMENDMENTS OF SOLICITATIONS

☐ The above numbered solicitation is amended as set forth in Item 14. The hour and date specified for receipt of Offers ☐ is extended, ☐ is not extended.
Offers must acknowledge receipt of this amendment prior to the hour and date specified in the solicitation or as amended, by one of the following methods: (a) By completing Items 8 and 15, and returning _____ copies of the amendment; (b) By acknowledging receipt of this amendment on each copy of the offer submitted; or (c) By separate letter or telegram which includes a reference to the solicitation and amendment numbers. FAILURE OF YOUR ACKNOWLEDGMENT TO BE RECEIVED AT THE PLACE DESIGNATED FOR THE RECEIPT OF OFFERS PRIOR TO THE HOUR AND DATE SPECIFIED MAY RESULT IN REJECTION OF YOUR OFFER. If by virtue of this amendment you desire to change an offer already submitted, such change may be made by telegram or letter, provided each telegram or letter makes reference to the solicitation and this amendment, and is received prior to the opening hour and date specified.

12. ACCOUNTING AND APPROPRIATION DATA (If required)
See Section G THIS IS NOT AN OBLIGATION OF FUNDS
Mod Obligated Amount US $0.00

13. THIS ITEM APPLIES ONLY TO MODIFICATIONS OF CONTRACTS/ORDERS, IT MODIFIES THE CONTRACT/ORDER NO. AS DESCRIBED IN ITEM 14.

(X)	A. THIS CHANGE ORDER IS ISSUED PURSUANT TO: (Specify authority) THE CHANGES SET FORTH IN ITEM 14 ARE MADE IN THE CONTRACT ORDER NO. IN ITEM 10A.
	B. THE ABOVE NUMBERED CONTRACT/ORDER IS MODIFIED TO REFLECT THE ADMINISTRATIVE CHANGES (such as changes in paying office, appropriation date, etc.) SET FORTH IN ITEM 14, PURSUANT TO THE AUTHORITY OF FAR 43.103 (b).
	C. THIS SUPPLEMENTAL AGREEMENT IS ENTERED INTO PURSUANT TO AUTHORITY OF:
X	D. OTHER (Specify type of modification and authority) UNILATERAL - F.4, Contract Period of Performance.

E. IMPORTANT: Contractor ☒ is not, ☐ is required to sign this document and return _____ copies to the issuing office.

14. DESCRIPTION OF AMENDMENT/MODIFICATION (Organized by UCF section headings, including solicitation/contract subject matter where feasible.)

a. The purpose of this modification to extend the term of the contract, as follows:

1) The expiration date of the contract is extended, at no additional cost to the Government:

FROM: 31 October 1995

TO: 31 July 1996

Except as provided herein, all terms and conditions of the document referenced in Item 9A or 10A, as heretofore changed, remains unchanged and in full force and effect.

15A. NAME AND TITLE OF SIGNER (Type or print)		16A. NAME AND TITLE OF CONTRACTING OFFICER (Type or print) TONI L. DAVIES C18	
15B. CONTRACTOR/OFFEROR (Signature of person authorized to sign)	15C. DATE SIGNED	16B. UNITED STATES OF AMERICA BY Toni L Davies (Signature of Contracting Officer)	16C. DATE SIGNED 11/2/95

2) Remove page F-1 and substitute the attached page F-1 in lieu thereof. Changes are denoted by a vertical line in the left margin.

b. All other terms and conditions remain unchanged.

SECTION F
DELIVERIES OR PERFORMANCE

F.1 52.212-0013 I STOP-WORK ORDER (AUG 1989)--ALTERNATE I (APR 1984)
(Reference 12.505(b)(2)

F.2 52.247-0034 F.O.B. DESTINATION (NOV 1991)
(Reference 47.303-6(c))

F.3 DELIVERY OF DATA
(Fort Huachuca Local 52.200-4051)

The data to be delivered in accordance with Contract Data Requirements List, DD Form 1423, (Exhibit A), shall be delivered in accordance with the instructions on the form. Data furnished to the Government, under this contract, shall be transmitted by letter to the address contained in Block 14 of the Contract Data Requirements List. A copy of the transmittal letter forwarding the data to the distribution address, shall be furnished to the Contracting Officer referenced in SECTION G., clause entitled GOVERNMENT CONTRACT ADMINISTRATOR.

F.4 CONTRACT PERIOD OF PERFORMANCE

It is estimated that the period of performance will extend from date of contract award through 31 Jul 96 both dates inclusive, unless sooner terminated under the provisions of the contract. If at a later date it becomes necessary to extend the period of performance due to uncertainties associated with performing R&D requirements, IAW DFARS 35.002, the performance period will not extend beyond 10 years.

END OF SECTION F

AMENDMENT OF SOLICITATION/MODIFICATION OF CONTRACT

CONTRACT ID CODE: U | PAGE OF PAGES: 1 2

2. AMENDMENT/MODIFICATION NO.	3. EFFECTIVE DATE	4. REQUISITION/PURCHASE REQ. NO.	5. PROJECT NO. (If applicable)
P00003	03/14/96	HJ1500 4348-0535	DAR6 A841/14

6. ISSUED BY CODE DKO-I

DIRECTORATE OF CONTRACTING
ATTN: ATZS-DKO-I
POST OFFICE BOX 12748
FORT HUACHUCA AZ 85670-2748
BARBARA VANDOREN C22(520) 533-1549

7. ADMINISTERED BY (If other than item 6) CODE EMPTY

8. NAME AND ADDRESS OF CONTRACTOR (No., street, county, State and ZIP Code) Vendor ID: 00017737

BOLT BERANEK & NEUMAN INC
MARGUERITE DIBLASIO
10 MOULTON STREET
CAMBRIDGE MA 02138

CODE 26970 FACILITY CODE

(X) | 9A. AMENDMENT OF SOLICITATION NO.

9B. DATED (SEE ITEM 11)

X | 10A. MODIFICATION OF CONTRACT/ORDER NO. DABT63-94-C-0017

10B. DATED (SEE ITEM 13) 94 APR 05

11. THIS ITEM ONLY APPLIES TO AMENDMENTS OF SOLICITATIONS

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12. ACCOUNTING AND APPROPRIATION DATA (If required) Mod Obligated Amount US $0.00

THIS IS NOT AN OBLIGATION OF FUNDS

13. THIS ITEM APPLIES ONLY TO MODIFICATIONS OF CONTRACTS/ORDERS, IT MODIFIES THE CONTRACT/ORDER NO. AS DESCRIBED IN ITEM 14.

(X) A. THIS CHANGE ORDER IS ISSUED PURSUANT TO: (Specify authority) THE CHANGES SET FORTH IN ITEM 14 ARE MADE IN THE CONTRACT ORDER NO. IN ITEM 10A

B. THE ABOVE NUMBERED CONTRACT/ORDER IS MODIFIED TO REFLECT THE ADMINISTRATIVE CHANGES (such as changes in paying office, appropriation data, etc.) SET FORTH IN ITEM 14, PURSUANT TO THE AUTHORITY OF FAR 43.103 (b).

X | C. THIS SUPPLEMENTAL AGREEMENT IS ENTERED INTO PURSUANT TO AUTHORITY OF: 10 USC 2304

D. OTHER (Specify type of modification and authority)

E. IMPORTANT: Contractor ☐ is not. ☒ is required to sign this document and return 1 copies to the issuing office.

14. DESCRIPTION OF AMENDMENT/MODIFICATION (Organized by UCF section headings, including solicitation/contract subject matter where feasible.)

a. The purpose of this modification is to acknowledge the transfer of equipment, as follows:

1) One (1) Keyboard, #101, SN: 81740742 is hereby transferred from the contract cited in Block 10A to contract DABT63-95-C-0013.

2) The contractor may utilize the equipment under the contract

Except as provided herein, all terms and conditions of the document referenced in Item 9A or 10B, as heretofore changed, remains unchanged and in full force and effect.

15A. NAME AND TITLE OF SIGNER (Type or print)	16A. NAME AND TITLE OF CONTRACTING OFFICER (Type or print)
Mark J. Sherman, Senior Manager, Contract Relations	JONI L. DAVIES C18

15B. CONTRACTOR/OFFEROR	15C. DATE SIGNED	16B. UNITED STATES OF AMERICA	16C. DATE SIGNED
Mark J. Sherman (Signature of person authorized to sign)	18MAR96	BY Joni L. Davies (Signature of Contracting Officer)	19 Mar 96

NSN 7540-01-152-8070
PREVIOUS EDITION UNUSABLE

30-105

STANDARD FORM 30 (REV. 10-83)
Prescribed by GSA
FAR (48 CFR) 53.243

AMENDMENT OF SOLICITATION/MODIFICATION OF CONTRACT

CONTRACT ID CODE	PAGE OF PAGES
U	1 2

2. AMENDMENT/MODIFICATION NO.	3. EFFECTIVE DATE	4. REQUISITION/PURCHASE REQ. NO.	5. PROJECT NO. (If applicable)
P00003	03/14/96	HJ1500 4348-0535	DAR6 A841/14

6. ISSUED BY	CODE	7. ADMINISTERED BY (If other than Item 6)	CODE
DIRECTORATE OF CONTRACTING ATTN: ATZS-DKO-I POST OFFICE BOX 12748 FORT HUACHUCA AZ 85670-2748 BARBARA VANDOREN C22(520) 533-1549	DKO-I		EMPTY

8. NAME AND ADDRESS OF CONTRACTOR (No., street, county, State and ZIP Code)	(X)	9A. AMENDMENT OF SOLICITATION NO.
Vendor ID: 00017737 BOLT BERANEK & NEWMAN INC MARGUERITE DIBLASIO 10 MOULTON STREET CAMBRIDGE MA 02138		9B. DATED (SEE ITEM 11)
	X	10A. MODIFICATION OF CONTRACT/ORDER NO. DABT63-94-C-0017
		10B. DATED (SEE ITEM 13) 94 APR 05

CODE 26970	FACILITY CODE

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	D. OTHER (Specify type of modification and authority)

E. IMPORTANT: Contractor ☐ is not, ☒ is required to sign this document and return 1 copies to the issuing office.

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Except as provided herein, all terms and conditions of the document referenced in Item 9A or 10A, as heretofore changed, remains unchanged and in full force and effect.

15A. NAME AND TITLE OF SIGNER (Type or print)		16A. NAME AND TITLE OF CONTRACTING OFFICER (Type or print) TONI L. DAVIES C18	
15B. CONTRACTOR/OFFEROR (Signature of person authorized to sign)	15C. DATE SIGNED	16B. UNITED STATES OF AMERICA BY (Signature of Contracting Officer)	16C. DATE SIGNED

cited in Block 10A until such use is no longer required.

b. All other terms and conditions remain unchanged.

AMENDMENT OF SOLICITATION/MODIFICATION OF CONTRACT

CONTRACT ID CODE	PAGE	OF PAGES
U	1	1

2. AMENDMENT/MODIFICATION NO.	3. EFFECTIVE DATE	4. REQUISITION/PURCHASE REQ. NO.	5. PROJECT NO. (If applicable)
P00005	See Block 16c	HJ1500-4348-0535	DAR A841/14

6 ISSUED BY	CODE	7. ADMINISTERED BY (If other than Item 6)	CODE
Directorate of Contracting ATTN: ATZS-DKO-I P.O. Box 12748 Fort Huachuca, AZ 85670-2748 Liz Amatulli (520) 533-8948	DABT63		

8. NAME AND ADDRESS OF CONTRACTOR (No., street, county, State and ZIP Code)	(√)	9A. AMENDMENT OF SOLICITATION NO.
Bolt, Beranek, and Newman, Inc. ATTN: Marguerite DeBlasio 10 Moulton Street Cambridge, MA 02138		9B. DATED (SEE ITEM 11)
	X	10A. MODIFICATION OF CONTRACTS/ORDER NO. DABT63-94-C-0017
CODE 26970 FACILITY CODE		10B. DATED (SEE ITEM 13) 5 April 1994

11. THIS ITEM ONLY APPLIES TO AMENDMENTS OF SOLICITATIONS

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(a) By completing Items 8 and 15 and returning _____ copies of the amendment; (b) By acknowledging receipt of this amendment on each copy of the offer submitted; or (c) By separate letter or telegram which includes a reference to the solicitation and amendment numbers. FAILURE OF YOUR ACKNOWLEDGMENT TO BE RECEIVED AT THE PLACE DESIGNATED FOR THE RECEIPT OF OFFERS PRIOR TO THE HOUR AND DATE SPECIFIED MAY RESULT IN REJECTION OF YOUR OFFER. If by virtue of this amendment you desire to change an offer already submitted, such change may be made by telegram or letter, provided each telegram or letter makes reference to the solicitation and this amendment, and is received prior to the opening hour and date specified.

12. ACCOUNTING AND APPROPRIATION DATA (If required)

97504001301ORPAICFP5T10A841142581000000HJ150043480535JWBL00S02086 DECREASE $9,889.28

13. THIS ITEM APPLIES ONLY TO MODIFICATIONS OF CONTRACTS/ORDERS, IT MODIFIES THE CONTRACT/ORDER NO. AS DESCRIBED IN ITEM 14.

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X	D. OTHER (Specify type of modification and authority) IAW 10 U.S.C. 2304(c) UNILATERAL

E. IMPORTANT: Contractor ☒ is not, ☐ is required to sign this document and return _____ copies to the issuing office.

14. DESCRIPTION OF AMENDMENT/MODIFICATION (Organized by UCF section headings, including solicitation/contract subject matter where feasible.)

a. The purpose of this modification is to deobligate excess funding and close subject contract. The estimated value and the obligation amounts are both decreased by $9,889.28 from $685,081 to $675,191.72. The accounting and appropriation data are at Block 12 above.

b. This action closes this contract.

Except as provided herein, all terms and conditions of the document referenced in Item 9A or 10A, as heretofore changed, remains unchanged and in full force and effect.

15A. NAME AND TITLE OF SIGNER (Type or print)		16A. NAME AND TITLE OF CONTRACTING OFFICER (Type or print) BARBARA C. VANDOREN	
15B. CONTRACTOR/OFFEROR (Signature of person authorized to sign)	15C. DATE SIGNED	16B. UNITED STATES OF AMERICA BY (Signature of Contracting Officer)	16C. DATE SIGNED 17 Feb 00

BBN Systems and Technologies
A Division of Bolt Beranek and Newman Inc.

BAA9327-P-016

4 Feb 1994 (ESTO)

BBN Proposal No. P94-LABS-C-002
ARPA Abstract Control # BAA9327-A-89

BodyLAN™: A Wireless Body Local Area Network

Wireless, Adaptive and Mobile Information Systems (WAMIS)
Area 1: Wireless Computing Systems

Volume I. Technical and Management Proposal

Submitted to: ARPA/ESTO in Response to BAA 93-27

Submitted by: BBN Systems and Technologies
A Division of Bolt Beranek and Newman Inc.
10 Moulton Street
Cambridge, MA 02140
BBN's business category: LARGE BUSINESS
Fax: (617)873-3776

Technical POC: Philip P. Carvey
(617) 873-3208
PCarvey@BBN.COM

Administrative POC: Marguerite DiBlasio
(617) 873-3153
MDiblasio@BBN.COM

™BodyLAN™ is a trademark of Bolt Beranek and Newman, Inc.

BBN Proposal No. P94-LABS-C-002
ARPA Abstract Control # BAA9327-A-89

BodyLAN™: A Wireless Body Local Area Network

Wireless, Adaptive and Mobile Information Systems (WAMIS)
Area 1: Wireless Computing Systems

Volume I. Technical and Management Proposal

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MDiblasio@BBN.COM

Table of Contents

Section I. Administrative

See Cover Page.

Section II. Summary of BodyLAN[1] Proposal

This section provides an overview of the proposed work, as well as an introduction to the associated technical and management issues. This summary plan is described and discussed in more detail in Section III, Detailed Proposal Information.

BBN proposes to develop the means for very low power wireless communications over a human body area. This development will comprise: the theoretical basis for the communications protocol, interface standards between body computer and modem, interface standards between sensor/transducer and modem, a prototype system demonstrating the technology, and a performance evaluation. Preliminary work done by BBN over the last two years suggests that by using spread spectrum techniques and a communications protocol especially suited for low power implementation, wireless modems can be constructed occupying a few hundred cubic millimeters and consuming a few hundred microwatts.

The key technical issues we will address in this development are:

- Wireless operation in compliance with license-free FCC Part 15 Regulations.
- Operation at microwatt power levels.
- Immunity to interference from similar and dissimilar systems
- Submicrosecond synchronization of all devices.

Motivation for this development is easy to find in both military and commercial applications, e.g. health sensors, special mission accessories, and training aids. Numerous sources have forecast that hip-worn computers, integrated with wired and wireless broadband networks, will fundamentally change the way people interact with their environment. Individuals will wear computers like clothing and jewelry. This evolution is not ten years out but is currently underway. Recently a "wearable computing" fashion show was presented in New York.

Apple Computer has named these computing devices Personal Digital Assistants (PDAs) and has introduced an initial implementation called Newton. Another company is already offering a hip-worn computer for general sale. As technology evolves, there will be a steady evolution to smaller, lighter, and cheaper PDAs having more powerful processors, more storage, and seamless communication with the information infrastructure. The technology being proposed here may enhance this evolution. BBN Systems and Technology has trademarked this technology as "BodyLAN™".

We envision an environment in which a PDA would be worn on a person's hip. This PDA would not be used directly as are today's laptop computers; rather it would communicate with ultra-lightweight devices called Personal Electronic Accessories (PEAs). Routine interactions with one's PDA would be accomplished exclusively via

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[1] BodyLAN™ is a trademark of Bolt Beranek and Newman, Inc.

these sensors/transducer PEAs. A PEA display device could be created today small enough to be worn like a wrist watch. Another PEA could include a gravitational and magnetic field sensor crafted to look like finger rings. These devices could be used to allow sign-language-like direct communications to the PDA. A PEA worn in the ear could give auditory feedback from the PDA. Low power health applications are too numerous to list.

Open standards for communication between PDAs and PEAs (possibly from different vendors) are central to the success of this vision. Our proposed work is:

- Formalize the BodyLAN communications architecture and develop a theoretical framework for its expected error rate under conditions of multiple near-field BodyLANs, narrow band interferers, and component aging.
- Produce a specification document describing the conceptual and hardware interface to the PEA modem, the interface to the PDA modem, and parameter initialization protocols.
- Build a digital PEA having a pseudo random sequence generator/checker, a microprocessor-driven PDA modem, and an interface to one of the existing PDAs. All hardware will utilize existing RF, field programmable logic devices, and microprocessor components.
- Evaluate the robustness, ease-of-use, and performance of the prototype systems.

Even though BodyLAN is about wireless communication, transmitting and receiving an RF signal over a distance of a few meters is not the hard part. Since all PEAs must be battery powered and very small, the challenges arise mostly from power consumption concerns. Basically, BodyLAN is concerned with converting electrical signals into radiated power at acceptable efficiencies. Since the FCC limits the radiated power to under 12 nanowatts, even a 12 microwatt power budget represents an efficiency of only 0.1%. While this efficiency appears incredibly small, to our knowledge, no one has ever constructed an RF modem and controller at these low power levels. Our preliminary work has shown just the local oscillator would consume tens of microwatts using the most efficient oscillator currently known.

Improving our understanding of "where the power goes" will be one of the contributions of the BodyLAN's research. It has been painfully clear in the last two years of work on BodyLAN that this understanding will be evolutionary and will no doubt involve many researchers over an extended period of time. The technological problems to be solved are hard problems. Like IC process technology where the question is "what are the limits of integration?", clever scientists and engineers have kept pushing the limits in an evolutionary manner. BodyLAN provides an excellent application for low-power research as it involves a complex interaction between protocol, circuit design, and IC processes with potentially a huge payoff.

BBN has structured the proposed research to focus on creating and evaluating a prototype system which examines the protocol issues of one BodyLAN architecture. Since the prototype will be constructed with no custom components other than Field Programmable Logic Devices, no power-consumption optimization will be possible other than what is achievable through protocol enhancements. We plan however on using SPICE simulations to gain a better understanding of power consumption of individual circuit sections to better drive the protocol decisions.

II. A. Innovative Claims for the Proposed Research

The principal innovative idea is that wireless BodyLAN can be done at all. Since the BodyLAN architecture was designed from the ground up to minimize power consumption, have ultra small size and weight, and require no user intervention, many innovative ideas were integrated into the architecture. They include:

- PEAs contain a crystal oscillator synchronized to the hub within a temporal uncertainty of a few tens of nanoseconds. This allows the full range of time multiplexing and spread spectrum techniques to be applied to solve problems of bandwidth allocation, spatial reuse by multiple BodyLANs, and robustness against narrow band interferers.
- A procedure and protocol for parameterizing PEAs to an individual hub such that they may regain synchronization after sleeping even in the near-field presence of other active PDAs.
- The use of Optical Orthogonal Codes (described in II. D. below) to reduce power consumption by almost an order of magnitude and still achieve spatial reuse.
- New analog and RF circuits which have very fast power-down and power-up times.
- Adaptive power transmission protocols which cause the PEAs and PDA modem to minimize transmitted RF power.
- Support for both analog and digital communications using the same protocol.
- A protocol which allows non-licensed use of any frequency bands below 1 GHz in which the FCC allows intentional transmitters. By employing temporarily randomized RF pulses, the average radiated power of a PEA or hub modem can be brought under the maximum radiated power allowed and still allow communication over short distances.
- Adaptive circuit techniques which bias the RF circuits at less current than normal worst case design techniques. These technique typically reduce power consumption by a factor of three over conventional worst case designs.
- Interface standards which are vendor and device independent (an open architecture).
- A new synchronization protocol which allows collisions of synchronization beacons between multiple BodyLANs.

This development will provide an advanced capability in personal communications. BodyLAN is one part of the triad of PEAs, PDA, and application programs which will fundamentally change the way people interact with computers and the information infrastructure. A whole new industry may emerge from ARPA's success in this program.

II. B. Deliverables

We will provide an analysis, develop a prototype, and evaluate a new wireless body local area network. Deliverables are:

- A document describing in detail the BodyLAN™ architecture, its limitations, and the FCC restrictions (if any).
- A specification describing interfacing to the PEA modem, the PDA modem, and the PDA of choice.
- A mathematical analysis of the Optically Orthogonal Codes used for the main data transfer link and different synchronization protocols. This analysis will explore the effects of various parameters such as narrowband interference power, multiple BodyLAN space sharing, and modulation diversity on error rates, synchronization acquisition probability, and power consumption.
- A set of eight PEA modems, three PDA modem cards, and a data pattern generator and checker PEA. These prototypes will be constructed using only existing RF and telecommunications chips, field programmable logic devices, and surface mounted discrete components on small PC boards. These prototypes will not attain the potential small size and low power consumption but will demonstrate the architecture and operation.
- Software on the PDA interface needed to compare the hardware performance with theoretical models.
- An evaluation of the architecture to verify its robustness and its theoretical performance.

With ARPA's concurrence, we will present these findings at appropriate wireless technology symposia, and publish our technical results in the appropriate communications journals.

The BodyLAN architecture was developed under BBN IR&D, and we are currently seeking a patent for this technology. However, we will grant a no cost license to the Government for applications of this technology.

II. C. Cost, Schedule and Milestones

The cost for this program is $724 K.

We anticipate that this contract will be awarded on October 1, 1993, with a period of performance of 18 months, as shown in Figure 1.

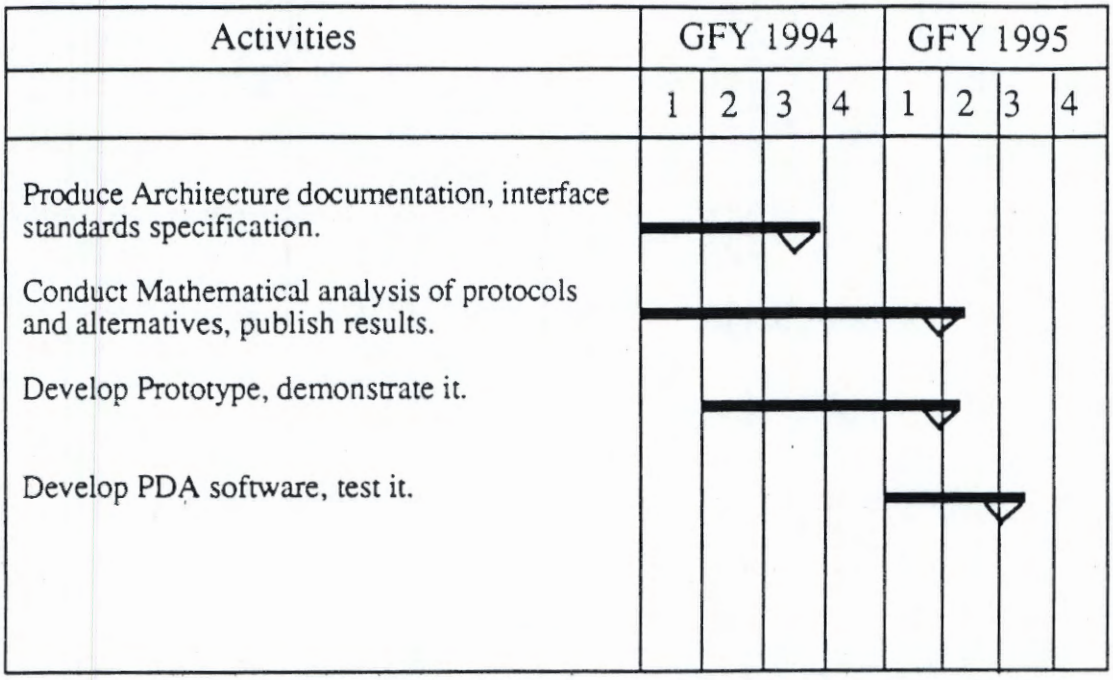

Figure 1: Schedule With Major Milestone Completion Dates

II. D. Technical Rationale, Technical Approach, and Constructive Plan

This section provides a summary of our plans for accomplishing the goals of this project. Section III C and D provide complete details of our plan.

Technical Rationale

Figure 2 illustrates the BodyLAN system. The architecture assumes transducer functions are handled in Personal Electronic Accessories (PEAs) controlled by application code executed on the PDA. A PCMCIA card implementing the BodyLAN hub modem plugs into the user's PDA. Control of the BodyLAN communications activities are implemented in a low-power processor residing on this card.

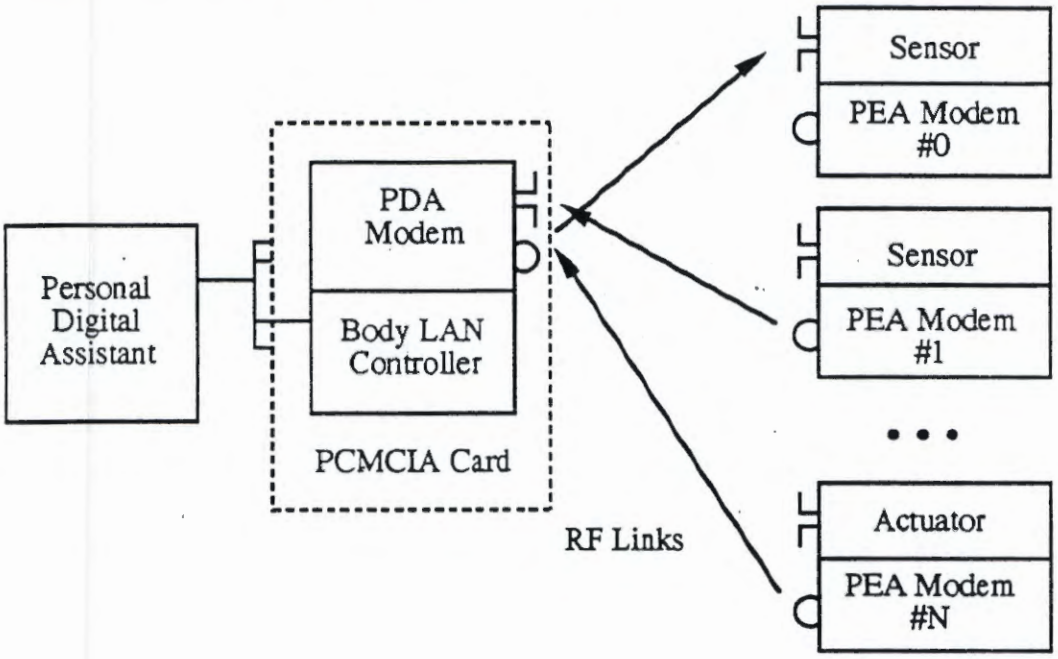

Figure 2: BodyLAN System

BodyLAN has a star topology where PEA modems communicate only with the PDA modem. PEAs operate as half duplex devices. Further, they do not receive simultaneously on the outbound channel and the synchronization channel. The PDA operates as a full duplex device, except that it does not transmit or receive application data when sending the synchronization beacons. This simplifies reception at the PEAs and is not an obstacle since no PEA should transmit or receive while its PDA is transmitting a synchronization beacon.

We have examined high frequency acoustic, infrared, and electromagnetic propagation between the hub and PEAs and have chosen electromagnetic propagation. Even with its crowded spectrum and FCC regulatory problems, RF signaling has many advantages over the alternatives.

The radio frequency spectrum is crowded and highly regulated. More than 30,000 channels are licensed by the FCC just in the Northeastern part of the United States (under 1000 MHz). For BodyLAN, we need to find a way to coexist with these licensed channels in such a way that the FCC will accept BodyLAN emitters and existing licensees will not object. Part 15 specifies 15 bands under 1000 MHz in which emission can be intentional but of limited field strengths. Typical field strengths correspond to a radiated power of 12 nanowatts.

While at first this power level appears incredibly small, thereby denying us the advantages of using RF communications, it turns out that generating and receiving such a signal at short distances is surprisingly easy. With a 400 MHz carrier, a receiver dipole of length 20 millimeters generates a voltage 10.5 microvolts at the maximum field strength allowed by the FCC. This signal level is 30 times the sensitivity of a conventional FM receiver.

An emitter having a maximum field emission of 20,000 microvolts per meter pulsed one microsecond on and 99 microseconds off has an average field strength of 200 microvolts per meter. If a wideband receiver is synchronized to the transmitter and only samples the received signal when the transmitter is sending, then it "sees" a 20,000 microvolts per meter field, not the 200 microvolts per meter average.

An important advantages of short distance communications is the comparative ease of synchronization. Maximum PEA/PDA separation distance is expected to be less than 1.4 meters (55 inches) for a hip-worn PDA. This corresponds to less than 10 nsec of temporal uncertainty for a PEA anywhere within the 2.8 meter diameter sphere surrounding the PDA.

Pulsed operation is desirable from a power conservation standpoint because transistors need large bias currents to obtain high gain and high frequency operation. By employing fast startup linear circuits operating at low duty cycles, low power consumption is obtained.

Synchronization between PEAs and the PDA is clearly the key to the entire BodyLAN concept. It is also the most challenging protocol problem to be solved. Principal requirements of a synchronization protocol are low power consumption, low complexity, and the ability to quickly reacquire synchronization after losing synchronization without disturbing other PEA/PDA communications.

We envision using a separate frequency band exclusively for the broadcast of synchronization signals called beacons. Since this synchronization band is shared, beacons from adjacent BodyLANs will interfere with one another. A PEA in one BodyLAN can actually receive a beacon from another PDA having a signal strength greater than from its own PDA. Signal strength alone is insufficient to determine the home PDA. One of the main problems in creating a synchronization protocol is that PDAs cannot detect a beacon collision at all the PEA sites. A PEA must therefore must be able to acquire synchronization in the presence of collisions from adjacent PDA.

In use, PEAs of one BodyLAN must share the same physical volume of adjacent BodyLANs. We require that adjacent BodyLANs not interfere with one another catastrophically but will allow some increase in error rate. In normal operation, the PDA will monitor the received power level and error rates. It adjusts the transmitted power

levels of itself and the PEAs to achieve the desired error rate. Thus PEAs close to the PDA would transmit at lower power levels than PEAs further away from the PDA. This power management tends to limit the effect of one BodyLAN on another. Moreover, the "FM Capture Effect" causes a receiver to completely "capture" the stronger of two FM signal having the same carrier frequency.

Technical Approach

The BodyLAN architecture calls for three frequency bands. Two bands, at 346.03 MHz and 387.97 MHz are used for application data and we label them the inbound channel and outbound channel respectively. The PDA transmits in the outbound channel and receives from the inbound channel. The situation reverses for PEAs. The third band at 367.0 is the synchronization channel and is used exclusively by the PDA to transmit a synchronization beacon to its PEAs together with some control data.

BodyLAN must operate within range of other BodyLANs. Our design uses spread spectrum transmissions to provide near-orthogonality among signals from adjacent BodyLANs. We have chosen a form of pulse position spread spectrum signal known as Optical Orthogonal Codes (OOCs). In this signaling scheme, each bit is transmitted as 64-chips. For each chip, the transmitter either sends no power (the most probable case) or transmits an RF burst above or below the carrier frequency. The locations at which power is transmitted are a codeword.

BodyLAN errors occur because two or more BodyLAN transmitters are using the same codeword and have pulses which overlap by more than 50% or when three or more transmitters using different codewords share more than a majority of pulses which overlap. For a $(63, 3, 1)^2$ code, the first error term dominates because there are few codewords. For example, the probability that two independent BodyLANs will not be sending the same data, will be synchronized within one chip time, and will be using the same codeword is about 0.1%. When more than two BodyLANs are considered, the error rate increases to about 1%.

Synchronization of PEAs to the PDA is accomplished by the PDA broadcasting beacons on a separate frequency band. Six beacons are transmitted in each 768-slot superframe, one in each frame but normally in different positions within each of the six successive frames. Each beacon is a 64-chip sequence using Frequency Shift Keying (FSK).

Each PEA contains an oscillator based on an a common watch crystal oscillating at 32,768 Hz. This oscillator is phase locked to beacons not suffering from collisions. The oscillator is sufficiently stable that once a PEA has phase locked its oscillator to the PDA's oscillator, it is very tolerant to missing beacon reception errors.

Each PEA has three major modes of operation: comatose, sleeping, and active. A PEA is dead, such as after a battery replacement, when its internal control parameters are uninitialized. When comatose, the PEA is also unsynchronized with the PDA. Our current plan calls for requiring that the PEA be physically moved close to the PDA such that the field strength emitted by the PDA is larger than a threshold. Note that this procedure is required only when the PEA's power source is disconnected.

Constructive Plan

We will conduct this research by carrying out the following tasks:

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[2] This notation signifies (number of chips, number of pulses, maximum crosscorrelation)

- Document the architecture and network protocols and develop the specification for interfacing to both the PEA modem and the PDA modem.

- Explore different synchronization protocols, error rates under narrowband interference and multiple BodyLANs, frequency diversity benefits and complexity issues, and circuit design for the various low power circuits.

- Develop the PEA modems, PDA modems, an interface to some PDA, and a data pattern generator/checker using existing RF chips, Field Programmable Logic Devices, and a low power microprocessor in the PDA interface.

- Develop the PDA interface software needed to evaluate the hardware performance versus theoretical models with respect to error rate, robustness to narrowband interference, etc.

We propose to work with some university and/or other organization (with ARPA's concurrence) on the low power circuit design issues and on the problems of integrating sensors and transducers to a PEA modem.

II. E. Comparison with Other Ongoing Research

Commercial Off-the-Shelf (COTS) Products

A number of companies have announced Personal Digital Assistants (PDAs), hand held computers. Apple Computer has announced its Newton PDA, in three models which range from $699 to $1250. The top two models will have a PCMCIA compatible radio modem to provide access to a nearby AppleLink port. Hewlett Packard has released its OmniBook 300 with an infrared communications link for $2000. This is a 2.2 pound PDA with a full-sized keyboard. AT&T has announced its Personal communicator, which functions as a computer, phone, and fax. This is a pen and notepad unit based on the AT&T Hobbit chip.

The Personal Computer Memory Card International Association (PCMCIA) has established standard specifications for credit-card-sized microcomputer add-on memories and peripherals. The cards are 54 mm wide by 85.6 mm long (2.1 by 3.4 inches) and have a 68 pin interface. Type I, Type II, and Type III cards are 3.3 mm thick, 5 mm thick, and 10.5 mm thick respectively.

This represents the current state of the art in microcomputer miniaturization, and many mainstream PCMCIA products (faxes, disks, RF modems, Ethernet adapters, static RAM, and flash memory) are now entering the market. Most notebook products now have one or more PCMCIA slots.

A number of vendors are offering license-free wireless LAN products which comply with FCC Part 15 regulations for unlicensed operation given in the Code of Federal Regulations Title 47 Part 15.247. These regulations for wireless LANs require the use of subwatt power and spread spectrum signaling within the three Industrial, Scientific and Medical (ISM) bands to minimize co-channel interference. Many of these products are packaged as PCMCIA cards which are radio modems capable of providing a wireless link at distances up to 50 meters. Examples include Toshiba's Wireless Portable Work group product and Spectrix Corp's SpectrixLite LAN product, with a $350 serial port and a $3K ISA network card. IBM Network Systems division offers its Wireless RF LAN card for $800.

Relationship to BodyLAN

BodyLAN is complementary to all the COTS technologies above, and in fact is highly synergistic to most of them. For example, we will use a COTS PDA as the central component of the body constellation of personal electronic accessories (PEAs). We will use a standard PCMCIA interface card to interface the BodyLAN to the PDA.

The COTS wireless LAN products provide connectivity from a person to his local communications infrastructure, using credit-card sized modems and subwatt power to reach over tens of meters in compliance with FCC Regulations Section 15.247. In contrast, the BodyLAN will eventually be implemented as fingernail-sized modems operating at microwatt power level to provide connectivity over a meter of personal body size, and operating under FCC Regulations Section 15.209.

The BodyLAN will serve as a seamless extension of the wireless LAN, providing connectivity from a person's PEAs (e.g., health monitors) to the global communications infrastructure.

II. F. Key Personnel and Effort

Key Personnel

Principal investigator for the BodyLAN project will be Philip Carvey.

Phil Carvey rejoined BBN in 1985 to work on the Monarch multiprocessor project. His responsibilities covered all aspects of the architecture, modeling, verification, and chip development. Prior to rejoining BBN, Mr. Carvey was V.P. of Research at Ztel Inc., where he developed research programs for a voice/data PBX. Mr. Carvey joined BBN originally in 1979 as the principal designer of the Butterfly multiprocessor. In 1969, he was one of very early employees of Applicon, Inc and served as chief hardware architect/designer.

Dr. Julio Escobar will serve as chief protocol analyst.

Julio is a senior scientist and member of the Advance Networks Department. At BBN since 1988, he has been a designer and analyst of communication protocols. He designed and developed channel access protocols for packet radio networks under the Survivable Adaptive Networks project (DARPA), and was co-developer of a congestion control algorithm for this network architecture. He was a co-designer of an adaptation layer protocol for ATM networks and is currently in charge of testing a protocol of his design for synchronization of multimedia flows. Julio also is an editor of the Journal of Fiber and Integrated Optics and has accepted an invitation to join the editorial board of the IEEE Networks magazine.

Dr. Lawrence Sher will lead the standards and BodyLAN evaluation efforts.

Larry is a division scientist at BBN and been with the company since 1971. He recently has been working on the Pathfinder project, a project involving integrating sensors and transducers to a lap-top computer using a wired LAN. Previously he was responsible for the conception, development, and application of the SpaceGraph Display. Dr. Sher has created videotape courses which teach the use of RS/1 and has taught many courses for BBN clients and BBN staff. Prior to joining BBN, he worked in developing medical electronic equipment. Dr. Sher has published 29 papers and holds a US patent on the SpaceGraph.

Effort Required

The effort proposed here will take 35 person months. Twenty-six of those person months will be spent in GFY 94, and the remaining 9 in GFY 95.

Section III: Detailed Proposal Information

This section provides the detailed discussion of our proposed work, discusses technical and management issues, and identifies the risks and payoff of the proposed work. This is a more detailed plan that enhances the discussion presented in Section II.

In this section, we discuss:

- the overall scientific and technical merit of this approach (Section III. B. and E.)
- its potential contribution and relevance to ARPA's mission (Section III. B. and C.)
- our plans and capability to accomplish this technology transition (Section III. A. and D.)
- BBN's capabilities and related experience (Section III. F, G, and H.)
- the basis of our costing (Section III. I.).

III. A. Statement of Work

Scope of the Effort

Our proposed effort is shown in the work breakdown structure of Figure 3.

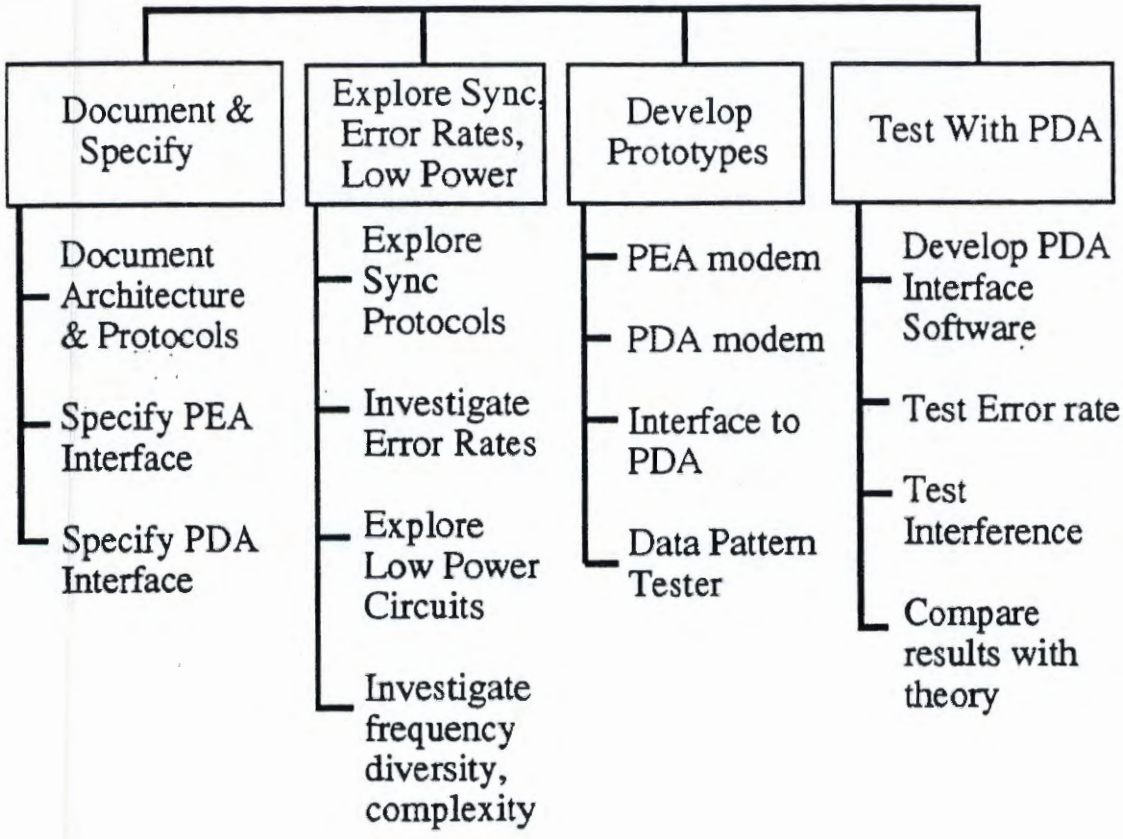

Figure 3: Work Breakdown Structure

Specific Tasks to be Performed

The ultimate goal for BodyLAN is to produce an MCM (multi-chip module) containing the PEA modem chip and a few discrete components together with the PCMCIA card which plugs into the PDA bus. This proposed effort is the first phase to reach this goal, namely to construct a prototype BodyLAN and to test it against the theoretical models developed as part of this project. As a subsequent phase, ARPA can issue an RFP to the semiconductor industry to fabricate the fully miniaturized chip version for mass production. At that point, we will have eliminated the significant technical risks and proven the feasibility of the BodyLAN architecture.

We have partitioned our work into four major areas: specification, protocol, prototype development, and evaluation. The sub-tasks within each area are explained below.

Specification Area

Document Architecture - We will create a formal description of BodyLAN suitable for other ARPA researchers to use in applying BodyLAN to their needs. The document will include a detailed architecture specification, specification of the BodyLAN network protocols, and description of the network protocol interactions and network operations. We will also report the results of our performance evaluation, a detailed theory of operation of the prototype components, and SPICE simulation results of low-power alternative circuits to be used in single chip implementations.

Document PEA Interface - A detailed description of the PEA modem interface will be provided together with a Verilog behavioral level model of the interface. This documentation will allow researchers to attach new transducers to the PEA modem.

Document PCMCIA Card - A detailed description of the PCMCIA card will be generated together with user interface code for one PDA. This documentation package will allow researchers to modify an existing software package to create a new application.

Protocol Area

Optical Orthogonal Code Study - We will explore various non-minimal OOCs for use in the inbound and outbound channels. We must generate these codes, and simulate their auto and cross correlation properties in a multiple BodyLAN environment.

Synchronization Code Study - We will study random assignment of BodyLAN identification codes versus codes that are more like OOCs in their cross correlation properties.

Beacon Chip Sequence Study - We will examine various beacon chip sequences for maximum tolerance to collision and ease of PEA oscillator phase locking. The benefits of different BodyLAN ID and control channel codes for the high error rate synchronization will also be examined.

Channel Modulation Study - The current plan has all RF pulses in a slot frequency modulated above or below the carrier frequency. This study explores alternative techniques such as modulating each pulse according to some coding paradigm with a goal to reduce the effect of narrow-band interferers and/or adjacent BodyLANs.

Synchronization Protocol Study - We know of several alternative synchronization procedures. These alternatives will be explored and compared to the proposed scheme.

Error Rate Analysis - We must develop channel error models when narrow band interferers and other BodyLANs are present to test our models against the prototype systems.

Prototype Area

Reference Oscillator - We must develop a phase lockable 32,768 Hz oscillator which has good short term stability in the absence of phase lock update signals. This oscillator must be capable of phase locking to the beacon frequency transitions which could be up to 30 ppm from the reference oscillator's center frequency. A low-power sine-wave-to-logic converter must be developed to create the 32,768 Hz clock needed to drive the modem controllers.

Local Oscillator - We must develop a local oscillator capable of switching between the inbound, outbound, and synchronization frequencies quickly. The LO must be phase locked to the 32,768 Hz timing reference.

Chip Oscillator - We must develop a fairly stable chip clock oscillator which is triggered off the rising edge of the 32,768 Hz clock. This oscillator must generate a logic-compatible clock signal and also be phase lockable to the reference clock.

Modem Receiver - We must develop a receiver section prototype composed of a low noise amplifier (LNA), mixer, BP filters, limiter and received signal strength indicator (RSSI), frequency discriminator, threshold generator, and comparators for the RSSI and frequency discriminator outputs.

Modem Transmitter - We must develop a transmitter section composed of frequency and amplitude modulators, loop antenna driver, and D/A transmit power selector. We will explore different circuits for fast power-up, power-down effectiveness using SPICE simulations.

PEA/PDA Controllers - We must develop a field programmable gate array (FPGA) version of the PEA and PDA modem controllers which will operate at 3 volts.

PCMCIA Card - We will develop the card incorporating the PDA modem, BodyLAN processor and its memory, and an interface to the PCMCIA bus.

BodyLAN Processor Firmware - We will develop the firmware executing on the BodyLAN processor to manage all initialization, channel communication, and synchronization activities.

Power-Saving Study - We will explore different circuits for fast power-up and power-down of the various BodyLAN components using SPICE simulations and models of a typical one micron BiCMOS process.

Evaluation Area

PDA Interface Software - We will develop the objects needed in the PDA to allow application development on the PDA. The first application will be the software needed for initialization and to test error rates over extended periods of time.

Sensor/Transducer Simulator - We will develop an EPLD which generates and sinks pseudo-random data sequences and interfaces to the PEA modem controller to test error rates.

Performance Evaluation Study - We will compare the theoretical and measured error rates under various conditions of narrow-band interferers and adjacent BodyLANs.

Power Consumption Study - We will verify that the modems can be implemented as a single BiCMOS chip and that the power consumption goals have some possibility of succeeding.

We propose to work with some university and/or other organization (with ARPA's concurrence) on the low power circuit design issues and on the problems of integrating transducers to a PEA modem. A companion research project (not included here) to create one or more of the transducer subsystems which would couple to the PEA modem would also make sense. A sensor subsystem to measure the earth's gravitational and magnetic fields to allow orientation input to the PDA has many promising applications.

Contractor Requirements

We would like the Government to furnish us with information about the bandwidth requirements of personal sensors (e.g., Corbino magnetic field sensors) being developed under other ARPA programs, so that we can investigate their compatibility with the BodyLAN architecture.

III. B. Results, Products, Transferable Technology, and Expected Technology Transfer Path

BodyLAN is an enabling technology that will open up many new application opportunities when it is coupled with various transducers, a wearable computer, and innovative software. The motivation to develop BodyLAN is thus primarily to enable creation of new and wonderful products. In this section, we discuss some preliminary ideas on BodyLAN usage.

Apple Computer's John Sculley has been promoting Apple's new computer, Newton, as the first of its kind of "personal digital assistant". Sculley heralds Newton as the start of the convergence of all information industries and asserts that this mega-industry will generate $3.5 trillion of sales in a decade. At that time, computer experts expect these personal digital assistants, or PDAs, to be as ubiquitous as wallets. They will integrate many of the services provided currently by telephones, radios, computers, faxes, and television and open up new applications for users in business, home, recreation, and education activities.

Initial PDA offerings from Sony, Apple, Sharp, IBM, and HP are relatively simple machines only loosely coupled to an embryonic information infrastructure. SRI International estimates that 2 million such devices were sold in 1991. Sales are expected to explode to 18 million by 1995. Experts suggest that the PDA promises to fundamentally change the way people interact with computers. PDAs potentially can sweep computers, consumer electronics, telecommunications, entertainment, publishing, and recreation into one industry that captures, processes, stores, displays, and transmits digital information.

While many people have computers, they are not ubiquitous. Computational and information retrieval resources are not available to us when we go for a walk, attend church, or even drive a car. Even with today's most advanced pen based PDAs, the user is confronted with the requirements of finding a place to work, physically opening and starting it, and then using a pen in an unfamiliar manner on an undersized display surface. One could not expect to interact with the information infrastructure while on the golf course, or at a party, or around the lunch table with fellow workers, or during daily household activities. The problem is that the user interacts with the current generation of small personnel computers unnaturally. PEAs could be the key to the solution.

We envision an environment whereby every person has a wide variety of ultra lightweight battery powered I/O devices worn on the body like jewelry, communicating to a PDA via wireless communications. The PDA would be carried in the pocket or purse or worn on the belt like today's pocket pagers. For services which could not be handled locally, the PDA would in turn communicate to the information infrastructure. The initial set of BodyLAN devices would be finger rings which sense earth's magnetic and gravitational field together with a sensor to detect acoustic pulses, wrist worn liquid-crystal displays, miniature digitizing microphones, and ear pieces for auditory feedback from the PDA. Sensors and output devices would be worn where it makes the most sense. Small, lightweight devices could be worn continuously much like today's rings and watches. Health sensors could be quickly attached to the body using Velcro straps and integrated into the body's local information infrastructure. Because the communications between sensor and PDA is wireless, these devices could be worn where needed, thereby not impairing freedom of motion.

This wireless capability would be useful to people who would like to interact with the information infrastructure without being tied to a keyboard/display or pen screen type device. The wireless intercommunications between ultra-small sensors and PDA will also open up brand new applications. Finger rings can be constructed to sense the earth's magnetic and gravitational fields and thus inform the PDA of the orientation of each finger. Pattern recognition software could then create a virtual keyboard or decode totally personalized sign language. These devices could also be used in conjunction with auditory feedback devices to form training aids in sports activities such as golf, tennis, and baseball. Medical applications include wireless sensors which monitor heart rate, blood pressure, respiration rate, body temperature, or alpha brain waves. All data would be captured and processed in real time and could be reported when patterns suggest medical attention is required. In the commercial world, this technology could be used to read, authenticate, and modify data contained in active identity badges or smart cards without the need to physically retrieve the card out of the person's wallet or purse.

Output devices include BodyLAN ear pieces for auditory feedback. Many people already wear ultra-low power display devices on their wrist, the common watch. Larger liquid crystal dot-matrix displays could be worn on the wrist to augment normal watch functions and the main PDA display for visual feedback such as telephone numbers, appointment information, account information, etc. When larger amounts of information are required and a work surface is available, the PDA itself could be brought out.

In the immediate future, we think that the wireless BodyLAN can become an important component of the Pathfinder system being developed at BBN under ARPA sponsorship. Pathfinder is a prototype personal communications system designed for military and police raiding applications. It is capable of accommodating a wide variety of specialized sensing equipment (audio, GPS receivers, health sensors, etc.). Pathfinder connects these sensors together using a wire-based communication system. The wireless BodyLAN proposed here could be used to replace this wire-based system.

Results

BodyLAN's key innovative results will include:

- Synchronization of PEAs to the hub within a temporal uncertainty of a few tens of nanoseconds. This allows the full range of time multiplexing and spread spectrum techniques to be applied to solve problems of bandwidth allocation, spatial reuse by multiple BodyLANs, and robustness against narrow band interferers.

- A procedure and protocol for parameterizing PEAs to an individual hub such that they may regain synchronization after sleeping even in the near-field presence of other active PDAs.

- The use of Optical Orthogonal Codes to reduce power consumption by almost an order of magnitude and still achieve spatial reuse.

- New analog and RF circuit designs which have very fast power-down and power-up times. New low-power oscillator and phase-locked-loop circuits.

- Adaptive power transmission protocols which cause the PEAs and PDA modem to minimize transmitted RF power.

- Support for both analog and digital communications using the same protocol.

- Randomization as a means of increasing temporal diversity and reducing worst case error probability.

- A protocol which allows non-licensed use of any frequency bands below 1 GHz in which the FCC allows intentional transmitters. By employing temporarily randomized RF pulses, the average radiated power of a PEA or hub modem can be brought under the maximum radiated power allowed and still allow communication over short distances.

- Adaptive circuit techniques which bias the RF circuits at less current than normal worst-case design techniques. These technique typically reduce power consumption by a factor of three over conventional worst-case designs.

- Interface standards which are vendor and device independent (an open architecture).

- A new synchronization protocol based on a derivative of Optically Orthogonal Codes which allows collisions of synchronization beacons between multiple BodyLANs but minimizes their probability.

These developments will provide a new capability. While the BodyLAN technology itself will not fundamentally change the way people interact with computers and the information infrastructure, BodyLAN is one part of the triad of PEAs, PDA, and application programs which will. If successful, a whole new industry may emerge.

Products and Transferable Technology

We will provide an analysis, develop a prototype, and evaluate a new wireless body local area network. Our products and transferable technology include:

- A document describing in detail the BodyLAN™ architecture, its limitations, and the FCC restrictions (if any).
- A specification describing interfacing to the PEA modem, the PDA modem, and the PDA of choice.
- A mathematical analysis of the Optically Orthogonal Codes used for the main data transfer link and different synchronization protocols. This analysis will explore the effects of various parameters such as narrowband interference power, multiple BodyLAN space sharing, and modulation diversity on error rates, synchronization acquisition probability, and power consumption.
- A set of eight PEA modems, three PDA modems, an interface to some PDA, and a data pattern generator/checker. These prototypes will be constructed using only existing RF and telecommunications chips, field programmable logic devices, and surface mounted discrete components on small PC boards. These prototypes will not attain the potential small size and low power consumption, but will demonstrate the BodyLAN architecture and concept of operation.
- Software on the PDA interface needed to compare the hardware performance with theoretical models.
- An evaluation of the architecture to verify the robustness of the architecture and its theoretical performance.

Expected Technology Transfer Path

We intend to influence the Personal Digital Assistants (PDA) industry by encouraging vendors to adopt the BodyLAN architecture and by helping to develop significant applications of the technology. We will proceed by presenting papers and joining recently formed industry groups. Key industry groups that we expect to influence and get direction from are the PCMCIA (Personal Computer Memory Card Industry Association) and the newly formed company, General Magic Inc., backed by Motorola, Sony, and Apple.

We also intend to further the development of the BodyLAN hardware after this proof of concept. We hope to enlist the aid of an ARPA-approved source for the final miniaturization, or to interest an industry leader with the means to provide the resources for the final miniaturization.

Both of these efforts are out of scope of this proposal, and BBN intends to pursue these issues with internal funding in the interest of spreading the technology and creating new business for BBN.

III. C. Detailed Technical Rationale

This section provides a more detailed discussion of the technical rationale behind our proposed effort, enhancing the discussion in Section II.D.

Technical Rationale

To any engineer who has experience in RF designs, sending a signal a few meters is fairly straightforward. A 1-turn coil, 15 millimeters in diameter, having a 400 MHz 20 milliampere sinusoidal current, generates an electric field of 2500 microvolts per meter at three meters distance. A receiver dipole of length 20 millimeters generates a voltage of 132 microvolts at that field strength, or 435 times that required by a low cost receiver. When antenna sizes are very small, higher frequency is a big win because of the cubic dependency of signal strength on frequency. At 1200 MHz, the same configuration would result in a signal 27 times as large. The question is, "if it's so easy, why hasn't someone already done it?".

The answer to this question is that technology heretofore did not provide the motivation to do this engineering. With the emergence of wearable computers, wireless communications, and low cost, high frequency, high density semiconductor chips, we now can investigate the practicality of a very-local-area, wireless network, the BodyLAN.

The radio frequency spectrum is crowded and highly regulated. More than 30,000 channels are licensed by the FCC just in the Northeastern part of the United States (under 1000 MHz). With the exception of the television bands, all these channels are narrow band FM. While the number of channels is very large, they are infrequently used. Only the FM radio, TV, and cellular radio bands are in constant use. Forty percent of the spectrum under 1000 MHz is dedicated to television. Of the 67 TV bands, only about 16-18 are typically occupied. Fire, police, amateur radio, and other bands are even less frequently utilized. One of the widest bands, the military aircraft bands (200-400 MHz) is also the least utilized. This is not surprising given the paucity of military flights over urban areas.

For BodyLAN, we need to find a way to coexist with these licensed channels in such a way that the FCC will accept unlicensed BodyLAN emitters and existing licensees will not object. FCC Regulations Part 15.209 specifies 15 bands under 1000 MHz in which unlicensed emission can be intentional but of limited field strengths. Typical field strength maximums are 100 to 200 microvolts per meter at three meters. For the remaining bands (all the television bands for example), the FCC prohibits intentional emissions.

For long distance transmissions, narrowband FM benefits both receiver and transmitter - hence its popularity. The receiver benefits from the narrow band because it receives less noise from natural and man-made noise sources and only the licensee is allowed to transmit power in that band. Since a transmitter's cost is normally highly dependent on its peak power, sending continuously (i.e. narrow band) maximizes the energy per unit of information transmitted. Narrow band transmission incidentally maximizes the number of channels. This maximization of precious radio spectrum is one of the most important benefits of narrow band transmission.

For short distance transmissions, as in BodyLAN, the benefits of narrow band FM disappear. In any narrow band, the receiver may find interfering signals from narrow-band transmitters and from other BodyLANs. A BodyLAN transmitter receives no cost reduction benefits from narrow-band operation because of the severe FCC limits on transmitted power. Accordingly, a new mode of operation now becomes desirable: pulsed operation (i.e. wideband), and, as described below, using a combination of AM and FM.

An emitter having a maximum field emission of 20,000 microvolts per meter pulsed one microsecond on and 99 microseconds off has an average field strength of 200 microvolts per meter. If a wideband receiver is synchronized to the transmitter and only samples the received signal when the transmitter is sending, then it "sees" a 20,000 microvolts per meter field, not the 200 microvolts per meter average. A narrowband interferer ten kilometers away would need to radiate 1.3 kilowatts to equal this signal strength.

If two adjacent BodyLANs each employ the same pulsed transmission scheme, normal operation will result in periods where both are exactly synchronized and thus give unacceptable error rates. This occurs because the two BodyLANs are not perfectly synchronized. Pulses from the two BodyLANs will eventually collide with one another even with only slight frequency differences. These pulse collisions, would give rise to an error behavior where the errors are all grouped together and could persist for long periods of time. Even worse, for lower duty cycles and/or more BodyLANs, the error probability and the persistence of error groups will increase. This unacceptable operation is mitigated by the "FM capture effect". In this effect, a receiver totally "captures" the transmitter which is sending out maximum field strength.

Thus simply periodically sending pulses from each BodyLAN has significant drawbacks: 1) the inability to control the error rate, 2) the possibility of long periods of high error rate, 3) the poor performance in crowded (many BodyLANs) conditions, and 4) the possibility of a receiver capturing another BodyLAN's private information. Pulsed operation combined with temporal diversity potentially solves this problem at the expense of higher complexity.

An important advantage of short distance communications is comparative ease of synchronization. Maximum PEA/PDA separation distance is expected to be less than 1.4 meters (55 inches) for a hip-worn PDA. This corresponds to less than 10 nsec of temporal uncertainty for a PEA anywhere within the 2.8 meter diameter sphere surrounding the PDA. If the RF pulses are on the order of 500 nanoseconds, none of the complexity associated with ranging must be implemented. In long distance communications, say 10 kilometers, the temporal uncertainty is 7,000 times larger. This requires either the data rates be kept unacceptably low or ranging compensation be incorporated.

Pulsed operation is desirable from a power conservation standpoint because transistors need large bias currents to obtain high gain and high frequency operation. By employing fast startup linear circuits operating at low duty cycles, low power consumption is obtained. For example, a CMOS state-of-the-art 1000 MHz divide by 128 prescaler consumes 900 microwatts continuously but would consume only 9 microwatts when used at a 1% duty cycle.

Power consumption is an issue critical to the success of BodyLAN applications. A non-rechargeable battery suitably small to be useful, also has low energy storage. For example, a standard lithium-manganese three volt battery has an energy storage of approximately 50 milliamp hours. If a PEA consumes 100 microamps (i.e. 300 microwatts), its battery will last only 20 days. Contrast this to a watch which has an expected battery life of more than five years. Although they have lower energy storage, rechargeable batteries are potentially an answer. A comparable rechargeable lithium-hydride battery can provide 20 milliamp hours. Assuming a 18 hours of use per day (6 hours for charging) allows a power budget of 3,300 microwatts.

Synchronization between PEAs and the PDA is clearly the key to the entire BodyLAN concept. It is also the most challenging protocol problem to be solved. Principal requirements of a synchronization protocol are low power consumption, low complexity, the ability to quickly reacquire synchronization after losing synchronization without disturbing other PEA/PDA communications, and single receiver design in the PEA modem. From a power consumption standpoint, the PDA can expend only a small amount of its power consumption and transmitted power budget on synchronization. This suggests that the PDA broadcast a low duty cycle beacon at a rate just sufficient to keep the PEA's local oscillator in synchronization.

With synchronization such an important part of BodyLAN, we envision using a separate frequency band exclusively for the broadcast of synchronization beacons. Since this synchronization band is shared, beacons from adjacent BodyLANs will interfere with one another. A PEA in one BodyLAN can actually receive a beacon from another PDA having a signal strength greater than from its own PDA, so signal strength alone is insufficient to determine the home PDA. Also, PDAs cannot detect a beacon collision at all the PEA sites. A PEA must therefore must be able to acquire synchronization in the presence of collisions from on adjacent PDA. Moreover, it must acquire synchronization even when the beacons from foreign PDAs have larger signal strength than those from its home PDA. This rules out collision avoidance protocols which require collision detection.

There are several operational constraints in the use of PEAs which critically affect the architecture and protocols. The first and foremost is that PEAs employing BodyLAN modems be autonomous. A PEA owner must only be aware of two constraints: first, PEA batteries become discharged and must be replaced or recharged, and second, PEAs must be in reasonable proximity to the home PDA. All other aspects such as synchronization, power management, initialization, error reporting, synchronization sequence changeover, etc., must be handled by the Finite State Machines in the PEAs and PDA. Since PEAs are intended to be very small, they do not have a keyboard, connectors, nor any other mechanism for conveying information to the PEA other than through BodyLAN. We assume even the initialization procedure which sets the PEA's personalization perameters is handled via the BodyLAN.

PEAs have three operating states: dead, sleep, and active. In its dead state, a PEA's internal control registers contain uninitialized data. This will be the normal state following a change of batteries if no electrically erasable ROM is provided. The PEA must be able to transition from the dead to active state with the smallest amount of user help. In this case, the user will only need to bring the dead PEA close to the PDA and start the PDA's initialization sequence. No further user intervention should be required. In its sleep state, a PEA's internal control registers have been loaded but it is unsynchronized with the PDA. This will be the normal state following turning the PDA off for the night or for PDA recharging. We expect no user intervention for a sleeping PEA to transition to its active state. Because of severe interference, a PEA could also inadvertently transition from active to sleep by losing synchronization. We expect the PEA to automatically reacquire synchronization and to do so within a few seconds.

In use, PEAs of one BodyLAN must share the same physical volume of adjacent BodyLANs. We require that adjacent BodyLANs not interfere with one another catastrophically but will allow some increase in error rate. In normal operation, the PDA will monitor the received power level and error rates. It adjusts the transmitted power levels of itself and the PEAs to achieve the desired error rate. Thus PEAs close to the PDA would transmit at lower power levels than PEAs further away from the PDA. This power management tends to limit the effect of one BodyLAN on another. Moreover, the "FM Capture Effect" causes a receiver to completely "capture" the stronger of two FM signal having the same carrier frequency. This effect will also reduce the interference of adjacent BodyLANs.

Since the PDA broadcasts synchronization beacons to all its PEAs, it must transmit them at a large enough power to guarantee that the farthest PEA has sufficient signal to noise ratio to achieve synchronization. If the PDA only transmits beacons at the minimum power to achieve synchronization a potential problem occurs. Assume a PDA only transmits beacons at the minimum power needed to keep its farthest PEA in the active mode. Assume now a sleeping PEA is physically brought close to the PDA but is kept farther away than the farthest active PEA. The sleeping PEA never becomes active. We require the synchronization protocol to be robust to these types of power management problems.

Far field strength drops off only inversely proportional to the PEA/PDA separation distance. Thus with power management, a PEA at its maximum distance from its home PDA (thus transmitting maximum power) also creates maximum interference with adjacent BodyLANs. Consider the case of two students in a 20' x 20' classroom. Student A in the center of the room raises his hand on which he has ring finger PEA(A). PEA(A) to PDA(A) separation distance is about 1.4 meters. Student B is seated just 10 feet away. PEA(A) to PDA(B) separation distance is about 3.3 meters. The received signal at PDA(B) from PEA(A) is just 58% smaller than that received from PEA(B). In a classroom, party, or meeting environment, a target PDA could be receiving pulses from 10-20 foreign PEAs which are of comparable power to that sourced by its own PEAs. The FM Capture Effect will reduce the interference somewhat, but multi-path fading, non-isotropic antenna radiation patterns, and power measurement uncertainty will still result in 10 or so foreign PEAs being captured by a target PDA.

For some geometries, the FM Capture Effect will work against us. Consider the case of BodyLAN equipped persons A and B shaking hands with one another. If person A has a finger-ring PEA(A) on his outstretched hand, it would probably be closer to PDA(B) than say person B's PEA(B) ear microphone. This requires that the transmission protocol must allow a relatively large number of interfering BodyLANs and still maintain a prescribed error rate.

Payoff of the Proposed Work

The BodyLAN architecture can integrate the results of multiple ARPA projects which are developing electronic subsystems having low power, small size and light weight. The result will be a personal information system which ushers in a new era of constant personal interaction with resources worldwide.

III. D. Detailed Technical Approach

This section provides a more detailed discussion of our technical approach , enhancing the discussion in Section 2.D.

Figure 2 illustrates the BodyLAN system. The architecture relegates transducer functions to PEAs and processing functions to the PDA. A PCMCIA card implementing the BodyLAN hub modem plugs into the user's PDA. Control of the BodyLAN is implemented in a low-power processor residing on this PCMCIA card. Applications interacting with the ensemble of PEAs are executed on the PDA.

The BodyLAN architecture calls for three frequency bands. Two bands, at 346.03 MHz and 387.97 MHz are used for application data and we label them the inbound channel and outbound channel respectively. The PDA transmits in the outbound channel and receives from the inbound channel. The third band at 367.0 MHz is the synchronization channel and is used exclusively by the PDA to transmit a synchronization beacon to its PEAs together with some control data. These bands were chosen to comply with the FCC regulations.

BodyLAN has a star topology where PEA modems communicate only with the PDA modem. PEAs operate as half duplex devices. Further, they do not receive simultaneously on the outbound channel and the synchronization channel. The PDA operates as a full duplex device, except that it does not transmit or receive application data when sending the synchronization beacons. This simplifies reception at the PEAs and is not an obstacle since no PEA should transmit or receive while its PDA is transmitting a synchronization beacon.

Multiuser interference among adjacent BodyLANs and narrow-band interferers are expected to be the main source of channel errors. Naturally occurring noise from the environment (i.e. from auto ignitions, electric motors, transmission lines, etc.) and thermally generated noise acting alone are expected to be insignificant sources of channel errors. Our design uses spread spectrum communication with 64 chips per bit and Optically Orthogonal Codes (OOC) to combat these error sources. The combination of spread spectrum and OOCs not only reduces the error rate but also make it easy for us to meet FCC regulations and reduce power consumption.

Standardization

As illustrated in Figure 2, BodyLAN is composed of a PCMCIA card on which the BodyLAN control processor and the PDA modem are mounted, and several PEA modems integrated with their sensor/actuators. Firmware in the control processor will control all BodyLAN communication activities such as power management, initialization, error detection, and synchronization. Application code exclusively executes on the PDA's processor.

We envision the PDA component of BodyLAN as a generic component implemented on a PCMCIA card. This card would plug in to a PDA of the user's choosing. It contains the PDA modem, a control processor with memory, and an interface to the PCMCIA bus. Processing power of the control processor is sized only to execute the communications activities of BodyLAN. It will process the data input from all PEAs, plus any external or application data fed to the PDA but not any transducer-specific functionality. Thus standardization of the PDA component appears achievable. The diversity of PEA form factors and transducers will make standardization of the PEA component more difficult.

For the PEA component, we envision standardizing only the PEA modem portion of the PEA. To achieve some measure of standardization we propose the interface between PEA modem and transducer as a full duplex serial communication with clock and a frame pulse sourced by the PEA modem. In addition, a low-data-rate, full-duplex overhead channel will also be provided to provide a communication path with the PDA processor.

Communication Channels

The choice of spectrum window must take into account naturally occurring noise, man-made noise, and FCC regulations. The 335 MHz to 400 MHz band, among others, is assigned to military aircraft. Other transmissions in this band are allowed as long as they do not exceed 200 microvolts per meter at a distance of three meters, as measured by a quasi-peak detector. Since this detector has low pass filter properties (contrary to what its name implies), our spread spectrum signals make it easy to meet FCC regulations. Aircraft transmissions, when they occur, are narrow band interferers.

We expect the two major sources of channel errors to be multiuser interference among adjacent BodyLANs and narrow-band interferers. For multiuser interference, we have chosen spread spectrum signals known as Optical Orthogonal Codes. To reduce the effect of narrow band jamming, the RF pulses are transmitted at either of two frequency tones. The tones are one MHz above and below the center frequency of the band. Thus, the combined spread spectrum signal with a two MHz chip rate occupies approximately 4 MHz of spectrum.

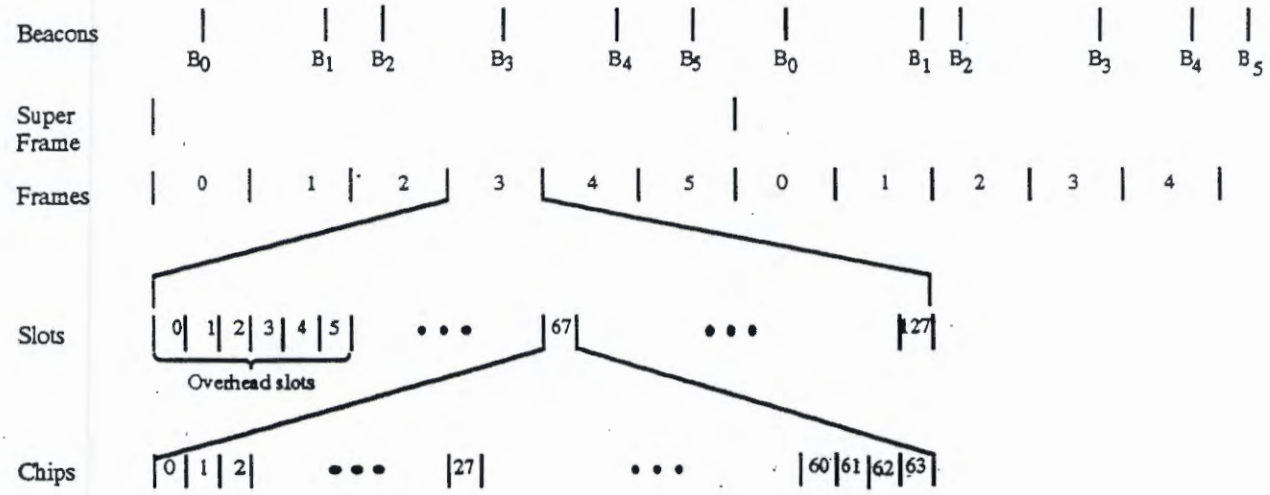

Figure 4. Body-LAN Transmission Hierarchy
Showing Superframe, Frame, Slots and Chips

BodyLAN's hierarchy of signals is shown in Figure 4. The figure shows the TDMA format with 6 frames per superframe, 128 slots per frame, one bit per slot, and 64 spread spectrum chips per bit. Six synchronization beacons are positioned among 768 slots repeated each superframe. The locations of these six beacons within a superframe form a codeword unique to each BodyLAN. Slots zero through five are dedicated to overhead channels between PDA and PEA modems. Power is transmitted in less than 10% of the chip periods. The locations in which power is transmitted form an Optically Orthogonal Code.

Spatial Coexistence Among Adjacent BodyLANs

BodyLAN must operate within range of other BodyLANs. Our design uses spread spectrum transmissions to provide near-orthogonality among signals from adjacent BodyLANs. We have chosen a form of pulse position spread spectrum signal known as Optical Orthogonal Codes (OOCs). OOCs are pulse patterns designed to have low cross-correlation among themselves (i.e. few pulse positions overlap for any shift of the codewords). Hence they are unipolar signals, i.e. mostly zeros with a few ones. and use a sparse number of pulses in their spread spectrum chip sequence. Normally, OOCs are detected using energy detection.

Because energy detection has numerous problems in an RF transmission environment, we have modified the application of OOCs in two ways. First, positions corresponding to a one in the code transmit energy regardless of whether a one or zero is to be sent. Second, the information is sent using frequency shift keying. If the frequency is above the center frequency for the majority of the pulses, it assumed that a one was transmitted, and if the frequency is below the center frequency for the majority of the pulses, a zero was transmitted. By encoding the information in the zero crossings of the RF energy, a much simpler, wide-bandwidth receiver can be designed. This new application of Optically Orthogonal Codes neatly fits within the constraints imposed by available receiver chip technology.

Choosing an OOC for BodyLAN is still an open issue. One problem with optimum OOCs is that they yield a high error rate due to too few codewords. Ideally, we would like to assign a unique code word to each BodyLAN. Unfortunately, the number of codewords in an optimum Optically Orthogonal Codes is typically very small. In the optimum (63, 3, 1) code, there are only 10 out of 1.84e19 possible codewords. An optimum (63, 5, 1) code has even fewer codewords. Increasing the correlation factor to two (i.e. any two code words can have two coincident pulses for an arbitrary shift) greatly increases the number of codewords but still results in far fewer codewords than possible users. Thus it will not be possible to assign each BodyLAN a unique codeword.

Given the small number of codewords, it is possible for two BodyLAN to be in exact synchronization. If they both used the same codeword and the effects of FM capture effect are neglected, an unacceptable error rate results. What is required is more diversity in the selection of codewords. One alternative has each modem choose one codeword and a phase within the slot of each frame based on 9-bits from a pseudo-random sequence generator. Now if two BodyLANs are exactly synchronized during one frame, their probability of being exactly synchronized in the next frame is 0.002 and their probability of being exactly synchronized in the next frame after that is 3.81E-6.

Multiple BodyLAN errors occur because two or more BodyLAN transmitters are using the same codeword and have pulses which overlap by more than 50% or when three or more transmitters using different codewords share more than a majority of pulses which overlap. For an optimum code, the first error term dominates because there are few codewords. For example, the probability that two independent BodyLANs will not be sending the same data, will be synchronized within one chip time, and will be using the same codeword is about 0.1%. When ten BodyLANs are considered, the error rate increases to about 1%.

For higher order OOCs such as a (63, 7, 3), the number of codewords grows dramatically, thereby lowering the probability of overlapped same codeword usage, but now the second error term increases because of the increased number of pulses. OOCs such as a (63, 9, 3) have an even larger number of codewords and require at least two overlapping pulses from other adjacent BodyLANs to produce an error. These codes

potentially offer even lower error rates. One of the first research tasks will be to explore various OOCs to minimize error probability for a given number of adjacent BodyLANs.

Synchronization

Synchronizing PEAs to the PDA is accomplished by the PDA broadcasting beacons on a separate frequency band. Six beacons are transmitted in each 768-slot superframe, one in each frame but normally in different positions within each of the six successive frames. Each beacon is a 64-chip sequence using Frequency Shift Keying (FSK). Thus unlike the inbound and outbound signals which are FSK bursts one chip in duration, beacons are FSK bursts of 64-chip duration. The relatively long length of the beacons allows the receiver to use its low-bandwidth Received Signal Strength Indication (RSSI) output to determine if RF energy is present or not. Each beacon will be composed of a chip sequence which is common to all beacons to assist in phase locking, a sequence which is unique to the particular BodyLAN, and a control channel. Since beacon collisions with adjacent BodyLANs are considered to be frequent, the control channel error rate is assumed to be high. Accordingly a high error rate code is employed in the control channel.

Each PEA contains an oscillator based on an a common watch crystal oscillating at 32,768 Hz. A non-premium watch crystal typically has a relatively poor +/-30 ppm initial frequency tolerance. Over a few seconds of time period however, oscillators constructed from these watch crystals have remarkable stability. We expect the stability to be better than +/-3E-7 over a time period of a few seconds. We therefor expect a PEA to not gain or lose more than 25% of a chip time in 400 milliseconds (i.e. 100 frames). Thus, once a PEA has phase locked its oscillator to the PDA's oscillator, it is very tolerant to missing beacon reception errors. The challenge is to establish synchronization in the presence of noise, jamming, and especially other BodyLANs.

Each BodyLAN receiver is assumed to have a relatively high frequency FSK detector and an RSSI output having a bandwidth about 0.05-0.1 that of the frequency discriminator. Beacons thus appear as six or more blips on the RSSI signal repeated each superframe. When adjacent BodyLANs are present, the RSSI signal could have 100-200 blips each superframe.

The first synchronization task is to establish the base RSSI signal caused by narrow-band interferers. RSSI signal levels above this base are assumed to be sourced from either the home PDA or adjacent BodyLAN PDAs. A search procedure is then initiated by assuming the first beacon is the first superframe beacon from the home PDA. Each BodyLAN is assigned a unique set of six beacon positions within the superframe. These positions form a high correlation (767, 6, 4) OOC. If five subsequent beacons occur in the correct positions relative to the assumed first superframe beacon, the beacon set is assumed to be a candidate for fine synchronization. Coarse synchronization typically only takes the duration of one superframe (i.e. 23.4 milliseconds) since a PEA can process all six combinations in parallel.

After coarse synchronization, the PEA locks onto the first part of the beacon which is common to all beacons. This chip pattern consists of 16-chips above the center frequency followed by 16-chips below the center frequency. The frequency transition marks beginning of a chip period. If more than one frequency transition occurs between the fourth and 28th chip periods, the beacon is assumed to have collided with a foreign beacon and the transition is ignored. If it is the only transition, the transition is used to phase lock the 32,768 Hz oscillator.

Once fine-level synchronization is established, the PEA examines the remaining chip positions to determine if the beacons are being sourced from the home PDA or from a foreign PDA. If the beacon identification code does not match that of the home PDA, the PEA repeats the entire process starting its coarse synchronization from the first beacon after the beacon which started the last coarse synchronization. If coarse synchronization does not occur after searching through at least two frames, the PEA enters a sleep phase for 2 to 4 seconds and repeats the synchronization process. With sparse synchronization codes, the probability of generating a false coarse synchronization is very small.

To simplify the PEA design, we require that no inbound nor outbound channel information be transmitted during the slots in which the beacon is transmitted. To remove any loss of channel bandwidth, slot two is assigned as the beacon alternative slot. Thus if a PEA has been assigned to receive a bit during slot N for a particular frame and a beacon is also to be received in slot N, the bit is instead transmitted and received in slot two. To reduce the problem of local oscillator frequency switch over, we will likely assign two contiguous slots for the beacon, thereby allowing 16 microseconds for the local oscillator frequency switch on either side of the beacon.

Analysis of Alternative Approaches

We have examined short range communications using acoustic, infrared, and RF. Acoustic communications have the problem of very low bandwidth except when a higher frequency carrier is employed. While it is fairly easy to generate a multi-megahertz acoustic wave, its very short wavelength of about 100-200 microns causes many problems including very high absorption by clothing. Infrared signaling has high bandwidth but requires either line of sight or external surfaces to reflect the energy. RF signaling has to comply with FCC regulations but is otherwise a well matched to a single low cost silicon implementation with very few additional components.

We plan on transmitting RF bursts rather than use standard coherent spread spectrum signals for three main reasons: it simplifies the receiver design, it substantially reduces power consumption, and its performance is less sensitive to transmitter-receiver distance. Although the choice of a codeword set for the inbound and outbound channels is still open, the limited code size will continue to be problem. Another alternative being considered is to is to change codeword and codeword phase only in response to a high error rate. Here, the PDA informs each PEA of the codeword to be used. The codeword is then used typically for a significant period of time before a collision with another BodyLAN assigned the same codeword occurs. When the collision increases the error rate, a random hop to another code word would take place either by one or by both BodyLANs.

We have also explored several alternative synchronization schemes. There are so many alternatives, one must set up an alternative tree to keep them all straight. One alternative synchronization scheme worth mentioning uses an OOCs for the beacon positions within the superframe having only a small number of codewords. In this scheme, when another BodyLAN, using the same code, drifts into exact alignment, each BodyLAN will jump to a new codeword. We can easily give a unique sequence of codewords to each BodyLAN.

III. E. Other Developments in This Area

Commercial Off-the-Shelf (COTS) Products

Personal Digital Assistants (PDAs)

Apple Computer has announced its Newton PDA, in three models which range from $699 to $1250. The top two models will have a PCMCIA compatible radio modem to provide access to a nearby AppleLink port.

Hewlett Packard has announced its OmniBook 300 with an infrared communications link for $2000. This is a 2.2 pound PDA with a full-sized keyboard.

AT&T has announced its Personal communicator, which functions as a computer, phone, and fax. This is a pen and notepad unit based on the AT&T Hobbit chip.

General Magic Inc. is a spin-off of Apple Computer with investment from AT&T, Motorola, Philips, Sony, and Matsushita. They are producing an operating system for PDAs called Magic Cap, which provides a highly intuitive graphical user intuitive graphical user interface.

The PCMCIA Standard Interface

The Personal Computer Memory Card International Association (PCMCIA) has established standard specifications for credit-card-sized microcomputer add-on memories and peripherals. The cards are 54 mm wide by 85.6 mm long (2.1 by 3.4 inches) and have a 68 pin interface. Type I, Type II, and Type III cards are 3.3 mm thick, 5 mm thick, and 10.5 mm thick respectively.

This represents the current state of the art in microcomputer miniaturization, and many mainstream PCMCIA products (faxes, discs, RF modems, Ethernet adapters, static RAM, and flash memory) are now entering the market. Most notebook products now have one or more PCMCIA slots.

License-free Wireless Networks Compliant with FCC Regulations Part 15.247

A number of vendors are offering wireless LAN products which comply with FCC Part 15 regulations for unlicensed operation given in the Code of Federal Regulations Title 47 Part 15.247. These regulations for wireless LANs require the use of subwatt power and spread spectrum signaling within the three Industrial, Scientific and Medical (ISM) bands to minimize co-channel interference.

Motorola has unveiled Mobile Networks Integration technology, software that unites disparate wired and wireless networks. The technology, previously code-named Monet, will let users send messages from anywhere in the nation, regardless of which network they are connected to.

PCMCIA cards for wireless communications

A number of vendors are providing PCMCIA cards which are radio modems capable of providing a wireless link at distances up to 50 meters. Examples include Toshiba's Wireless Portable Work group product and Spectrix Corp's SpectrixLite LAN product,

with a $350 serial port and a $3K ISA network card. IBM Network Systems division offers its Wireless RF LAN card for $800. IBM Canada has its Infrared Personal Area Network (PAN) adapter card for $300, which supports communications within a 10 meter square room. Both the Wireless RF LAN and the Infrared PAN operate at speeds up to 1 Mbit/sec.

Relationship to BodyLAN

BodyLAN is complementary to all the COTS technologies above, and in fact is highly synergistic to most of them. For example, we will use a COTS PDA as the central component of the body constellation of personal electronic accessories (PEAs). We will use a standard PCMCIA interface card to interface the BodyLAN to the PDA.

The COTS wireless LAN products provide connectivity from a person to his local communications infrastructure, using credit-card sized modems and subwatt power to reach over tens of meters in compliance with FCC Regulations Section 15.247. In contrast, the BodyLAN will eventually be implemented as fingernail-sized modems operating at microwatt power level to provide connectivity over a meter of personal body size, and operating under FCC Regulations Section 15.209.

The BodyLAN will serve as a seamless extension of the wireless LAN, providing connectivity from a person's PEAs (e.g., health monitors) to the global communications infrastructure.

Advantages and Disadvantages of this Approach

The advantages of this approach include:

- Interface standards which are vendor and device independent (an open architecture).
- Minimal power consumption, ultra small size and weight, and no requirements for user intervention.
- A protocol which allows non-licensed use of any frequency bands below 1 GHz in which the FCC allows intentional transmitters. By employing temporarily randomized RF pulses, the average radiated power of a PEA or hub modem can be brought under the maximum radiated power allowed and still allow communication over short distances.
- Synchronization to the hub within a few tens of nanoseconds, supporting the full range of time multiplexing and spread spectrum techniques. These techniques solve the problems of bandwidth allocation, spatial reuse by multiple BodyLANs, and robustness against narrow band interferers.
- The use of Optical Orthogonal Codes to reduce power consumption by almost an order of magnitude and still achieve spatial reuse.
- Adaptive power transmission protocols which cause the PEAs and PDA modem to minimize transmitted RF power.
- Randomization as a means of increasing temporal diversity and reducing worst case error probability.

The disadvantage of this approach is that it is an innovative and advanced approach to solving these communications problems, and it requires a phase of research and development to prove the concept and demonstrate a working prototype BodyLAN. Of course, ARPA's charter is to conduct this kind of high leverage, high payoff R&D that can lead to the creation of new national industries.

III. F. BBN's Previous Accomplishments in this Research Area

BBN's BodyLAN™ IR&D Project

The concepts included in this proposal abstract have resulted from internally funded BBN research. A small IR&D project was initiated in 1991 which focused on basic requirements for BodyLAN, problems to be solved, and architectural aspects of short range wireless communications. Communication data rates needed and obtainable, error rates, multiple BodyLAN issues and the selection of acoustic, optical or electromagnetic radiation as the carrier of choice were examined.

A follow-on project was initiated in 1992 to concentrate on the practical issues, especially the synchronization problem. This work is not yet completed. Work so far has progressed on RF circuits for the transmitter, receiver, local oscillator, and phase locked loop and a synchronization protocol. A consistent BodyLAN architecture has been developed, although only the high level details have been described here. An internal BBN report describing the BodyLAN IR&D research effort will be available in July 1993.

We consider the proposed work to be exploratory development. Synchronization between PEA and PDA is clearly the key problem to be solved. We have a plan for synchronization (explained briefly here) which shows promise of working but has not been demonstrated. Alternative synchronization schemes have been proposed but not examined in detail because of limited funding resources. All the synchronization aspects of BodyLAN must be considered to be in the research arena. To our knowledge, continuous operation versions of the circuits which will be needed in BodyLAN have been public knowledge for decades. If power consumption were not a goal, creating a BodyLAN prototype would be considered pure development. Creating equivalent functionality circuits for pulsed operation will require invention. Since one of our goals is to demonstrate the feasibility of BodyLAN power reduction techniques, some circuit design research will be required.

BBN has also had extensive experience developing network protocols to carry real-time traffic such as voice, video or distributed interactive simulation. BBN has been a leading participant in the groups that have specified these real-time networking protocols, (e.g., Internet Stream Protocol ST-2), and has developed implementations of these real-time protocols in several networks such as the Wideband Satellite Network, the Defense Simulation Internet, and DARTNET.

Hardware Design, Development and Integration

BBN Systems and Technologies has a long history of developing hardware systems, ranging from the early Pluribus and ARPANET IMP's to next generation communication processors and sophisticated data acquisition gear. Recent projects include the following systems:

- T/20, a highly integrated communications processor
- Emerald, BBN CD's next generation ATM cell switch
- KG interfaces to the T/20 communication processor
- AVR, a data acquisition and control system
- High speed, SONET OC-3 long link emulator.

- NUWC Torpedo emulator
- VME-based Hydrophone Sampling Unit (analog data acquisition)
- VME-based speech vocoder
- Digital terminal for NASA ACTS Gigabit Satellite Network supporting OC-3 and OC-12 SONET.

Our staff of ten designers has experience in board level digital design using TTL, CMOS, and ECL technologies. Our group has designed many ASICs ranging in complexity from PALs to field programmable gate arrays to hard gate arrays to full custom VLSI. We own CAD tools to support board level design, PAL development, and the design of FPGAs. The design group is augmented with a complete printed circuit CAD group as well as mechanical design services.

Pathfinder Project

BBN is developing a personal communications system architecture based upon emerging technology in microsystems, radio networks, and packaging. The system, called Pathfinder, enhances communications, coordination, and navigation of military and police raiding teams.

During a mission, each team member will carry a compact, modular, low-power computer system with a small visual display and a variety of mission-specific sensors and actuators interlinked by a self-configuring, wired, local-area network called BodyLAN. A typical mission system might be composed of a computer, a Global Positioning System (GPS) receiver, and a packet radio. The radio will not only provide team communications, but will link each member to command posts remote from the mission site.

This system provides many capabilities for members of the raiding team. While preparing for a mission, the team leader can monitor the positions of his team members on a mapping display. The leader then will know when his team is in position without having to check in audibly with each member. During the mission itself, command and medical personnel can monitor the positions and health of each team member and can send help to those in trouble. During rendezvous and withdrawal from the target, the positions and status of the team can be monitored and decisions can be made according to their progress without distracting the team members from their mission.

The Pathfinder system uses an open architecture to implement the hardware and software protocols. By adopting a modular approach to the mission system hardware and software, we can include or exclude capabilities according to the mission. For example, by combining just the computer, packet radio, and microphone units, we can create a small listening device that can be dropped anywhere in the target area and monitored by the team. Similarly, we can build a small tracking system by combining just the computer, packet radio, and GPS modules. We can also add totally new devices to the network because the network protocol is similarly open and modular. For example, compressed-video surveillance devices could be added to the net as video compression technology improves in terms of power consumption and bandwidth.

The Pathfinder system significantly increases the amount and timeliness of mission-relevant information available both to individual team members and to team leaders. This capability may redefine command organization and information flow and may result in entirely new requirements for operational planning and execution procedures.

Semi - Custom VLSI Development

BBN's Emerald ATM cell switch project is developing four large CMOS gate arrays using state-of-the-art tools and methodologies. Each of the arrays is approximately 70,000 gates in size, and includes embedded RAMs, embedded controllers, complex state machines, and external memory interfaces. The arrays are being implemented using logic synthesis (Synopsys) and are currently being functionally verified using full chip and system-level simulation (Verilog).

Software project techniques are being employed to ensure the integrity of the verification effort. These include a revision control system and an automated regression framework.

Previous to the Emerald project, BBN successfully developed a 20,000-gate CMOS device as well as several semi-custom ECL devices.

BBN Protocol Standards Activities

BBN Systems and Technologies assisted the NIST Institute for Computer Sciences and Technology (ICST) in the development of protocol standards for most of the layers of the Reference Model (Network, Transport, Session, Presentation, File Transfer Access and Management (FTAM), Virtual Terminal, and Computer-Based Message Systems). To this end, BBN participated in the key committees of the American National Standards Institute (ANSI), ISO, and International Telephone & Telegraph Consultative Committee (CCITT) concerned with the development of national and international networking protocol standards. During the course of this work, BBN representatives were appointed to key positions, including chairmanships and editorships, within the committees. BBN also produced complete standards documents, including formal descriptions, as well as prototype implementations, for many of the protocols being standardized.

As part of the support provided to NIST, BBN developed formal languages for specifying protocols and tools for automatic generation of significant portions of protocol implementations, and for verification, testing, and evaluation of prototype implementations. Some of BBN's work on computer-based message systems resulted in the publication of a FIPS, and our work on transport protocol became a FIPS.

ARPA Internet Protocols

BBN has played a central role in the development of many of the protocols in use today in the ARPA Internet, including Internet Protocol, Transmission Control Protocol, File Transfer Protocol, and TELNET. We have been involved in the specification and implementation of these protocols on a wide variety of computer systems. When BBN has not been directly involved in the original specification work for internet protocols (such as Stream Protocol and Network Voice Protocol), we have had much experience in their implementation on modern computing equipment.

III. G. Facilities to be Used

Corporate Facilities

Founded in 1948 as an acoustic consulting partnership, Bolt Beranek and Newman Inc. has grown into a diversified high-technology company. The company has earned an international reputation for innovative services and products related to acoustics and environmental technologies, information sciences, and computer and communications technologies.

BBN, which has its headquarters in Cambridge, Massachusetts, employs approximately 2000 people. More than 1000 are scientists and engineers, a large number of whom hold advanced degrees. The company is organized into three major divisions: BBN Communications Division, BBN Software Products Division, and BBN Systems and Technologies Division (from which the Communications and Software Products divisions evolved).

BBN Systems and Technologies performs the major research and development activities of the corporation and engages in technology transfer and systems development. Areas of specialization include architectural acoustics and environmental technologies; physical sciences; computer, communications, and information sciences; and graphics technology.

BBN Systems and Technologies' principal offices are located in Cambridge, Massachusetts. Other offices are located in New London, Connecticut; Newport, Rhode Island; San Diego and Canoga Park, California and Arlington, Virginia.

Computer Aided Design

BBN has heavily invested in CAD over the last decade in CAD software, workstations, engineer training, and design methodology. Multi-hundred chip boards are routinely designed and fully simulated using behavioral level models for the board environment. This design methodology has resulted in most prototype boards designed in the last few years being completely functional. BBN personnel have extensive experience developing the highest complexity Field Programmable Logic Arrays now available from Actel, Xylinx, and Altera.

Designs are captured in schematic form using Valid, in behavioral form using Synopsis, and in Finite State Machine form using Maxplus2. Behavioral and gate level simulations are performed using VerilogXL and analog sections are simulated using HPSPICE. Logic Automation models are utilized when available. Behavioral level models are created for non-library components. PC boards are designed using Valid to Allegro using components from over 200 project libraries. Timing analysis is performed using many device specific timing analyzers when available together with BBN developed analyzers. Documentation standards, file system structures, and revision control procedures provide a means for managing the thousands of files typically created for each project. Design guidelines for synchronization, clocking, timing margins, and parts usage provide further process control.

Computational Facilities

As a leading research and development organization in the computer, information, and physical sciences, BBN has highly developed and extensive computational, experimental, and software facilities. Our computer facilities range from numerous personal computers for our scientists, engineers and secretaries to large mainframe computers and parallel processors. Our computers are networked, allowing easy access to any system; and all of our systems are well supported by a variety of peripherals.

Workstations and Personal Computers

BBN utilizes a large number of personal workstations. In addition, BBN Systems and Technologies' staff currently have seven MASSCOMP and over 500 Sun workstations available for general use. A high percentage of our staff have a readily available or a dedicated Macintosh, IBM PC, PC/XT or PC/AT. Macintosh computers are the predominate PCs at BBN, and we have about 2000 of them in use throughout the corporation.

Shared Server Systems

BBN Systems and Technologies supports time shared general scientific computing with a variety of DEC and Sun systems, ranging from large mainframe to supermini computers. These include:

- Two VAX 8600 VMS systems with 3.6 gigabytes of storage;
- A MicroVAX 3600/VAXstation 3200 VMS cluster with 4.0 gigabytes of storage;
- A MicroVAX 3600 ULTRIX system with 1.5 gigabytes of storage;
- Over two dozen Sun 3 and Sun 4 UNIX compute and file servers with over 10 gigabytes of aggregate storage;
- A VAX 11/780 VMS system with an FPS AP-120 array processor and 4.0 gigabytes of storage; and
- Six large parallel processors.

Over 1000 PC and terminal users may access these systems through the networks described below.

Computer Networks

BBN has been working in network development and distributed processing since the 1960s when we developed the original 4-node ARPANET. Our networks include:

- BBNNET, an internal BBN packet-switching network consisting of more than a dozen BBN-designed packet switches and fifty host computers in Cambridge and Arlington, VA.

- FiberNet, an internal fiber-optics local area network supporting connections of hundreds of terminals, workstations, output devices and computers.

- Multiple Local Area Ether Networks, each supporting connection of a number of terminals, workstations, and computers.

- Approximately a dozen gateways connecting various BBN internal networks to each other and, in appropriate cases, to MILNET, CSNET, and NEARNet, ARPA's Defense Simulation Internet (also developed by BBN under contract to ARPA).

All BBN Systems and Technologies' offices are connected to these networks allowing any single user access to numerous computing systems. These systems are also available to non-BBN personnel, allowing clients access to powerful, global networks.

BBN operates and manages NEARNet, an Internet regional network. This provides high speed interconnect (10 Mbit/sec) in the Boston area and lower speeds throughout New England.

We are also developing the ground station for high bandwidth digital communications through the NASA ACTS (Advanced Communications Technology Satellite.)

III. H. Qualifications of Key Personnel, and other sources of support

Philip P. Carvey, Division Engineer

Education: BSEE, Illinois Institute of Technology, 1965; EE, Massachusetts Institute of Technology, 1967; MSEE, Massachusetts Institute of Technology, 1967

Professional Positions and Responsibilities

Mr. Carvey rejoined BBN in 1985 to work on the Monarch multiprocessor project. His responsibilities include contributing to all aspects of the architecture, modeling, verification, and chip development. The Monarch projects goal was to demonstrate the innovative use of VLSI technology in a fine grained shared memory multiprocessor. Four full custom CMOS chips were in partial phases of development before project termination.

Mr. Carvey was the principal designer of Butterfly multiprocessor. This machine interconnects up to 256-fully autonomous processors together through a Banyan style interconnect network. Mr. Carvey started custom chip designing in 1982 with an NMOS implementation of the entire Butterfly switch board.

Mr. Carvey was one of the original 8 employees to start Applicon Inc in 1969. Applicon introduced the first computer aided workstations for layout of integrated circuits. Mr. Carvey was the chief hardware architect/designer at Applicon. His designs often constituted 3/4 of Applicon yearly shipments. He generated hardware designs for a wide variety of projects including, a 32-bit processor, two 16-bit processors, three workstations, a math coprocessor, 6-10 Unibus interface boards, a family of digitizers, and a disk controller. He also developed the architecture, algorithms, and data structures for the circa 1978 state-of-the-art VLSI design workstation and wrote all drawing assembly code. Mr. Carvey also created CAEE programs for analysis and optimization of microwave networks available on time sharing machines prior to focusing on hardware development activities.

Publications

"The Monarch Parallel Processor Design," submitted to IEEE Computer Magazine.

Dr. Julio Escobar, Scientist

Education: Ph.D. (Electrical Engineering & Computer Science) M.I.T. (1988) E.E.(Electrical Engineering & Computer Science) M.I.T.. (1985) S.M.(Electrical Engineering & Computer Science) M.I.T. - (1985) B.Sc.(Electronics) U.M.I.S.T. - England (1982)

Professional Positions:

BBN Systems and Technologies Corporation, Cambridge, MA, 06/1988-present; IBM T. J. Watson Research Center, Yorktown Heights, NY, 09/1983-06/1984.

Professional Responsibilities and Projects:

Dr. Escobar has been involved in the development of computer network communication systems for local, wide, and nationwide data networks. He has experience in protocol design and system analysis. His expertise includes optical-based networks and radio-based networks.

Dr.Escobar is currently a member of the Gigabits Project at BBN Science and Technology Division. He is designing a multi-stream synchronization protocol for distributed computing applications such as multimedia applications and distributed processing. He is also in charge of planning networking experiments to test the synchronization protocol. His previous work in the Gigabits Project includes the design of a Segmentation and Reassembly protocol for cell-based networks and the theoretical analysis of buffer utilization in high-bandwidth, high-delay networks.

During his first 18 months at BBN Science and Technology Division, Dr. Escobar participated in the Survivable Adaptive Packet Radio Network Project. He designed the radio link Control algorithm for the Packet Radio Network protocol suite and developed the mathematical model for performance analysis. He was also a main designer and analyst of the Congestion Control algorithm in the protocol suite. He supervised simulation work to benchmark both algorithms. He also helped in the design of the Channel Access Protocols for the Packet Radio Units.

His Doctoral research, under Prof. Pierre Humblet, investigated optimal detection methods for Spread Spectrum Optical signals. The results included formulating a Probabilistic Model for analysis of the problem and identifying a simple detector architecture for implementation. He participated, with the rest of the group, in the inception of an experimental laboratory for optical communications sponsored by NYNEX of New England.

Dr. Escobar's field of Minor Studies for his Doctoral degree was in the area of Electromagnetic Theory, with advanced graduate courses in Electromagnetic Theory, Non-linear Optics and Receivers, Antennas and Signals.

Publications:

J. Escobar, G. Lauer, M. Steenstrup, "A Congestion-Control Algorithm for Receiver-Directed Packet-Radio Networks," Proc. of the Tactical Communications Conference, Fort Wayne, Indiana, April 1990.

J. Escobar, "Radio-Parameter Selection Algorithm for Receiver-Directed Packet-Radio networks (SRNTN-73)," Technical Report, No. 7172, BBN, Cambridge, Massachusetts, December 1989.

"Maximum Likelihood Detection for Probabilistic Models of Optical Code Division Multiple Access Channels," LIDS Technical Report 1782, LIDS, MIT, July 1988.

Dr. Lawrence D. Sher, Division Scientist

Education: B.S. (Physics), Drexel University, 1956; Graduate Study (Physics), Princeton University, 1956-1958; Ph.D. (Biomedical Engineering), University of Pennsylvania, 1963.

Professional Positions:

Assistant Professor, The Moore School of Electrical Engineering, University of Pennsylvania, 1964-1971; Bolt Beranek and Newman Inc. (BBN), 1971-present.

Professional Responsibilities and Projects:

Dr. Sher has been responsible for the conception, development, and application of the SpaceGraph Display, a new generic display technology capable of interactive computer graphics in true 3-D.

He is currently working on Pathfinder, a project that is exploring technologies for equipping special forces with various navigation, information, and communication tools.

Dr. Sher's academic experience has been valuable in creating a nine-hour video tape course which teaches the use of RS/1, a software product sold by BBN Software Products Corp. He teaches courses on RS/1 for BBN clients and for BBN staff members.

Selected Publications:

"The Oscillating-Mirror Technique for Realizing True 3-D," L. D. Sher, Chap. 13 in Stereo Computer Graphics and Other True 3D Technologies, Editor: D. F. McAllister, Princeton Univ. Press, in print (July, 1993)

"The Use of an Oscillating Mirror for Three-Dimensional Display," L. D. Sher and C.D. Barry, Chapter 6 in New Methodologies in Studies of Protein Configuration, Editor: T. T. Wu. Publisher: Van Nostrand Reinhold, NY. (1985)

"Near-to-farfield transition of a scalar-wave pencil beam" (with M. Lassoeur and H. Kritikos), J. Acoustical Society, 48, 414 (1970).

"On the possibility of non-thermal biological effects of pulsed electromagnetic fields" (with E. Kresch and H.P. Schwan), Biophysical Journal, 10, 970 (1970).

Patents:

"Three-dimensional Display," U.S. Patent No. 4,130,832 (Dec. 19, 1978).

Other Sources of Support

Mr. Carvey is also working part-time on the NASA ACTS Digital Terminal. Dr. Sher is also working part time on the ARPA Pathfinder project. Dr. Escobar is working on the ARPA Gigabits Networking Architecture Project.

III. I. Cost Breakdown by Major Task

Produce Documentation & Specifications for the Architecture - $ 62K

This will require us to:

- Document the BodyLAN architecture and network protocols.
- Develop specifications for interfacing to the PEA modem.
- Develop specifications for interfacing to the PDA modem.

Explore Synchronization, Error rates, & Low Power Circuits - $ 242K

This will require us to:

- Explore different synchronization protocols.
- Investigate error rates under narrowband interference and multiple BodyLANs .
- Carry out circuit design for the various low power circuits.
- Investigate frequency diversity benefits and complexity issues.

Develop Prototypes - $ 305K

This will require us to:

- Develop the PEA modems.
- Develop the PDA modems.
- Interface the modems to some PDA.
- Develop data pattern generators/checkers using existing RF chips, Field Programmable Logic Devices, and a low power microprocessor in the PDA interface.

Test With PDA - $ 115K

This will require us to:

- Develop the PDA interface software needed to evaluate the BodyLAN hardware performance.
- Carry out error rate tests.
- Carry out BodyLAN interference and narrowband interference tests.
- Compare test results with theoretical models and reconcile them.

Section IV. Bibliography of Relevant Technical Papers

"Maximum Likelihood Detection for Probabilistic Models of Optical Code Division Multiple Access Channels," LIDS Technical Report 1782, LIDS, MIT, July 1988.

The Code of Federal Regulations Title 47, Telecommunications, Part 15, Radio Frequency Devices, Subpart C, Intentional Radiators, Section 15.209, Radiated Emission Limits; General Requirements.

The International Special Committee on Radio Interference (CISPR) Publication 16.

BBN Proposal No. P94-LABS-C-002A

BodyLAN™: A Wireless Body Area Local Network

Wireless, Adaptive and Mobile Information Systems (WAMIS)

Area 1: Wireless Computing Systems

Volume II. Cost Proposal

Submitted by: BBN Systems and Technologies
A Division of Bolt Beranek and Newman Inc.
10 Moulton Street
Cambridge, MA 02138
BBN's business category: Large Business
Fax: (617) 873-3776

Technical POC: Philip P. Carvey
(617) 873-3208
PCarvey@BBN.COM

Administrative POC: Marguerite I. DiBlasio
(617) 873-3153
MDiblasio@BBN.COM

BBN SYSTEMS AND TECHNOLOGIES

17 February 1994

Directorate of Contracts
P.O. Box 748
Building No. 22208
Ft. Huachuca, AZ 85613

Attention: ATZS-DKM
Gloria Bickler
Contracting Officer
(602) 533-1338

Subject: Wireless Adaptive and Mobile Information Systems (WAMIS)
BBN Proposal No. P94-LABS-C-002A

Dear Ms. Bickler:

BBN Systems and Technologies, a Division of Bolt Beranek and Newman Inc. ("BBN"), is pleased to submit its revised Proposal No. P94-LABS-C-002A entitled "Wireless Adaptive and Mobile Information Systems (WAMIS)".

Our revised proposal assumes the award of a cost plus fixed fee type contract incorporating mutually acceptable terms and conditions. The cost estimate is based on a commencement date of April 1, 1994 with an eighteen (18) month period of performance. This proposal will remain valid for a period of sixty (60) days from the date of this letter.

Our revised proposal consists of the following:

1. This Cover Letter (Original plus four copies)
2. Volume II - Cost Proposal
   a. SF1411
   b. Supporting Schedules
   c. DD 1861
   d. Subcontracting Plan

This revised proposal has been prepared in accordance with BBN's standard procedures for pricing Government proposals.

BBN is a large business with revenue of approximately $233 million in 1993.

If you have any questions, or require any additional information, please do not hesitate to contact Mark J. Sherman, Senior Contracts Manager, at (617) 873-4296 or the undersigned at (617) 873-3153.

Sincerely,
BBN SYSTEMS AND TECHNOLOGIES

Marguerite I. DiBlasio
Senior Contract Administrator

cc: K. Gabriel, ARPA w/Enclosure
Effie Luzatis, DCAA w/Enclosure
F. Heart, BBN, w/o Enclosure
T. Blackadar, w/Enclosure

BBN Proposal No. P94-LABS-C-002A

CONTRACT PRICING PROPOSAL COVER SHEET

1. SOLICITATION/CONTRACT/MODIFICATION N: **BAA-93-27**

FORM APPROVED OMB NO. 3090-0116

NOTE: This form is used in contract actions if submission of cost or pricing data is required (See FAR 15.804-6(b))

2. NAME AND ADDRESS OF OFFEROR (Include ZIP Code)

BBN SYSTEMS AND TECHNOLOGIES,
A Division Bolt Beranek and Newman Inc.
10 MOULTON STREET
CAMBRIDGE, MA 02138

TELEPHONE NO. **(617)873-3153**
FACSIMILE **(617)873-3776**

3A. NAME AND TITLE OF OFFEROR'S POINT OF CONTACT
Marguerite I. DiBlasio
Senior Contract Administrator

3B. TELEPHONE NO.
(617) 873-3153

4. TYPE OF CONTRACT ACTION (Check)

X	A. NEW CONTRACT		D. LETTER CONTRACT
	B. CHANGE ORDER		E. UNPRICED ORDER
	C. PRICE REVISION/REDETERMINATION		F. OTHER (Specify)

5. TYPE OF CONTRACT (Check)
☐ FFP ☒ CPFF ☐ CPIF ☐ CPAF
☐ FPI ☐ OTHER

6. PROPOSED COST (A+B=C)

A. COST	B. PROFIT/FEE	C. TOTAL
$652,786	**$64,967**	**$717,753**

7. PLACE(S) AND PERIOD(S) OF PERFORMANCE
Cambridge, Massachusetts 02138 **18 Months**

8. List and reference the identification, quantity and total price proposed for each contract line item. A line item cost breakdown supporting this recap is required unless otherwise specified by the Contracting Officer. (Continue on reverse, and then on plain paper, if neccessary. Use same headings.)

A. LINE ITEM NO.	B. IDENTIFICATION	C. QUANTITY	D. TOTAL PRICE	E. REF.
	Wireless Adaptive Mobile Information Systems (WAMIS)	**1 LOT**	**$717,753**	**A**

9. PROVIDE NAME, ADDRESS, AND TELEPHONE NUMBER FOR THE FOLLOWING (If available)

A. CONTRACT ADMINISTRATION OFFICE
DCMAO, Boston
495 Summer Street
Boston, MA 02210
Ms. A. Fleming (617) 451-4158

B. AUDIT OFFICE
DCAA
Waltham Branch Office
424 Trapelo Road, Bldg. 137
Waltham, MA 02154-6397 **(617) 565-7340**

10. WILL YOU REQUIRE THE USE OF ANY GOVERNMENT PROPERTY IN THE PERFORMANCE OF THIS WORK? (If "Yes," identify)
☒ YES ☐ NO

11A. DO YOU REQUIRE GOVERNMENT CONTRACT FINANCING TO PERFORM THIS PROPOSED CONTRACT? (If "YES," complete Item 11B)
☐ YES ☒ NO

11B. TYPE OF FINANCING (X one)
☐ ADVANCE PAYMENTS ☐ PROGRESS PAYMENTS ☐ GUARANTEED LOANS

12. HAVE YOU BEEN AWARDED ANY CONTRACTS OR SUBCONTRACTS FOR THE SAME OR SIMILAR ITEMS WITHIN THE PAST 3 YEARS? (If "Yes," identify item(s), customer(s) and contract number(s))
☐ YES ☒ NO

13. IS THIS PROPOSAL CONSISTENT WITH YOUR ESTABLISHED ESTIMATING AND ACCOUNTING PRACTICES AND PROCEDURES AND FAR PART 31 COST PRINCIPLES? (If "No," explain)
☒ YES ☐ NO

14. COST ACCOUNTING STANDARDS BOARD (CASB) DATA (Public law 91-379 as amended and FAR PART 30)

A. WILL THIS CONTRACT ACTION BE SUBJECT TO CASB REGULATIO (If "No," explain in proposal)
☒ YES ☐ NO

B. HAVE YOU SUBMITTED A CASB DISCLOSURE STATEMENT (CASB DS-1 or 2)? (If "Yes," specify in proposal the office to which submitted and if determined to be adequate)
☒ YES ☐ NO **See Exhibit A**

C. HAVE YOU BEEN NOTIFIED THAT YOU ARE OR MAY BE IN NON-COMPLIANCE WITH YOUR DISCLOSURE STATEMENT OR COST ACCOUNTING STANDARDS? (If "Yes," explain in proposal)
☐ YES ☒ NO

D. IS ANY ASPECT OF THIS PROPOSAL INCONSISTENT WITH YOUR DISCLOSED PRACTICES OR APPLICABLE COST ACCOUNTING STANDARDS? (If "Yes," explain in proposal)
☐ YES ☒ NO

This proposal is submitted in response to the RFP, contract, modification, etc. in item 1 and reflects our best estimates and/or actual costs as of this date

15. NAME AND TITLE (Type)
Marguerite I. DiBlasio
Senior Contract Administrator

16. NAME OF FIRM
BBN SYSTEMS AND TECHNOLOGIES,
A Division of Bolt Beranek and Newman Inc.

17. SIGNATURE
Marguerite I. DiBlasio

18. DATE OF SUBMISSION
02/15/94

NSN 7540-01-142-9845 1411-102 STANDARD FORM 1411 (REV. 7-87)

USE OF DISCLOSURE OF DATA CONTAINED ON THIS SHEET IS SUBJECT TO THE RESTRICTION ON THE TITLE PAGE OF THIS PROPOSAL

EXHIBIT A

The Company's disclosure statement, dated July 1, 1992 was filed with DCMAO, Boston, and was determined to be adequate. The Company has filed a revised Disclosure Statement with DCMAO, Boston, dated July 1, 1993 and has not yet been notified of a determination of adequacy.

REFERENCE A

TOTAL GFY'S
PERIOD OF PERFORMANCE
04/01/94 09/30/95
TOTAL MOS. 18

DIRECT LABOR CLASSIFICATIONS	LEVEL	Document/Specifications HOURS	Document/Specifications AMOUNT	Synchronization/Error HOURS	Synchronization/Error AMOUNT	Develop Prototypes HOURS	Develop Prototypes AMOUNT	Test W/PDA HOURS	Test W/PDA AMOUNT	TOTAL GFY'S HOURS	TOTAL GFY'S AMOUNT
Lead Engineer	24	160	7,998	160	8,170	480	24,510	480	24,510	1,280	65,187
Senior Scientist	23	80	3,246	960	39,795	640	26,530	200	8,291	1,880	77,863
Scientist/Engineer	21	120	3,884	160	5,277	960	31,743	80	2,645	1,320	43,549
Staff Sci/Eng	19	0	0	0	0	180	4,771	80	2,121	260	6,892
Prog Admin/Tech	16	0	0	0	0	400	8,675	0	0	400	8,675
System Admin	13	0	0	0	0	160	2,729	0	0	160	2,729
Senior Secretary	10	200	2,853	0	0	0	0	0	0	200	2,853
TOTAL DIRECT LABOR		560	17,982	1,280	53,242	2,820	98,959	840	37,566	5,500	207,749
TOTAL OVERHEAD		17,982	21,902	53,242	63,113	98,959	117,266	37,566	44,516	207,749	246,797
TRAVEL		TRIPS/DAYS		TRIPS/DAYS		TRIPS/DAYS		TRIPS/DAYS		TRIPS/DAYS	
Bos/Washington, D.C.		0	0	2	2,022	0	0	0	0	2	2,022
Subsistence - Washington, D.C.		0	0	6	903	0	0	0	0	6	903
Bos/Los Angeles		1	2,395	0	0	0	0	2	4,841	3	7,236
Subsistence - Los Angeles		3	423	0	0	0	0	8	1,139	11	1,562
Auto Rental		3	136	3	137	0	0	4	183	10	456
TOTAL TRAVEL			2,953		3,062		0		6,163		12,179
DIRECT MATERIAL/SUBCONTRACTS/CONSULTANTS											
Gateway 4DX2-66V		0	0	1	2,795	0	0	0	0	1	2,795
CDW Ethernet Card 3C503		0	0	1	160	0	0	0	0	1	160
Data I/O PCMCIA CARDPRO2-EXT		0	0	1	389	0	0	0	0	1	389
Tape Backup 250 DJ-20		0	0	1	174	0	0	0	0	1	174
Tape Cartridges Jumbo DT-250		0	0	6	138	0	0	0	0	6	138
Power Supply Smart UPS 600		0	0	1	329	0	0	0	0	1	329
Norton Utilities 5136		0	0	1	116	0	0	0	0	1	116
Norton Utilities LapLink V		0	0	1	100	0	0	0	0	1	100
Borland C++		0	0	1	315	0	0	0	0	1	315
Network Software FTP PC/TCP TCP/IP		0	0	1	319	0	0	0	0	1	319
Personal Digital Assistant 486DX2-40		0	0	2	3,990	0	0	0	0	2	3,990
Spare NiMH Batteries		0	0	2	178	0	0	0	0	2	178
Advance Photographic Artwork		0	0	24	900	0	0	0	0	24	900
PDA Modem on PCMCIA Card		0	0	2	1,000	0	0	0	0	2	1,000
PDA Modem W/Pattern Generator/Check		0	0	5	1,250	0	0	0	0	5	1,250
PEA Modem W/Pattern Generator/Check		0	0	16	4,000	0	0	0	0	16	4,000
Lab Equipment Rental		0	0	1	3,000	0	0	0	0	1	3,000
Miscellaneous Hardware		0	0	1	1,000	0	0	0	0	1	1,000
RF Expertise Consulting		0	0	416	24,960	0	0	0	0	416	24,960
TOTAL DIRECT MATERIAL/SUBCONTRACTS/CONSULTANTS			0		45,113		0		0		45,113
DIRECT MATERIAL HANDLING		0	0	45,113	2,256	0	0	0	0	45,113	2,256
OTHER DIRECT COSTS		UNITS		UNITS		UNITS		UNITS		UNITS	
Labs Computer Center		0	0	11,429	20,001	0	0	0	0	11,429	20,001
Labs Computer Center		0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0
TOTAL OTHER DIRECT COSTS			0		20,001		0		0		20,001
SUBTOTAL			42,837		186,786		216,225		88,246		534,094
GENERAL & ADMINISTRATIVE		42,837	10,281	141,674	33,442	216,225	51,029	88,246	20,826	488,981	115,578
ESTIMATED COST WITHOUT COST OF CAPITAL			53,118		220,228		267,254		109,072		649,672
COST OF CAPITAL		BASE		BASE		BASE		BASE		BASE	
Direct Labor		17,982	167	53,242	553	98,959	1,028	37,566	390	207,749	2,159
G & A		42,837	51	141,674	167	216,225	255	88,246	104	488,981	577
Labs Computer Center		0	0	20,001	379	0	0	0	0	20,001	379
TOTAL COST OF CAPITAL			237		1,099		1,283		494		3,114
TOTAL ESTIMATED COST WITH COST OF CAPITAL			53,356		221,327		268,537		109,566		652,786
FIXED FEE		53,118	5,312	220,228	22,023	267,254	26,725	109,072	10,907	649,672	64,967
TOTAL ESTIMATED COST AND FIXED FEE			58,668		243,350		295,262		120,473		717,753

Basis of Estimate

- A PC Magazine
- B PC Magazine
- C Quotation
- D PC Catalogue
- E PC Catalogue
- F PC Catalogue
- G PC Magazine
- H PC Magazine
- I PC Catalogue (Typo)
- J PC Catalogue
- K PC Magazine
- L PC Magazine
- M BBN Bulk Quote/Eng Est
- N Engineering Estimate
- O Engineering Estimate
- P Engineering Estimate
- Q Engineering Estimate
- R Engineering Estimate
- S Quote

GFY 94
PERIOD OF PERFORMANCE
04/01/94 06/30/94
TOTAL MOS. 3

LEVEL 01/06/94
D/L AVG. 01/01/94
APR= 5.000%
MONTHS FROM MBREP TO START = 1.5

DIRECT LABOR CLASSIFICATIONS	LEVEL	RATE MEMO #94.03	ESC. = 101.250%	Document/Specifications HOURS	Document/Specifications AMOUNT	Synchronization/Error HOURS	Synchronization/Error AMOUNT	Develop Prototypes HOURS	Develop Prototypes AMOUNT	Test W/PDA HOURS	Test W/PDA AMOUNT	TOTAL HOURS	GFY 94 AMOUNT
Lead Engineer	24	49.37	49.99	160	7,998		0		0		0	160	7,998
Senior Scientist	23	40.08	40.58	80	3,246		0		0		0	80	3,246
Scientist/Engineer	21	31.97	32.37	120	3,884	20	647		0		0	140	4,532
Staff Sci/Eng	19	25.63	25.95		0		0		0		0	0	0
Prog Admin/Tech	16	20.97	21.23		0		0		0		0	0	0
System Admin	13	16.49	16.70		0		0		0		0	0	0
Senior Secretary	10	14.09	14.27	200	2,853		0		0		0	200	2,853
TOTAL DIRECT LABOR				560	17,982	20	647	0	0	0	0	580	18,629
TOTAL OVERHEAD		121.80% X D/L BASE OF		17,982	21,902	647	789	0	0	0	0	18,629	22,691
TRAVEL 02/01/94		OAG RATE +	ESC. = 100.625%	TRIPS/DAYS		TRIPS/DAYS		TRIPS/DAYS		TRIPS/DAYS		TRIPS/DAYS	
Bos/Washington, D.C.		994.00	1,000.21		0		0		0		0	0	0
Subsistence - Washington, D.C.		148.00	148.93		0		0		0		0	0	0
Bos/Los Angeles		2,380.00	2,394.88	1	2,395		0		0		0	1	2,395
Subsistence - Los Angeles		140.00	140.88	3	423		0		0		0	3	423
Auto Rental		45.00	45.28	3	136		0		0		0	3	136
TOTAL TRAVEL					2,953		0		0		0		2,953
DIRECT MATERIAL/SUBCONTRACTS/CONSULTANTS													
Gateway 4DX2-66V		2,795.00 /Each			0	1	2,795		0		0		2,795
CDW Ethernet Card 3C503		159.84 /Each			0	1	160		0		0		160
Data I/O PCMCIA CARDPRO2-EXT		389.00 /Each			0	1	389		0		0		389
Tape Backup 250 DJ-20		174.00 /Each			0	1	174		0		0		174
Tape Cartridges Jumbo DT-250		23.00 /Each			0	6	138		0		0		138
Power Supply Smart UPS 600		329.00 /Each			0	1	329		0		0		329
Norton Utilities 5136		115.95 /Each			0	1	116		0		0		116
Norton Utilities LapLink V		99.95 /Each			0	1	100		0		0		100
Borland C++		315.00 /Each			0	1	315		0		0		315
Network Software FTP PC/TCP TCP/IP		319.00 /Each			0	1	319		0		0		319
Personal Digital Assistant 486DX2-40		1,995.00 /Each			0		0		0		0		0
Spare NiMH Batteries		89.00 /Each			0		0		0		0		0
Advance Photographic Artwork		37.50 /Each			0		0		0		0		0
PDA Modem on PCMCIA Card		500.00 /Each			0		0		0		0		0
PDA Modem W/Pattern Generator/Check		250.00 /Each			0		0		0		0		0
PEA Modem W/Pattern Generator/Check		250.00 /Each			0		0		0		0		0
Lab Equipment Rental		3,000.00 /Each			0		0		0		0		0
Miscellaneous Hardware		1,000.00 /Each			0		0		0		0		0
RF Expertise Consulting		60.00 /Hour			0		0		0		0		0
TOTAL DIRECT MATERIAL/SUBCONTRACTS/CONSULTANTS					0		4,835		0		0		4,835
DIRECT MATERIAL HANDLING		5.00% X BASE OF		0	0	4,835	242	0	0	0	0	4,835	242
OTHER DIRECT COSTS				UNITS		UNITS		UNITS		UNITS		UNITS	
Labs Computer Center		1.75 /CRU			0		0		0		0	0	0
Labs Computer Center		0.00 /Sq Ft Mo			0		0		0		0	0	0
		0.00 /Hour			0		0		0		0	0	0
TOTAL OTHER DIRECT COSTS					0		0		0		0		0
SUBTOTAL					42,837		6,512		0		0		49,350
GENERAL & ADMINISTRATIVE		24.00% X BASE OF		42,837	10,281	1,678	403	0	0	0	0	44,515	10,684
ESTIMATED COST WITHOUT COST OF CAPITAL					53,118		6,915		0		0		60,033
COST OF CAPITAL				BASE		BASE		BASE		BASE		BASE	
Direct Labor		.01039		17,982	187	647	7	0	0	0	0	18,629	194
G & A		.00118		42,837	51	1,678	2	0	0	0	0	44,515	53
Labs Computer Center		.01893		0	0	0	0	0	0	0	0	0	0
TOTAL COST OF CAPITAL					237		9		0		0		246
TOTAL ESTIMATED COST WITH COST OF CAPITAL					53,356		6,924		0		0		60,280
FIXED FEE				53,118	5,312	6,915	692	0	0	0	0	60,033	6,003
TOTAL ESTIMATED COST AND FIXED FEE					58,668		7,615		0		0		66,283

Basis of Estimate

- A PC Magazine
- B PC Magazine
- C Quotation
- D PC Catalogue
- E PC Catalogue
- F PC Catalogue
- G PC Magazine
- H PC Magazine
- I PC Catalogue (Typo)
- J PC Catalogue
- K PC Magazine
- L PC Magazine
- M BBN Bulk Quote/Eng Est
- N Engineering Estimate
- O Engineering Estimate
- P Engineering Estimate
- Q Engineering Estimate
- R Engineering Estimate
- S Quote

GFY 94-95
PERIOD OF PERFORMANCE 07/01/94 09/30/95
TOTAL MOS. 15
APR= 3.400%
ESCALATED MONTHS FROM MBREP TO START = 4.5

DIRECT LABOR CLASSIFICATIONS	LEVEL	RATE FROM GFY 94	ESC. = 102.150%	Document/Specifications HOURS	Document/Specifications AMOUNT	Synchronization/Error HOURS	Synchronization/Error AMOUNT	Develop Prototypes HOURS	Develop Prototypes AMOUNT	Test W/PDA HOURS	Test W/PDA AMOUNT	TOTAL HOURS	TOTAL GFY 94-95 AMOUNT
Lead Engineer	24	49.99	51.06		0	160	8,170	480	24,510	480	24,510	1,120	57,189
Senior Scientist	23	40.58	41.45		0	960	39,795	640	26,530	200	8,291	1,800	74,616
Scientist/Engineer	21	32.37	33.07		0	140	4,629	960	31,743	80	2,645	1,180	39,017
Staff Sci/Eng	19	25.95	26.51		0		0	180	4,771	80	2,121	260	6,892
Prog Admin/Tech	16	21.23	21.69		0		0	400	8,675		0	400	8,675
System Admin	13	16.70	17.06		0		0	160	2,729		0	160	2,729
Senior Secretary	10	14.27	14.57		0		0		0		0	0	0
TOTAL DIRECT LABOR				0	0	1,260	52,594	2,820	98,959	840	37,566	4,920	189,119
TOTAL OVERHEAD		118.50% X D/L BASE OF		0	0	52,594	62,324	98,959	117,256	37,566	44,515	189,119	224,106
TRAVEL		GFY 94	ESC. = 101.075%	TRIPS/DAYS		TRIPS/DAYS		TRIPS/DAYS		TRIPS/DAYS		TRIPS/DAYS	
Bos/Washington, D.C.		1,000.21	1,010.96		0	2	2,022		0		0	2	2,022
Subsistence - Washington, D.C.		148.93	150.53		0	6	903		0		0	6	903
Bos/Los Angeles		2,394.88	2,420.62		0		0		0	2	4,841	2	4,841
Subsistence - Los Angeles		140.88	142.39		0		0		0	8	1,139	8	1,139
Auto Rental		45.28	45.77		0	3	137		0	4	183	7	320
TOTAL TRAVEL					0		3,062		0		6,163		9,226
DIRECT MATERIAL/SUBCONTRACTS/CONSULTANTS													
Gateway 4DX2-66V		2,795.00 /Each			0		0		0		0		0
CDW Ethernet Card 3C503		159.84 /Each			0		0		0		0		0
Data I/O PCMCIA CARDPRO2-EXT		389.00 /Each			0		0		0		0		0
Tape Backup 250 DJ-20		174.00 /Each			0		0		0		0		0
Tape Cartridges Jumbo DT-250		23.00 /Each			0		0		0		0		0
Power Supply Smart UPS 600		329.00 /Each			0		0		0		0		0
Norton Utilities 5136		115.95 /Each			0		0		0		0		0
Norton Utilities LapLink V		89.95 /Each			0		0		0		0		0
Borland C++		315.00 /Each			0		0		0		0		0
Network Software FTP PC/TCP TCP/IP		319.00 /Each			0		0		0		0		0
Personal Digital Assistant 486DX2-40		1,995.00 /Each			0	2	3,990		0		0		3,990
Spare NiMH Batteries		89.00 /Each			0	2	178		0		0		178
Advance Photographic Artwork		37.50 /Each			0	24	900		0		0		900
PDA Modem on PCMCIA Card		500.00 /Each			0	2	1,000		0		0		1,000
PDA Modem W/Pattern Generator/Check		250.00 /Each			0	5	1,250		0		0		1,250
PEA Modem W/Pattern Generator/Check		250.00 /Each			0	16	4,000		0		0		4,000
Lab Equipment Rental		3,000.00 /Each			0	1	3,000		0		0		3,000
Miscellaneous Hardware		1,000.00 /Each			0	1	1,000		0		0		1,000
RF Expertise Consulting		60.00 /Hour			0	416	24,960		0		0		24,960
TOTAL DIRECT MATERIAL/SUBCONTRACTS/CONSULTANTS					0		40,278		0		0		40,278
DIRECT MATERIAL HANDLING		5.00% X BASE OF		0	0	40,278	2,014	0	0	0	0	40,278	2,014
OTHER DIRECT COSTS				UNITS		UNITS		UNITS		UNITS		UNITS	
Labs Computer Center		1.75 /CRU			0	11,429	20,001		0		0	11,429	20,001
Labs Computer Center		0.00 /Sq Ft Mo			0		0		0		0	0	0
		0.00 /Hour			0		0		0		0	0	0
TOTAL OTHER DIRECT COSTS					0		20,001		0		0		20,001
SUBTOTAL					0		180,274		216,225		88,246		484,744
GENERAL & ADMINISTRATIVE		23.60% X BASE OF		0	0	139,996	33,039	216,225	51,029	88,246	20,826	444,466	104,894
ESTIMATED COST WITHOUT COST OF CAPITAL					0		213,313		267,254		109,072		589,638
COST OF CAPITAL				BASE		BASE		BASE		BASE		BASE	
Direct Labor		.01039		0	0	52,594	546	98,959	1,028	37,566	390	189,119	1,965
G & A		.00118		0	0	139,996	165	216,225	255	88,246	104	444,466	524
Labs Computer Center		.01893		0	0	20,001	379	0	0	0	0	20,001	379
TOTAL COST OF CAPITAL					0		1,090		1,283		494		2,868
TOTAL ESTIMATED COST WITH COST OF CAPITAL					0		214,403		268,537		109,566		592,506
FIXED FEE				0	0	213,313	21,331	267,254	26,725	109,072	10,907	589,638	58,964
TOTAL ESTIMATED COST AND FIXED FEE					0		235,734		295,262		120,473		651,470

Basis of Estimate

- A PC Magazine
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- F PC Catalogue
- G PC Magazine
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- I PC Catalogue (Typo)
- J PC Catalogue
- K PC Magazine
- L PC Magazine
- M BBN Bulk Quote/Eng Est
- N Engineering Estimate
- O Engineering Estimate
- P Engineering Estimate
- Q Engineering Estimate
- R Engineering Estimate
- S Quote

(A)

INTEGRATED & VESA SYSTEMS

4SX-33/4DX-33

- Intel 33MHz 486SX or DX CPU
- 4MB RAM
- 212MB 13ms IDE Hard Drive
- Local Bus Graphics with 512KB
- 3.5" Diskette Drive
- 14" Color CrystalScan® 1024NI
- Mini Desktop Case
- 5 16-Bit ISA Slots
- 101-Key Keyboard & MS Mouse
- MS-DOS® 6.2 & WFW™ 3.11
- MS Works for Windows™
- EPA Energy Star Compliant

4SX-33 - **$1295**

4DX-33 - **$1495**

4DX2-50/4DX2-66

- Intel 50 or 66MHz 486DX2 CPU
- 4MB RAM, 128KB Cache
- 424MB 13ms IDE Hard Drive
- Local Bus Graphics with 1MB
- 3.5" Diskette Drive
- 14" Color CrystalScan 1024NI
- Mini Desktop Case
- 5 16-Bit ISA Slots
- AnyKey® Keyboard & MS Mouse
- MS-DOS 6.2 & WFW 3.11
- Choice of Application Software
- EPA Energy Star Compliant

4DX2-50 - **$1795**

4DX2-66 - **$1995**

4SX-33V

- Intel® 33MHz 486SX CPU
- 4MB RAM
- 212MB 13ms IDE Hard Drive
- VLB™ Graphics with 1MB
- Local Bus IDE Interface
- 5.25" & 3.5" Combo Drive
- 14" Color CrystalScan® 1024NI
- Baby AT Case
- 5 ISA & 2 VESA®/ISA Slots
- AnyKey® Keyboard & MS Mouse
- MS-DOS® 6.2 & WFW™ 3.11
- Choice of Application Software
- EPA Energy Star Compliant

$1495

4DX2-50 FAMILY PC

- Intel 50MHz 486DX2 CPU
- 8MB RAM, 128KB Cache
- 212MB 13ms IDE Hard Drive
- Local Bus Graphics with 1MB
- Double-Speed CD-ROM, 16-Bit Sound Card & Speakers
- 2400/9600 Data/Fax Modem
- 3.5" Diskette Drive
- 14" Color CrystalScan 1024NI
- Mini Desktop Case
- 5 16-Bit ISA Slots
- 101-Key Keyboard, MS Mouse & Joystick
- Choice of Family PC Software
- EPA Energy Star Compliant

$1995

VESA & PCI SYSTEMS

4DX-33V/4DX2-50V

- Intel 33MHz 486DX or 50MHz DX2 CPU
- 8MB RAM, 128KB Cache
- 424MB 13ms IDE Hard Drive
- VLB Graphics with 1MB
- Local Bus IDE Interface
- 5.25" & 3.5" Combo Drive
- 14" Color CrystalScan 1024NI
- Baby AT Case
- 5 ISA & 2 VESA/ISA Slots
- AnyKey Keyboard & MS Mouse
- MS-DOS 6.2 & WFW 3.11
- Choice of Application Software
- EPA Energy Star Compliant

4DX-33V - **$1975**

4DX2-50V - **$1995**

4DX2-66V BEST BUY

- Intel 66MHz 486DX2 CPU
- 8MB RAM, 128KB Cache
- 424MB 13ms IDE Hard Drive
- VLB Graphics with 1MB
- Double-Speed CD-ROM
- Local Bus IDE Interface
- 3.5" Diskette Drive
- 15" Color CrystalScan 1572FS
- Baby AT Case
- 5 ISA & 2 VESA/ISA Slots
- AnyKey Keyboard & MS Mouse
- MS-DOS 6.2 & WFW 3.11.
- Choice of Application Software
- EPA Energy Star Compliant

$2295

P4D-66

- Intel 66MHz 486DX2 CPU
- 8MB RAM, 256KB Cache
- 424MB 13ms IDE Hard Drive
- PCI Local Bus Graphics with 2MB
- Double-Speed CD-ROM
- 3.5" Diskette Drive
- 15" Color CrystalScan 1572FS
- Baby AT Case
- 4 ISA, 2 PCI & 1 PCI/ISA Slots
- AnyKey Keyboard & MS Mouse
- MS-DOS 6.2 & WFW 3.11
- Choice of Application Software

$2495

4DX2-66V

- Intel 66MHz 486DX2 CPU
- 16MB RAM, 128KB Cache
- 424MB 13ms IDE Hard Drive
- VLB Graphics with 2MB
- Double-Speed CD-ROM
- Local Bus IDE Interface
- 3.5" Diskette Drive
- 15" Color CrystalScan 1572FS
- Baby AT Case
- 5 ISA & 2 VESA/ISA Slots
- AnyKey Keyboard & MS Mouse
- MS-DOS 6.2 & WFW 3.11
- Choice of Application Software
- EPA Energy Star Compliant

$2795

PENTIUM SYSTEMS

P5-60

- Intel 60MHz Pentium™ CPU
- 8MB RAM, 256KB Cache
- 424MB 13ms IDE Hard Drive
- PCI Local Bus Graphics with 2MB
- 3.5" Diskette Drive
- 14" Color CrystalScan 1024NI
- Baby AT Case
- 4 ISA, 2 PCI & 1 PCI/ISA Slots
- AnyKey Keyboard & MS Mouse
- MS-DOS 6.2 & WFW 3.11
- MS Works for Windows

$2495

P5-60 BEST BUY

- Intel 60MHz Pentium CPU
- 8MB RAM, 256KB Cache
- 424MB 13ms IDE Hard Drive
- PCI Local Bus Graphics with 2MB
- Double-Speed CD-ROM
- 3.5" Diskette Drive
- 15" Color CrystalScan 1572FS
- Baby AT Case
- 4 ISA, 2 PCI & 1 PCI/ISA Slots
- AnyKey Keyboard & MS Mouse
- MS-DOS 6.2 & WFW 3.11
- Choice of Application Software

$2795

P5-60

- Intel 60MHz Pentium CPU
- 16MB RAM, 256KB Cache
- 540MB 13ms IDE Hard Drive
- PCI Local Bus Graphics with 2MB
- Double-Speed CD-ROM
- 3.5" Diskette Drive
- 15" Color CrystalScan 1572FS
- Baby AT Case
- 4 ISA, 2 PCI & 1 PCI/ISA Slots
- AnyKey Keyboard & MS Mouse
- MS-DOS 6.2 & WFW 3.11
- Choice of Application Software

$3295

P5-66

- Intel 66MHz Pentium CPU
- 16MB RAM, 256KB Cache
- 540MB 13ms IDE Hard Drive
- PCI Local Bus Graphics with 2MB
- Double-Speed CD-ROM
- 16-Bit Sound Card & Speakers
- 3.5" Diskette Drive
- 17" Color CrystalScan 1776LE
- Tower Case, 300W Power Supply
- 4 ISA, 2 PCI & 1 PCI/ISA Slots
- AnyKey Keyboard & MS Mouse
- MS-DOS 6.2 & WFW 3.11
- Choice of Application Software

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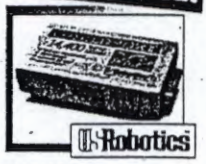

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(B)

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TC5245 ARCNET COAX CARD	179.99
TC5249 ARCNET TP CARD	99.94
TC5245 ARCNET ALL-IN-ONE CARD	258.34
TC5040 ARCNET PASSIVE 4 PORT HUB COAX	39.50
TC5055 ETHERNET 8 PORT CON 10BT	328.74
TC6151 ARCNET 16 PORT SMART HUB COAX	672.12
TC4035 TOKEN RING 4MBPS CARD	299.99
TC4045 TOKEN RING 16/4 CARD	359.44
TCNS 100MBPS COAX CARD	438.57
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TCNS 100MBPS STP CARD	457.88
TCNS 100MBPS FIBER OPTIC CARD	715.60
TCNS 100MBPS 6 PORT SMART HUB COAX	1366.27
TCNS 100MBPS 8 PORT SMART HUB COAX	1149.47
TCNS 100MBPS 8 PORT SMART HUB STP	1169.75
TCNS 100MBPS 8 PORT SMART HUB FIBER	1486.80

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NODERUNNER 2000T	178.47
NODERUNNER 2000C	178.47
NODERUNNER/SI 2000A	119.88
NODERUNNER/SI 2000T	95.44
NODERUNNER/SI 2000C	97.44
CENTRAL STATION II	389.89
10BT 5 PORT INTERNAL HUB	269.33
NODERUNNER STARTER KIT WINDOWS	499.57
LANTASTIC AI V5.0	79.17
LANTASTIC AI V5.0 WINDOWS	79.19
LANTASTIC SOFTWARE	69.80
LANTASTIC FOR WINDOWS SW	129.68
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T-RUNNER 12 PORT 10BT	497.41

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ULTRA16 ETHERNET 10BT 6PK	583.68
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ULTRA16 ETHERNET COMBO 6PK	693.49
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ETHERCARD+ ELITE COAX	119.64
ETHERCARD+ ELITE COAX 6PK	628.73
ETHERCARD+ ELITE MCA COAX	189.26
ETHERCARD+ ELITE 10BT	119.64
ETHERCARD+ ELITE 10BT 6PK	619.22
ETHERCARD+ ELITE MCA 10BT	189.55
ETHERCARD+ ELITE EISA 10BT	579.78
ETHERCARD+ ELITE COMBO	139.57
ETHERCARD+ ELITE COMBO 6PK	753.59
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3512 ETHERNET 12+2 PORT CON 10BT	614.76
PC600WS ARCNET CARD COAX	125.93
PC650WS ARCNET CARD TP	119.88
PC600FS ARCNET CARD COAX	199.29
PC130 ARCNET CARD COAX	68.50
ARCNET 8 PORT ACTIVE HUB COAX	229.41
TOKENCARD ELITE 16/4	289.88

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3C509 ETHERLINK III MCA 10BT	242.45
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ETHEREXPRESS 16 10BT 20PK	1698.38
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EtherLink II/16 Coax	1.5 lbs.	$154
EtherLink II/16 TP	1.5 lbs.	$164
EtherLink III	Call	Call
EtherLink/MC	1.5 lbs.	$264
LinkBuilder 12TP	5.0 lbs.	$379

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Advanced Digital Systems

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Back-UPS 250	15.5 lbs.	$98
Back-UPS 400	17.5 lbs.	$155
Back-UPS 450	26.5 lbs.	$188
Back-UPS 600	26.5 lbs.	$257
Back-UPS 900	52.0 lbs.	$359
Back-UPS 1250	50.0 lbs.	$479
Smart UPS 400	21.5 lbs.	$279
Smart UPS 600	31.0 lbs.	$329
Smart UPS 900	48.5 lbs.	$529
Surge Arrest Plus	2.5 lbs.	$29
Wallmount	1.5 lbs.	$20
With Telephone & 3 Outlets	1.5 lbs.	$34
With Telephone & 7 Outlets	2.5 lbs.	$49

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AE-3 Ethernet Adapter	1.5 lbs.	$218
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NetWare	8.0 lbs.	$372
Central Station II LANtastic	7.5 lbs.	$379
Central Station II NetWare	7.5 lbs.	$379

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Boca Modems *Internal 14,400 Baud V32*	2.0 lbs.	$168
External 14,400 Baud V42	4.5 lbs.	$149
Other Boca Modems	Call	Call
BocaBoard 16-Port Intelligent	5.0 lbs.	$389

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CDS-435 Internal 600MB CD-ROM Drive	6.0 lbs.	$314
Other CD-ROM Hardware	Call	Call

Colorado Memory Systems

Jumbo Tape Drives *250 QJ-20 Tape Drive*	4.0 lbs.	$174
Trakker 120MB Backup	5.0 lbs.	$287
Trakker 250MB Backup	9.0 lbs.	$344
FC-10 Tape Controller	1.0 lbs.	$62
Jumbo DT-250 Cartridge	0.5 lbs.	$23
PowerTape	Call	Call
2GB Internal w/ SCSI Controller	7.0 lbs.	$948
2GB Tapes	1.0 lbs.	$45
4GB External w/ SCSI Controller	15.0 lbs.	$1585
4GB Internal w/SCSI Controller	7.0 lbs.	$1479

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BARCODE READERS *Wedge*	2.0 lbs.	$219
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Creative Labs

Discovery 16-bit CD-ROM *Int Double Speed*	Call	$429
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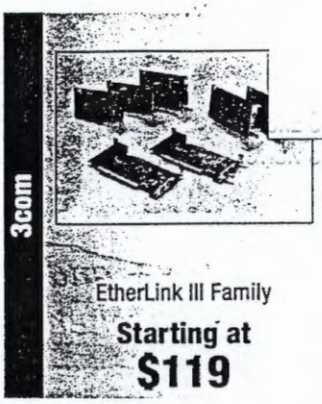
OmniCD	Call	Call



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ComputerEyes/LPT Color *NTSC*	2.0 lbs.	$299
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Color Pal	1.5 lbs.	$219
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Color Pal for Macintosh	1.5 lbs.	$279
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OPTIMA *OPTIMA 24 + Fax96*	6.0 lbs.	$116
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Multimedia Business Comm Pack	11.0 lbs.	$484
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MicroSaver *Security System*	1.0 lbs.	$45
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LaserMaster

WinJet Upgrade *Upgrade 300*	2.5 lbs.	$187
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EtherLink II/16 *Coax* ..... 1.5 lbs. $154
EtherLink II/16 *TP* ..... 1.5 lbs. $164
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EtherLink/MC ..... 1.5 lbs. $264
LinkBuilder 12TP ..... 5.0 lbs. $379

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Disk Controller Kit ..... Call Call

Advanced Digital Systems

VGA TV Elite ..... Call $259

American Power Conversion

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Back-UPS 400 ..... 17.5 lbs. $155
Back-UPS 450 ..... 26.5 lbs. $188
Back-UPS 600 ..... 26.5 lbs. $257
Back-UPS 900 ..... 52.0 lbs. $359
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Wallmount ..... 1.5 lbs. $20
With Telephone & 3 Outlets ..... 1.5 lbs. $34
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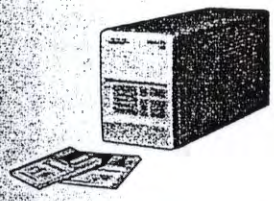

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Ethernet Adapter ..... Call Call

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AE-2/T Ethernet Adapter ..... 1.5 lbs. $179
AE-3 Ethernet Adapter ..... 1.5 lbs. $218
Artisoft Central Station *LANtastic* ..... 7.5 lbs. $309
NetWare ..... 8.0 lbs. $372
Central Station II LANtastic ..... 7.5 lbs. $379
Central Station II NetWare ..... 7.5 lbs. $379

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Ethernet Cards for Macintosh ..... Call Call

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Boca Modems *Internal 14,400 Baud V32* ..... 2.0 lbs. $168
External 14,400 Baud V42 ..... 4.5 lbs. $149
Other Boca Modems ..... Call Call
BocaBoard 16-Port Intelligent ..... 5.0 lbs. $389

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CDS-435 Internal 600MB CD-ROM Drive *6.0 lbs.* $314
Other CD-ROM Hardware ..... Call Call

Colorado Memory Systems

Jumbo Tape Drives *250 DJ-20 Tape Drive* ..... 4.0 lbs. $174
Trakker 120MB Backup ..... 5.0 lbs. $287
Trakker 250MB Backup ..... 9.0 lbs. $344
FC-10 Tape Controller ..... 1.0 lbs. $62
Jumbo DT-250 Cartridge ..... 0.5 lbs. $23
PowerTape ..... Call Call
2GB Internal w/ SCSI Controller ..... 7.0 lbs. $948
2GB Tapes ..... 1.0 lbs. $45
4GB External w/ SCSI Controller ..... 15.0 lbs. $1585
4GB Internal w/SCSI Controller ..... 7.0 lbs. $1479

COMPUTERWISE

BARCODE READERS *Wedge* ..... 2.0 lbs. $219
Serial ..... 2.5 lbs. $219

Creative Labs

Discovery 16-bit CD-ROM *Int Double Speed* ..... Call $429
External Double Speed ..... Call $495
OmniCD ..... Call Call

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3799

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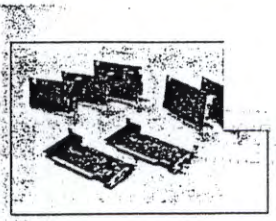


EtherLink III Family

Starting at $119

Sound Blaster *Deluxe* ..... 2.0 lbs. $72
16 ASP ..... 4.0 lbs. $218
For Microchannel ..... Call Call
Sound Blaster Multimedia Upgd *Ext* ..... 13.5 lbs. $579
Internal ..... 14.0 lbs. $509
Sound Blaster Pro *Deluxe* ..... 3.5 lbs. $119
For Microchannel ..... Call Call
Video Blaster ..... 3.5 lbs. $324
Video Spigot *For Windows* ..... 4.5 lbs. $325

CTX

CTX Monitors *5439A 14" SVGA 39mm* ..... 31.0 lbs. $218
5468A 14" SVGA 28mm ..... 30.0 lbs. $259
5468LR 14" SVGA 29mm ..... 32.0 lbs. $289
5468NI 14" SVGA 28mm ..... 31.0 lbs. $288
5468NR 14" SVGA 28mm ..... 32.0 lbs. $299
CPS 1461LR 14" Multiscan 28mm ..... 31.0 lbs. $339
CPS 1560 15" Multiscan 28mm ..... 35.0 lbs. $418
CPS 1561LR 15" Multiscan 28mm ..... 32.0 lbs. $409

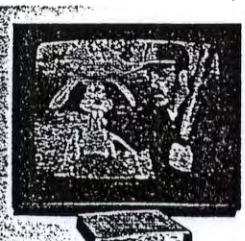
Diamond Computer Systems

SPEEDSTAR VIDEO CARD *24X 1MB* ..... 1.0 lbs. $115
Stealth Pro *1MB VLB* ..... 1.5 lbs. $257
1MB SVGA ..... 1.5 lbs. $249
2MB SVGA ..... 2.0 lbs. $339
Viper VLB 2MB SVGA *1280X1024NI* ..... 2.0 lbs. $409

Digital Vision

ComputerEyes/LPT Color *NTSC* ..... 2.0 lbs. $299
Pal ..... 2.0 lbs. $299
ComputerEyes/Pro *Color* ..... 1.5 lbs. $209
Color Pal ..... 1.5 lbs. $219
Color for Macintosh ..... 1.5 lbs. $269
Color Pal for Macintosh ..... 1.5 lbs. $279
Black & White For Macintosh ..... 2.0 lbs. $169
ComputerEyes/RT ..... 1.5 lbs. $299
Monochrome ..... 1.5 lbs. $209
Pal ..... 1.5 lbs. $289
TelevEyes VGA-to-TV Converter ..... 3.0 lbs. $208
Pal ..... 3.0 lbs. $215
TelevEyes/Pro ..... 4.0 lbs. $569

Digital Vision



TelevEyes/Pro

$569

DSG Communications

CALL Link for CallerID ..... 1.5 lbs. $184

Equinox

MegaPlex Kit *24 Port AT/EISA* ..... 7.5 lbs. $1379
RS6000 ..... 6.5 lbs. $1549

GalactiBoard ..... 1.0 lbs. $549
GalactiBox ..... 33.0 lbs. $1599

Hayes Microcomputer Products

Accura *Accura 96 With Fax* ..... 2.5 lbs. $198
Accura 144 w/Fax V.42bis Internal ..... 2.5 lbs. $195
Accura 144 w/Fax V.42bis External ..... 5.0 lbs. $219
OPTIMA *OPTIMA 24 + Fax96* ..... 6.0 lbs. $116
OPTIMA 96 V.32/42bis Modem ..... 3.5 lbs. $329
OPTIMA 144/SC V.42bis Modem ..... 3.5 lbs. $359
OPTIMA 144 + Fax 144 /SC EZ ..... 4.0 lbs. $378

Hewlett-Packard

Jet Direct Card *For NetWare* ..... 2.0 lbs. $375

IBM Corporation

Tape Backup *PS/2 Internal* ..... Call $77
Token Ring *Dual 16/4 AT Adapter* ..... Call $608
Dual 16/4 PS/2 Adapter ..... 1.5 lbs. $497
8228 MultiStation Access Kit ..... 8.0 lbs. $429
PC Network Cable - 8 Ft ..... 1.0 lbs. $23
LAN Support Software ..... 2.0 lbs. $47

Intel[2]

EISA Token Express 16/4 Card ..... 1.5 lbs. $675

Integrated Information Technology

IIT Math CoProcessors *2C87 12Mhz* ..... 0.5 lbs. $50
2C87 16Mhz ..... 0.5 lbs. $52
2C87 20Mhz ..... 0.5 lbs. $57
3C87 16Mhz ..... Call $54
3C87 20Mhz ..... Call $54
3C87 25Mhz ..... Call $54
3C87 33Mhz ..... 0.5 lbs. $59
3C87 40Mhz ..... 0.5 lbs. $62
3C87SX 20Mhz ..... 0.5 lbs. $54
3C87SX 25Mhz ..... 0.5 lbs. $55
3C87SX 33Mhz ..... 0.5 lbs. $59
3C87SX 40Mhz ..... 0.5 lbs. $59

InterActive Inc.[4]

Multimedia Business Comm Pack ..... 11.0 lbs. $484
SoundXchange *Model A* ..... Call $95
Model B ..... Call $185

IOMEGA

Bernoulli MultiDisks

Starting at $95

IOMEGA

90 MB Cartridge Tripak *5YR* ..... 1.5 lbs. $282
Additional IOMEGA Products ..... Call Call

Kensington Microware

Expert Mouse *Bus* ..... 2.5 lbs. $113
Serial ..... 2.5 lbs. $97
LaserStand ..... 19.5 lbs. $108
MasterPiece ..... 8.0 lbs. $83
MasterStand ..... 8.5 lbs. $54
MicroSaver *Security System* ..... 1.0 lbs. $45
Notebook Keypad ..... 1.0 lbs. $98
Turbo Mouse-MAC ..... 2.0 lbs. $105

LaserMaster

WinJet Upgrade *Upgrade 300* ..... 2.5 lbs. $187
800 ..... 3.5 lbs. $459

USA & CANADA **800-336-1166** INTERNATIONAL **216-494-8715**

INTERNATIONAL RESTRICTIONS (superscripted numbers following manufacturer name)

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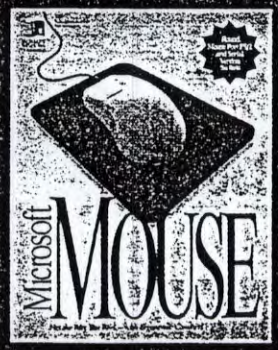
hardware

F

HARDWARE

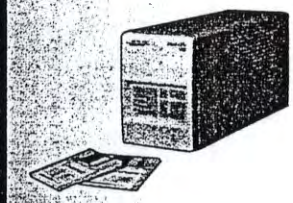
Microsoft® - New Mouse

Get your hands on the most comfortable Microsoft Mouse ever! Designed to meet the exacting ergonomic criteria, the Microsoft Mouse has tested superior to others for long-term comfort. Developed to enhance the Windows ™ operating system, the Microsoft Mouse is one of the most accurate pointing devices you can use. Hold the Mouse in either hand with equal comfort and support. The more you use it, the more task-efficient you become. The unique shape of the Microsoft Mouse gives enhanced support to the hand for long term ergonomic comfort.



$75

	Weight	Price
3com		
EtherLink II *8-Bit*	1.5 lbs.	$184
EtherLink II/16 Coax	1.5 lbs.	$154
EtherLink II/16 TP	1.5 lbs.	$164
EtherLink III	Call	Call
EtherLink/MC	1.5 lbs.	$264
LinkBuilder 12TP	5.0 lbs.	$379
Adaptec		
Disk Controller Kit	Call	Call
Advanced Digital Systems		
VGA TV Elite	Call	$259
American Power Conversion		
Back-UPS 250	15.5 lbs.	$98
Back-UPS 400	17.5 lbs.	$155
Back-UPS 450	26.5 lbs.	$188
Back-UPS 600	26.5 lbs.	$257
Back-UPS 900	52.0 lbs.	$359
Back-UPS 1250	60.0 lbs.	$479
Smart UPS 400	21.5 lbs.	$279
Smart UPS 600	31.0 lbs.	$329
Smart UPS 900	48.5 lbs.	$529
Surge Arrest Plus	2.5 lbs.	$29
Wallmount	1.5 lbs.	$20
With Telephone & 3 Outlets	1.5 lbs.	$34
With Telephone & 7 Outlets	2.5 lbs.	$49

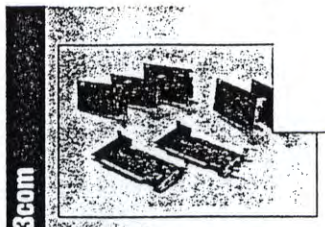


American Power Conversion

Smart UPS 600

$329

Ansel Communications		
All-In-One	Call	Call
Ethernet Adapter	Call	Call
ARTISOFT		
AE-2/T Ethernet Adapter	1.5 lbs.	$179
AE-3 Ethernet Adapter	1.5 lbs.	$218
Artisoft Central Station *LANtastic*	7.5 lbs.	$309
NetWare	8.0 lbs.	$372
Central Station II LANtastic	7.5 lbs.	$379
Central Station II NetWare	7.5 lbs.	$379
Asante		
Ethernet Cards for Macintosh	Call	Call
Boca Research		
Boca Modems *Internal 14,400 Baud V32*	2.0 lbs.	$168
External 14,400 Baud V42	4.5 lbs.	$149
Other Boca Modems	Call	Call
BocaBoard 16-Port Intelligent	5.0 lbs.	$389
Chinon America		
CDS-435 Internal 600MB CD-ROM Drive	6.0 lbs.	$314
Other CD-ROM Hardware	Call	Call
Colorado Memory Systems		
Jumbo Tape Drives *250 DJ-20 Tape Drive*	4.0 lbs.	$174
Trakker 120MB Backup	5.0 lbs.	$287
Trakker 250MB Backup	9.0 lbs.	$344
FC-10 Tape Controller	1.0 lbs.	$62
Jumbo DT-250 Cartridge	0.5 lbs.	$23
PowerTape	Call	Call
2GB Internal w/ SCSI Controller	7.0 lbs.	$948
2GB Tapes	1.0 lbs.	$45
4GB External w/ SCSI Controller	15.0 lbs.	$1585
4GB Internal w/SCSI Controller	7.0 lbs.	$1479
COMPUTERWISE		
BARCODE READERS *Wedge*	2.0 lbs.	$219
Serial	2.5 lbs.	$219
Creative Labs		
Discovery 16-bit CD-ROM *Int Double Speed*	Call	$429
External Double Speed	Call	$495
OmniCD	Call	Call



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2C87 20Mhz	0.5 lbs.	$57
3C87 16Mhz	Call	$54
3C87 20Mhz	Call	$54
3C87 25Mhz	Call	$54
3C87 33Mhz	0.5 lbs.	$59
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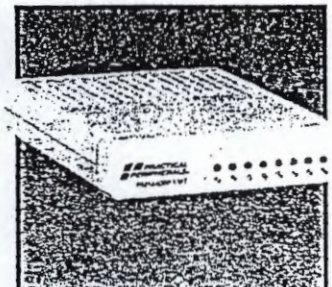
MicroTac Software
13380 *Spanish Assistant for Windows*—Gives you fast, understandable translations to or from Spanish, including powerful reference tools $54.95
13379 *French Assistant for Windows* 54.95
13378 *German* 54.95, 13377 *Italian* 54.95

Borland
11915 *Borland Office for Windows*—A power-packed combination of products that work together—WordPerfect 6.0, Quattro Pro 5.0 Paradox 4.5, Presentation Graphics Adviser & The Workgroup Desktop ... call
11978 *Competitive Upgrade* ..... call

Hewlett-Packard ... 1 year
12212 *LaserJet 4L (with toner)*— Four pages per minute and 300 dpi provides affordable laser-quality printing. Overnight freight charge is just $5! $699.95

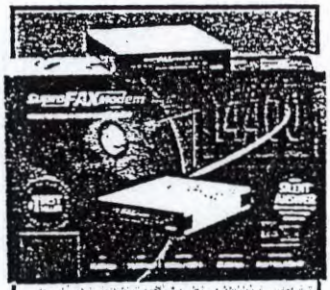
Zoom Telephonics ... 7 years
14763 *Zoom FaxModem VFP 28.8K*—Data throughput at 28,800 bps uncompressed (yes 28.8K) using the new V.Fast Class standard. V.32bis compatible with S/R fax at 14.4 Kbps *(internal)* $299.95

Delrina
2682 *The Far Side Daily Planner for Windows*—365 cartoons by Gary Larson and animation sequences plus a complete schedule planner ..... $39.
9853 *Opus 'n Bill Screen Saver*—A hilarious way to protect your screen ..... 29.



Practical Peripherals ... lifetime
10570 *PM14400EXMT*—V.32 14,400 data/fax modem with V.42bis data compression for throughput to 57,600 bps. $215.95
2425 *PM14400FX SA* 399.95
6123 *PractiCARD 144* 289.95

Norton-Lambert
2754 *Close-Up 5.0 Host & Remote*— Take control of PCs miles away by modem & run both Windows & DOS applications. For remote access to PCs & networks, file transfer, remote support & general communications $119.95



Supra Corporation ... 5 years
5252 *SupraFAXModem144LC*— 14,400 bps fax/data speeds with maximum 57,600 bps throughout. Simple LED lights track modem activity $149.95
11441 *SupraFAXModem144e* 209.95

Delrina
9853 Opus 'n Bill Screen Saver ..... $29.
Hewlett-Packard
8731 Dashboard 2.0 for Windows 46.95
MBS Technologies
12812 FileRunner Win. 1.4 *(3½" only)* 46.95
Microsoft
10154 Visual Basic 3.0 Win. Std. Edition 129.95
10437 Visual Basic 3.0 Win. Pro. Edition 319.95
11444 Visual C++ Std. Ed. *(3½" only)* 125.95
Pacific Microelectronics
13089 Mac-in-DOS for Windows 109.95
PC-Kwik
8004 Power Pak 3.1 w/Power Disk 45.95
Qualitas
12541 386MAX 7.0 *(3½" only)* 61.95
Quarterdeck
3217 QEMM 7.02 *(3221 5¼")* 63.95
Stac Electronics
1409 Stacker 3.1 ..... 95.95
Symantec
2360 Norton Desktop Win. *(2359 5¼")* 115.95
5136 The Norton Util. 7.0 *(3146 5¼")*. 115.95
8535 pcANYWHERE DOS 119.95
11303 pcANYWHERE Windows 129.95
6250 Speedrive 4.0 *(3½" only)* 65.95
TouchStone Software
11665 CheckIt Pro: Set *(Vols. I & II incl.)* 79.95

NETWORKING/COMMUNICATIONS

3 Com ... lifetime (conditional)
3453 EtherLink II/16 159.95 3469 TP 169.95
Asanté Technologies ... 5 years
2775 8 Port Hub 249.95
2772 12 Port Hub 499.95
Artisoft
2234 Lantastic AE-2 Start. Kit DOS 5.0 459.95
2452 AE-2 EtherNet Adapter Card 199.95
BOCA Research ... 5 years
8397 M1440I FaxModem 119.95
8398 M1440E FaxModem 149.95
Coactive Computing
14025 Connect. DOS & Win. 1.0 *(3½")*.. 134.95
1184 Coactive Connector Mac 29.95
14028 Starter Pack 1.0 *(3½" only)* 189.95
Data Storm
4798 PROCOMM PLUS 2.01 ..... 69.95
2006 PROCOMM PLUS 2.01 Windows ... 95.95
DataViz, Inc.
6508 Conv. Plus for Win. 1.0 *(3½" only)* $89.95
DCA/Crosstalk
5611 Crosstalk 2.0 for Windows 119.95
Delrina Technology
2446 WinFax PRO 3.0 ..... 79.95
5974 DOSFax PRO 49.95
Hayes ... 2 years
11396 ACCURA 144+FAX144 *(external)* 229.95
11397 ACCURA 144+FAX144 *(internal)*. 199.95
7395 OPTIMA 144+FAX144 ..... 389.95
8167 OPTIMA 144+FAX144 PCMCIA 309.95
Hilgraeve
12081 HypAcc. Win. 109.95 8204 DOS . 59.95
IBM
13207 Int. FaxModem *(P/N MOD531)*..... 49.95
Intel ... 3 years
2994 EtherExpress 16 or 3021 16 TP *ea.*.. 99.95
1531 FaxModem 14.4/14.4 *(int.)* 159.95
1536 FaxModem 14.4/14.4 *(ext.)*..... 179.95
5934 SatisFAXtion Modem/400 ..... 285.95
12931 14.4 PCMCIA FaxModem 299.95
8903 2400 bps Wireless Modem 649.95
Megahertz ... 5 years
10515 C5144 14.4 FaxModem *(Compaq)* 419.95
12763 XJ1144 14400 FaxMod. *(PCMCIA)* 319.95
Microcom
6234 CarbonCopy Plus 6.1 ..... 129.95
4410 CarbonCopy Plus Windows 129.95
Microsoft
5743 Windows for Workgroups 3.11 ... 144.95
6172 Windows for Workgroups *(single)* 47.95
Norton-Lambert
2754 Close-Up Host & Remote 5.0 ..... 119.95
Novell
12058 NetWare 4.01 *(10 user)* 1899.95
12056 NetWare 4.01 *(25 user)* 2799.95
Practical Peripherals ... lifetime
10570 PM14400FX MT $215.95
9234 PM14400FXPPM Pock. Fax/Mod. 359.95
2425 PM14400FX SA 399.95
6123 PractiCARD 144 (PCMCIA card) . 289.95
Shiva
NetMod/E Win. for Workgrps. *ea.*1439.95
Solectek
13083 AirLan Bridge 3449.95
Starter Kit *(ISA or MCA)* ..... *ea.* 1369.95
SupraFaxModems ... 5 years
5252 144LC... 149.95 11441 144e.... 209.95
Technology Concepts ... 2 years
6315 Fax Line Manager 203 ..... 124.95
Traveling Software
4407 LapLink V 99.95
U.S. Robotics
11923 Sportster 14.4 FaxModem Int. 159.95
11924 Sportster 14.4 FaxModem Ext..... 184.95
6631 WorldPort 14.4 PMCIA FaxMod.. 319.95
11922 WorldPort 14.4 Pocket FaxMod. 249.95
Zoom Telephonics ... 7 years
3386 FaxModem AFC 24/96/48 *(int.)*..... 49.95
9519 FaxModem VFP 24K *(internal)*.... 175.95
14763 FaxModem VFP 28.8K *(internal)*. 299.95
13172 14.4 FxM w/CoSession Rem. *(int.)* 134.95
13171 14.4 FxM w/CoSession Rem. *(ext.)* 169.95

VIDEO & SOUND

Adobe Systems ... 120 day MBG
12891 Premiere 1.0 for Win *(3½" only)* 179.95
Advanced Digital Systems
13985 VGA TV-Elite 249.95
Altec Lansing
12924 ACS50 Computer Speakers 69.95
12920 ACS300 Computer Speakers 279.95
Aristosoft, Inc.
6780 Wired for Sound Pro 2.0 ..... $39.95
ATI Technologies ... 5 years
12720 VGA Wonder GT 174.95
3886 Graph. Ult.+2 MB 249.95 3871 Pro 369.95
11022 Graphics Ultra Pro EISA *(w/2 MB)*. 399.95
Claris Clear Choice
13907 From Alice to Ocean *(Book & CD)*. 46.95
Creative Labs ... 1 year
5770 Sound Blaster 16 MCA ASP 209.95
Diamond Computer ... 5 years
1569 Stealth 24 VLB 159.95
1585 Viper VLB 399.95
Hauppauge
10598 Win/TV w/Microsoft Video Win... 419.95
IBM
13199 16 bit Audio Card *(P/N AC 523)*.. 169.95
Intel ... 3 years
11587 Smart Video Recorder 499.95
KOSS Corporation ... lifetime
11323 HD-4 speakers w/AC adapter 54.95
11700 HD-6 speakers w/AC adapter 79.95
Logitech ... 2 years
11462 SoundMan Super Pak 139.95
Media Vision ... 3 years
5637 ProAudio Spectrum 16 ..... 169.95
12028 ProAudio Studio 16 ..... 219.95
NEC MultiSync Monitors ... 2 years
11949 3FGE.... 629.95 11948 4FGE..... 749.95
Sony ... 1 year
6801 CDU-7811 Dbl. Speed CD-ROM.. 459.95
10530 CPD-1430 14" Multiscan Trinitron 629.95

INPUT/OUTPUT

Caere ... 1 year
4277 OmniScan *(w/OmniPage Direct)*. 289.95
Canon BubbleJet Printers ... 1 year
7809 BJ-200 315.95 9614 BJ-600 Color 599.95
CoStar ... 1 year
1814 LabelWriter II Plus 239.95
Epson ... 2 years
11800 LQ570+ *(80 col., 269 cps)*..... 269.95
10784 Action Laser 1500 *(2 MB)*..... 699.95
13110 Action Scanning System 849.95
Hewlett-Packard ... 1 year
6442 LaserJet 4 *(with toner)*..... 1479.95
12212 LaserJet 4L 699.95 13682 4P 1059.95
7620 DeskJet 550C 629.95

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SALES 603-446-0004 FAX 603-446-7791

software

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	Weight	Price
BayFront Cape Tools		Call $529
For Windows		Call $529
For UNIX		Call $615

BayWare

	Weight	Price
Power Japanese	2.0 lbs.	$219

Beacon Hill Software

	Weight	Price
10 Pack *for Windows*	1.0 lbs.	$40
SnapShot 3 *for Windows*	1.0 lbs.	$50

Beame & Whiteside Software

	Weight	Price
BW-NFS *For DOS*	4.0 lbs.	$289
10 User	3.0 lbs.	$1899
BW-NFS *For LAN WorkPlace*	1.5 lbs.	$189
BW-TCP *For DOS*	3.5 lbs.	$199

Berkeley Systems

	Weight	Price
After Dark	1.0 lbs.	$29
For Windows	1.0 lbs.	$27
For Macintosh	1.0 lbs.	$27
More After Dark *For Windows*	0.5 lbs.	$23

Bimillennium Corp

	Weight	Price
HiQ *For Macintosh*	6.0 lbs.	$899
For SUN SPARCStation	6.0 lbs.	$2199

BitWise Solutions

	Weight	Price
AutoBasiC Professional	3.5 lbs.	$165

Black Belt Systems

	Weight	Price
WinImages:Morph *For Windows*	1.0 lbs.	$119

Black Ice Software

	Weight	Price
ColorFax *For Windows*	1.0 lbs.	$79
Image SDK Plus *For Windows*	1.0 lbs.	$234
TIFF SDK *For Windows*	1.0 lbs.	$249

Blast Inc

	Weight	Price
BLAST *PC*		Call Call
Professional	3.0 lbs.	$89
Professional For UNIX	3.0 lbs.	$249
Professional Server	3.0 lbs.	$314
Additional Configurations		Call Call

Blink[2]

	Weight	Price
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	Weight	Price
INTERWORK	3.5 lbs.	$199
With C Source Code	3.5 lbs.	$1599
For UNIX or Xenix 386	4.0 lbs	$269
For UNIX or Xenix 386 With Source	4.0 lbs.	$1699
For Xenix 286	3.5 lbs.	$194
For Xenix 286 With Source	3.5 lbs.	$1589
INTERWORK *Professional*	5.0 lbs.	$539

Blue Sky Software

	Weight	Price
Magic Fields	1.0 lbs.	$309
QuickMENU	2.0 lbs.	$95
RoboHELP	1.0 lbs.	$437
WindowsMaker *Professional*		Call Call
WindowsMaker *Professional 32-bit*	4.0 lbs.	$849

BlueRithm Software

	Weight	Price
Aeris *For DOS or Windows 3.1*	9.5 lbs.	$105

Bluestone Consulting

	Weight	Price
Bluestone MWM	1.0 lbs.	$92
UIM/X	1.0 lbs.	$4399
UIM/Xtend *Editing*	1.0 lbs.	$225
UIM/Xtend *Widgets*	1.0 lbs.	$449

BonAmi Software

	Weight	Price
CPU Monitor Plus *For OS/2*	1.0 lbs.	$114

Borland International[2]

	Weight	Price
Beyond the World of C++ *Video*	3.0 lbs.	$95
~~Borland C++ & Applications Frameworks~~	~~22.5 lbs.~~	~~$450~~
Borland C++ 4.0		Call $315
Competitive/Version Upgrade		Call $175
Borland C++ *For OS/2*	8.5 lbs.	$315
Borland Client/Server Pack	15.0 lbs.	$649
Borland InterBase *For UNIX*		Call Call
2 Users		Call Call
10 Users		Call Call
Borland Office *For Windows*	22.0 lbs.	$219
Borland Pascal *With Objects*	15.5 lbs.	$316
Borland SQL Link *For Interbase*	1.0 lbs.	$48
For Oracle Server	1.0 lbs.	$92
For Microsoft/Sybase Server	1.0 lbs.	$92
Borland Visual Solutions Pack		Call $95
BRIEF *For DOS & OS/2*	3.0 lbs.	$87
dBASE Compiler *For DOS*	5.0 lbs.	$179
dBASE III Plus	7.0 lbs.	$434
dBASE IV	9.0 lbs.	$495
LAN License	2.0 lbs.	$273
Channel Upgrade	9.0 lbs.	$89
For UNIX	9.5 lbs.	$639
Learn Programming *Turbo Pascal Video*	2.0 lbs.	$45
ObjectVision	3.0 lbs.	$93
For OS/2	2.5 lbs.	$155
ObjectVision *PRO*	12.0 lbs.	$314
Paradox 4.5	9.5 lbs.	$489
LAN License	4.0 lbs.	$274
Special Upgrade	10.0 lbs.	$135
Paradox Development Edition *For Windows*		Call Call
Maintenance Kit	0.5 lbs.	Call
Paradox Dev Tools *For Windows*	6.5 lbs.	$165
Paradox Engine *& Database Frameworks*	3.0 lbs.	$195
Paradox *For Windows*	10.0 lbs.	$132
For Windows for Workgroup		Call $324
License Pack		Call $279
Paradox *Runtime for Windows*		Call Call

	Weight	Price
Paradox SQL Link *Netware*	1.5 lb	
For DB2	2.0 lb	
For Interbase	C	
For Oracle Server	C	
For Microsoft/Sybase Server	C	
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Special Upgrade	7.0 lb	
Quattro Pro	4.5 lbs.	$42
Quattro Pro 5.0 *For Windows Video*	1.0 lbs.	$27
Quattro Pro *For Windows*	7.0 lbs.	$42
LAN License	1.0 lbs.	$191
WorkGroup Edition	7.0 lbs.	$222
WorkGroup Edition Upgrade	4.0 lbs.	$87
Superpack 2.0 *For Windows*	2.0 lbs.	$155
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Turbo C++ 3.0	4.0 lbs.	$64
Turbo C++ *Visual Edition For Windows*	7.0 lbs.	$73
Turbo Pascal 7.0	6.5 lbs.	$98
Turbo Pascal *For Windows*	9.0 lbs.	$97
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World of Database Management *Video*	0.5 lbs.	$16
World Of Objects *Video*	0.5 lbs.	$17
World of ObjectVision *Video*	1.5 lbs.	$36
World of ObjectWindows *C++ Video*	2.5 lbs.	$89
World of ObjectWindows *Turbo Pas Video*	2.5 lbs.	$89

Boston Business Computing

	Weight	Price
EDT+ 6.0	1.5 lbs.	$229
LAN Configurations		Call Call

Brightwork Development

	Weight	Price
LAN Automatic Inventory *100 User*	1.5 lbs.	$319
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For Windows 100 User	1.5 lbs.	$329
For Windows 250 User	1.5 lbs.	$499
NETremote+ *DOS & Win 100 User*	2.0 lbs.	$314
DOS & Windows 250 User	2.5 lbs.	$624
PS-Print *100 User*	1.5 lbs.	$249
SiteLock *100 User*	1.0 lbs.	$314
SiteMeter *For Windows 100 Users*	1.5 lbs.	$329
250 Users	1.5 lbs.	$659

Building Block Software

	Weight	Price
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Personal With Source	3.5 lbs.	$569
Professional	3.0 lbs.	$669
Professional With Source	3.0 lbs.	$1289
CAD/CAM Developer's Kit/3D *Personal*	5.0 lbs.	$829
Personal With Source	5.0 lbs.	$1594
Professional	5.0 lbs.	$1445
Professional With Source	5.0 lbs.	$2849
CAD/CAM Developer's Kit/DXF *Personal*	3.0 lbs.	$389
Personal With Source	3.0 lbs.	$789
Professional	2.0 lbs.	$789
Professional With Source	3.0 lbs.	$1545

Burton Systems Software

	Weight	Price
TLIB *Version Control System*	1.5 lbs.	$99
DOS, OS/2 & Windows NT	1.5 lbs.	$128
5 Station LAN	2.0 lbs.	$299
5 Station LAN DOS, OS/2, & NT	1.5 lbs.	$404

BUZZWORDS INTERNATIONAL

	Weight	Price
dANALYST GOLD *SPECIAL*	1.0 lbs.	$69
WinGEN *For Windows*	1.0 lbs.	$129
For Windows NT	1.0 lbs.	$209
For OS/2	1.0 lbs.	$129
Add-On Engine Support	0.5 lbs.	$89

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		195
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10 User		Call Call
25 User		Call Call

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	Weight	Price
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c_pslib	1.0 lbs.	$135

C::napse

	Weight	Price
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With Source Code	1.0 lbs.	$259

CADKEY

	Weight	Price
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	Weight	Price
Eagle PCB Software *AutoRouter Module*		Call Call
Schematic Module		Call Call
Layout Editor 16-Bit		Call Call

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Professional	3.5 lbs.	$585
Professional for Macintosh		Call Call
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Plus For Windows	2.0 lbs.	$389

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CSC Chemfinder *For Macintosh*	3.0 lbs.	$395
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CSC ChemOffice *For Macintosh*	4.0 lbs.	$779
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	Weight	Price
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ZIP Colorkit	0.5 lbs.	$65

CDP Consultants

	Weight	Price
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For Networks	1.0 lbs.	$199

Celect Software

	Weight	Price
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	Weight	Price
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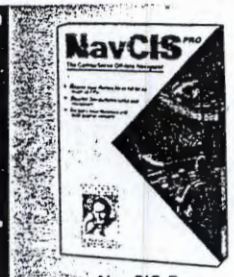

NavCIS Pro

$70

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eNOTE		Call	Call
Additional configurations		*Call*	*Call*

Eclipse Systems

Eclipse FAX for Windows		1.5 lbs.	$63

Ecosoft

Microstat-II		1.5 lbs.	$249
Microstat III For Windows		*Call*	Call

EditPro

EditPro *For Windows*		3.0 lbs.	$219

Enable Software

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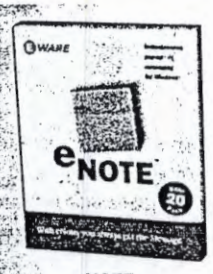

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For Windows		4.5 lbs.	$829
International Customers		*Call*	Call

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FairCom

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Spread/VBX		2.0 lbs.	$219
Spread/VBX++ for C++		3.0 lbs.	$219

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RDBMS Network		3.0 lbs.	$819

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Fleet & Partners

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GRAF/DRIVE PLUS *Developers Edition*		1.0 lbs.	$174
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Foundation Microsystems[2]

Schedule Express		1.0 lbs.	$89

Fourth Wave Technologies

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Fractal Design Painter *For Windows*		2.0 lbs.	$254

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FrameMaker *For Windows*		*Call*	$559
Upgrades		*Call*	Call

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SerialTest *Async*		2.5 lbs.	$239

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Frye Utilities *NetWare Management*		3.0 lbs.	$329
Additional Server License		2.5 lbs.	$249
Frye Utilities *Software Update & Distrib*		3.0 lbs.	$629
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FTP PC/TCP TCP/IP		5.5 lbs.	$319
5 Pack		9.0 lbs.	$1199
10 Pack		17.5 lbs.	$2249
20 Pack w/Support		11.5 lbs.	$3319
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For DOS & Windows w/Interdrive		5.5 lbs.	$319
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Funk Software

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FutureSoft

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TN3270		5.0 lbs.	$279
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X.25 Software Option		1.0 lbs.	$809
Additional Add-Ons		*Call*	Call

Galacticomm

The Major BBS

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Gazelle Systems

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10 User		*Call*	$264

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GCP++ *Visual Basic Custom Controls*		1.0 lbs.	$179
Customers Outside US & Canada		1.0 lbs.	$274
GCP++ *WINSOCK SDK*		1.0 lbs.	$354
Customers Outside US & Canada		1.0 lbs.	$539

Genus Microprogramming

GIF Developer's Pak		7.0 lbs.	$879
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GIF Developer's Pak/16		7.0 lbs.	$1074
GIF Developer's Pak/16 with Source		7.0 lbs.	$2164
GIF Toolkit		3.5 lbs.	$184
With Source Code		4.0 lbs.	$429
GIF Toolkit/16		4.0 lbs.	$214
GIF Toolkit/16 with Source		4.0 lbs.	$464
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With Source Code		3.0 lbs.	$279
GX Effects/16		3.0 lbs.	$169
GX Effects/16 With Source		4.0 lbs.	$319
GX Effects *For Windows*		4.0 lbs.	$185
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GX Games		1.0 lbs.	$47
GX Graphics		4.0 lbs.	$178
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GX Graphics/16		3.5 lbs.	$229
GX Graphics/16 with Source		4.0 lbs.	$549
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GX Images *For Windows*		4.0 lbs.	$365
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With Source Code		3.0 lbs.	$504
GX Printer/16		4.0 lbs.	$289
GX Printer/16 with Source		4.0 lbs.	$549
GX Text		2.5 lbs.	$112
With Source Code		3.0 lbs.	$243
GX Text/16		3.0 lbs.	$150
GX Text/16 with Source		4.0 lbs.	$299
PCX Developer's Pak		7.5 lbs.	$874
With Source Code		7.0 lbs.	$1929
PCX Developer's Pack/16		*Call*	Call
PCX Developer's Pack/16 With Source		7.0 lbs.	$2094

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- Weight: 2.94 Lbs.
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- NiMH Battery & AC Pack
- Suspend/Resume Feature
- 1 PCMCIA Type II Slot
- EZ Point™ Integrated Pointer
- 78-Key Keyboard
- Parallel, Serial & PS/2 Ports
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HANDBOOK 486SX-25

With 25MHz 486SX CPU and 80MB Hard Drive

$1495

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$1995

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Traveler's Packs:

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- NiMH Battery & AC Pack
- Simultaneous Video with 1MB
- 79-Key Keyboard & Mouse
- 9600/2400 Fax/Modem
- 1 Parallel, 1 Serial Port
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- 2 Labtec® Speakers
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Only with system purchase.

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Gateway 2000 is a corporate sponsor of GLOBAL RELEAF

SOFTWARE & EXTRAS

If a system comes with "choice of application software," choose one of the following packages:

- Microsoft Excel for Windows™
- Microsoft Word for Windows™
- Microsoft Word and Bookshelf '92,® CD-ROM Edition
- Microsoft PowerPoint for Windows™
- Microsoft Project for Windows™
- The Entrepreneur Pack (Works,™ Publisher,™ Money™ & games)
- Borland Paradox® database and Quattro® Pro for Windows spreadsheet
- Microsoft Access™ for Windows

With desktop and selected portables you also get the following software and extras at no additional charge:

- MS-DOS 6.2 & Windows for Workgroups 3.11
- CoSession™ Host Remote Diagnostics (with all modems)
- Kiplinger's™ CA-Simply™ Money
- QAPlus Diagnostics
- Gateway Computer Glossary
- Gateway Mouse Pad

Systems with CDs also include:

- Gateway System CD with Microsoft Multimedia Pack™
- Multimedia On-Line User's Guide
- Gateway Mall On-Line Catalog

SERVICE

Every Gateway system is backed by:

- 30-Day Money-Back Guarantee
- One-Year Limited Warranty
- Lifetime Toll-Free Technical Support
- On-Site Service Available To Most Locations
- Lifetime BBS Membership
- FaxBack Automated Fax Service

Our money-back guarantee does not include shipping. On-site service is provided at no charge during warranty if our technicians determine it is necessary. If you'd like to read our warranty and guarantee policies, please call for a free copy.

intel inside

Basis of Estimate

M: Quote from a firm with whom BBN gets a bulk rate for photo artwork. Quantity 24 arises from the expectation of doing two layouts for each of the three boards (items N, O, and P), using 4 film plots per (half are copies).

N, O, P: Based on a prior project: It is the central thrust of this project to develop the enabling technology for radio modems that operate at microwatt power levels.

The three boards (items N, O, and P) are all instances of such radio modems. In item N, the modem takes the form of a PCMCIA card that can be plugged into a PDA (or a laptop computer acting as a surrogate for a PDA). In items O and P, the modems are primarily for laboratory experiments, although, once working, they can be used for demonstration purposes also.

Since the components are not known at this time but are likely to be small quantities of commercially standard components, we can only give engineering estimates of the modest costs of these boards based on having previously created small boards ("PSIO boards") at a similar level of complexity. Item N is slightly more expensive, since it is based on a premade PCMCIA board.

Q: Engineering Estimates

Since this is still early in the evaluation phase, we are anticipating that we may not have some sensitive test equipment that may be needed to perform some of the tests.

R: Engineering Estimates

Due to the nature of this program, we may not have foreseen all of the design issues we may come across. Therefore, some miscellaneous hardware may need to be purchased.

Post-it™ brand fax transmittal memo 7671 | # of pages ▸ 1

To	Sheila King	From	Steve Alaimo
Co.	BBN	Co.	Advance Repro
Dept.		Phone #	685-2911
F			

advance reproductions corporation

VER, MA

TO

M

Quotation #: 072292SPA1

Date of quote: July 22, 1993

Reference: Photoplotting

Terms: Net 30

FOB: North Andover

Price firm for: 1 Year

Shipment Date: 4 - 24 Hours

Quoted by: Stephen P. Alaimo

BBN Communications
70 Fawcett Street
Cambridge, MA 02138

Attn: Jan Stevenson

We appreciate your inquiry and are pleased to quote the following:

ITEM #	QTY	DESCRIPTION	UNIT PRICE	AMOUNT
		Generation of photoplots from Gerber plot files utilizing 4 MacDonald Dattwiler photoplotters.		
		1/4 Mil Resolution		
		20x24 film plots		$ 37.50
		20x26 film plots		$ 41.25
		24x30 film plots		$ 56.25
		24x36 film plots		$ 75.00
		32x36 film plots		$112.50
		NOTES		
	*	The above photoplotting prices reflect a 25% discount off of Advance Reproductions Corp. published price list.		
	*	Capable of merging multiple files on one plot at no extra charge.		
	*	Free pick-up and delivery.		
	*	Same day service available at no extra charge.		
	*	1/8th mil resolution available.		

This quotation and purchaser's acceptance thereof include all the above terms and conditions and those shown on the reverse side hereof. We hope we may be favored with your order.

N, O, P

Pathfinder PSIO Parts Quotation Summary

BBN Part Number	Part Name	Part Description	Manufacturer	Quantity per Unit	Extended Cost per Unit at Quantity: 1	50	120	100	Minimum Order Qty.
4013930-02	8054.	ALB	SEIKO	1	$0.59	$0.59	$0.59	$0.59	
45XXXXX-01	CS82C52_PLCC	16MHZ, PLCC,PE	HARRIS	1	$28.95	$23.85	$21.65	$21.65	
5322522-01	CAPACITOR	0.22UF,50V,SMT		15	$13.33	$4.80	$2.00	$1.33	3000 @0.08
530000-180	CAPACITOR	18PF,50V,SMT		2	$0.72	$0.26	$0.22	$0.22	100 @0.13
5221427-01	CAPACITOR	22UF,20V,TANT,SMT		1	$13.33	$4.80	$2.00	$1.33	500 @0.48
5221426-01	CAPACITOR	47UF,10V,TANT,SMT		2	$13.33	$4.80	$2.00	$1.33	500 @0.48
65XXXXX-01	CRYSTAL (SERIES)	7.3728MHZ,HC49S	FOX S/073	1	$8.33	$3.00	$1.50	$1.50	100 @1.50
5821411-01	DIODE_SCHOTTKY	IN5818		2	$0.46	$0.46	$0.42	$0.42	
42XXXXX-01	DS2401	SILICON SERIAL NO.	DALLAS SEMI	1	$1.75	$1.40	$1.20	$1.20	
7160014-01	CONN4_MOLEX_M_RA	CGRID,MALE,RA 70553-0003	MOLEX	1	$0.75	$0.75	$0.75	$0.75	
4013925-01	LM34DZ	TEMP. SENSOR	NATIONAL	2	$2.02	$1.98	$1.98	$1.98	
4013963-01	LM385BYZ	2.5V VOLTAGE REFERENCE	NATIONAL	1	$12.50	$4.50	$2.25	$2.25	100 @2.25
4021386-01	LT1111	SO DC/DC CONV.	LINEAR TECH.	1	$2.65	$2.65	$2.65	$2.65	
41XXXXX-01	LTC491CS	SO,PE	LINEAR TECH.	1	$19.86	$7.15	$3.25	$3.25	110 @3.25
41XXXXX-01	MAX222CWN	SOL,PE	MAXIM	1	$2.45	$2.45	$2.45	$2.45	
4521396-01	PSIO_68HC11	68HC811E2	MOTOROLA	1	$13.51	$13.51	$13.51	$13.51	
4420747-01	*PSIO_GLUE	PAL16V8_CMOS	ATMEL	1	$4.00	$3.60	$3.15	$2.90	
310251-101	RESISTOR	100,1/4W,SMT		2	$12.50	$4.50	$1.88	$1.25	5000 @0.045
300241-104	RESISTOR	100K,1/8W,SMT		4	$0.56	$0.20	$0.12	$0.12	200 @0.05
300241-103	RESISTOR	10K,1/8W,SMT		4	$0.56	$0.20	$0.12	$0.12	200 @0.05
300241-106	RESISTOR	10M,1/8W,SMT		1	$0.56	$0.20	$0.08	$0.06	200 @0.05
300241-102	RESISTOR	1K,1/8W,SMT		3	$0.56	$0.20	$0.15	$0.09	200 @0.05
300241-203	RESISTOR	20K,1/8W,SMT		3	$0.56	$0.20	$0.15	$0.09	200 @0.05
300241-393	RESISTOR	39K,1/8W,SMT		2	$0.56	$0.20	$0.10	$0.10	200 @0.05
300241-472	RESISTOR	4.7K,1/8W,SMT		1	$0.56	$0.20	$0.08	$0.06	200 @0.05
5005796-01	RES_SIP_BUS_10_PIN	22K 4310R-101-223		3	$2.00	$1.44	$0.90	$0.81	
6421418-01	TRANSFORMER	CTX50-1,SMT	COILTRONICS	1	$6.68	$4.40	$3.78	$3.78	
1123084-01	PSIO BARE BOARD	1.6"x3.0" PCB w/break tabs		1	$44.00	$27.00	$18.00	$16.00	
1123084-01	PSIO BARE BOARD	CONFORMAL COAT (SILICONE)		1	$2.59	$1.69	$1.28	$1.24	
1123084-01	PSIO BARE BOARD	NRE		1	$525.00	$525.00	$525.00	$525.00	
1123084-01	PSIO BARE BOARD	TEST		1	$450.00	$450.00	$450.00	$450.00	
			Total Parts Cost per Unit:		$210.21	$120.98	$88.22	$83.03	
			Total Parts Cost plus PCB NRE & Test:		$4,758.73	$7,024.18	$11,560.86	$15,920.16	

E. Brian Kallia, 10/28/93

EBK 10/28/93

DIGITAL ARTS GROUP

(S)

January 25, 1994

Charlie Reeves

BBN, Incorporated
70 Fawcett Street
Cambridge, MA 02138

Dear Mr. Reeves,

Digital Arts Group is pleased to present a price quote for a Senior RF Engineer. The price range would be $45.00 /hr - $60.00 /hr.

If we can be of further assistance please call me.

Sincerely,

DIGITAL ARTS GROUP

Helen I. Alpin
Vice-President

HIA/wd

• 270 Cambridge Street • Burlington, MA 01803 • (617) 273-2780 • FAX: (617) 273-5592

DD 1861

CONTRACT FACILITIES CAPITAL COST OF MONEY	Form Approved OMB No. 0704-0267 Expires Oct 31, 1989
1. CONTRACTOR NAME BBN Systems and Technologies, a Division of BBN	2. CONTRACTOR ADDRESS 10 Moulton Street Cambridge, Ma 02138
3. BUSINESS UNIT Laboratories	
4. RFP/CONTRACT PIIN NUMBER BAA 93-27	5. PERFORMANCE PERIOD 04/01/94 - 09/30/95

6. DISTRIBUTION OF FACILITIES CAPITAL COST OF MONEY

POOL	ALLOCATION BASE	FACILITIES CAPITAL COST OF MONEY	
		FACTOR	AMOUNT
Direct Labor	207,749	.01039	2,159
G & A	488,981	.00118	577
Labs Computer Center	20,001	.01893	379
		.00000	0
		.00000	0
		.00000	0
		.00000	0
		.00000	0
		.00000	0
		.00000	0
		.00000	0
		.00000	0
		.00000	0
		.00000	0
		.00000	0
TOTAL			3,114
TREASURY RATE			5.500%
FACILITIES CAPITAL EMPLOYED (TOTAL DIVIDED BY TREASURY RATE)			56,620

7. DISTRIBUTION OF FACILITIES CAPITAL EMPLOYED

	PERCENTAGE	AMOUNT
LAND	25.5%	14,438
BUILDINGS	21.3%	12,060
EQUIPMENT	53.2%	30,122
FACILITIES CAPITAL EMPLOYED	100.0%	56,620

DD FORM 1861, Aug 87 *Supersedes all previous editions of DD Forms 1861-1 and 1861-2 which are obsolete*

SUBCONTRACTING PLAN GOALS SUBMITTED UNDER
BOLT BERANEK AND NEWMAN, INC.
SUBCONTRACTING MASTER PLAN
IN ACCORDANCE WITH PUBLIC LAW 95-507

1. BBN Proposal No.: P94-LABS-C-002A

2. Contractor Name: Bolt Beranek and Newman Inc.

3. Name of individual completing plan: John Forcucci
(617) 873-3365

4.

	Total Estimated Cost of Prime Contract		Total Estimated Cost of Subcontracts	
	$717,753 over 18 months		$111,111	
	Percentage Goals of Prime Contract		Percentage Goals of Total Subcontracts	
Small Business	$47,656	6.7%	$47,656	42.9%
Small Disadvan Business	$8,017	1.1%	$8,017	7.2%

5. The above goals, submitted in accordance with BBN's Annual Small Business and Small Disadvantaged Business Subcontracting Master Plan, include both Direct Goals and Indirect Goals.

Bolt Beranek and Newman, Inc.

By: John Forcucci
John Forcucci
Small Business Liaison Officer

Date: 9 February 1994

BBN SYSTEMS AND TECHNOLOGIES

February 2, 1995

Advanced Research Projects Agency, ESTO
3701 N. Fairfax, Drive
Arlington, VA 22203-1714

Attention: Dr. Kaigham Gabriel
(703) 696-2252

Subject: BodyLAN Technical Report
Contract No. DABT63-94-C-0017
BBN Reference No. 11592 – BodyLan –

Dear Dr. Gabriel:

Enclosed is the BodyLAN Technical Report covering the period July 2 through January 31st, 1995 on the subject contract.

If you have any questions, or require any additional information, please do not hesitate to contact the undersigned at (617) 873-4579.

Sincerely,

Julio Escobar

Dr. Julio Escobar
Senior Scientist

cc: ARPA/ESTO/CSTO/SSTO/ASTO
ARPA/S&IO
ARPA/Technical Library
B. Bolling
T. Blackadar
M. DiBlasio

JE/ro

7 February 1996

Directorate of Contracting
Post Office Box 748
Fort Huachuca, AZ 85613-0748

Attention: ATZS-DKO-I
Ms. Barbara Van Doren
(602) 538-0412

Subject: Transfer of Government-owned Equipment

Reference: (1) Contract No. DABT63-94-C-0017
BodyLAN: A Wireless, Body Local Area Network
BBN Reference No. 11592

(2) Contract No. DABT63-95-C-0013
TIA Voice Map
BBN Reference No. 11683

Dear Ms Van Doren:

BBN Systems and Technologies ("BBN") requests authorization to transfer the equipment identified below from reference (1) to Fort Huachuca Contract reference (2).

Asset No.	Description	Serial No.
DABT63-0017-002B	101-Keyboard	81740742

This equipment was originally purchased by the Government for use on the referenced (1) Contract. Its use is no longer required.

Fort Huachuca referenced (2) Contract has a need for the above equipment and by transferring this equipment, we can fulfill that need at no additional cost to the Government.

Therefore, in addition to requesting the above transfer, BBN also requests a Rent-Free Blanket Right of Use Agreement covering the interim period until the transfer has been completed.

The Contracting Officer for Contract Reference (2) is William DiGiovanni. Should you need to speak with him, he can be reached at (602) 533-1347.

Should you require further information or if you have any questions, please contact Kristin Ross, Property Administrator at (617) 873-2656.

Sincerely
BBN SYSTEMS AND TECHNOLOGIES
Marguerite D. DiBlasio
Marguerite I. DiBlasio
Senior Representative, Contract Relations

cc: W. DiGiovanni, Ft. Huachuca
C. Shine, ACO
B. Kalita
L. Sher
C. O'Connor
K. Ross

DEPARTMENT OF THE ARMY
UNITED STATES ARMY INTELLIGENCE CENTER AND FORT HUACHUCA
FORT HUACHUCA, ARIZONA 85613-6000

REPLY TO
ATTENTION OF

April 8, 1996

Directorate of Contracting
Operations Division-Intel

BBN Systems and Technologies
Attn: Marguerite DiBlasio
10 Moulton Street
Cambridge, Massachusetts 02138

Dear Ms DiBlasio:

The Pathfinder Medical program has deliverables which are to be transferred from the Pathfinder contract to the U.S. Army Institute of Environmental Medicine, (USARIEM) Natick, MA 01760.

As design and test is completed, each deliverable will be fully transferred to USARIEM and will be removed from the Pathfinder contract.

This letter authorizes delivery of such equipment.

Delivery of equipment will be the responsibility of BBN and all costs related to the delivery of the equipment shall be at no cost to the Government.

Toni L Davies

TONI L. DAVIES
Contracting Officer

707
Mal

ATZS-DKO-I (715h)

AUG - 8 1994

MEMORANDUM FOR Mel Chernow, U.S Army Intelligence Center, ATTN: ATZS-CDT-T, Fort Huachuca, AZ 85613-6000

SUBJECT: Designation of Contracting Officer's Representative (COR) for Advanced Research Projects Agency Contracts

1. Pursuant to the authority vested in me by AFARS 42.9001, I hereby designate you COR for the contracts highlighted at enclosure 1. You shall exercise strict adherence to the instructions set forth herein. All personnel engaged in contracting and related activities must conduct business dealings in a manner above reproach and shall protect the U.S. Governments interest and maintain its reputation for fair dealings with contractors. While the Contract Officer has the legal responsibility for contract administration, certain portions of this authority may be delegated to a COR. The COR is responsible to the Contracting Officer and close communication should be maintained.

2. The limitations and scope of your authority are contained in AFARS subpart 42.9002 and TRADOC Pamphlet (encl 2) entitled "Guide for Contracting Officer's Representatives." Further information on COR responsibilities/duties can be obtained in the DOD 5500.7-R Joint Ethics Regulation, August 1993 and AFARS 3.101. A checklist on your specific COR responsibilities/duties is provided in this letter (encl 3).

3. Signing the COR letter constitutes certification that the regulations stated above have been read and understood. Your COR files must be kept current. A copy of this letter shall be placed in said file.

4. You shall thoroughly familiarize yourself with the terms and conditions of the contract.

5. A Contractor's Quarterly Progress Report (see Appendix C, encl 2) shall be prepared and submitted to this office within 10 calendar days following the end of the reporting quarter. Deficiencies, delinquencies, or problems noted should be identified (contractor must be immediately advised of these problems) and all related correspondence summarized and referenced therein. Upon completion of the contract or termination of your appointment, whichever occurs first, you shall prepare and forward to this office, one copy of the Contractor's Performance Evaluation Form 40-R (encl 4).

6. Your instructions and directions to the contractor shall be thoroughly documented. Verbal instructions and directions shall immediately be reduced to writing and placed in your files. Copies of all correspondence with the contractor shall be furnished to the undersigned with the Contractor's Quarterly Progress Report. Each communication to the contractor shall contain the following statement: "This instruction/direction/clarification shall in no way affect the price, delivery, quantity, or quality under the terms of the contract." Each file referred to herein is a part of the contract administration files. These files shall contain only one copy of each document. Your file shall bear the legend and disposition instruction as follows: 715K Contract Actions (FORWARD TO CONTRACTING OFFICER UPON COMPLETION).

7. The instructions, directions, and contract clarifications given to the contractor shall not be:

a. contrary to the contract, statutory or regulatory authority or,

b. in conflict with command policies and guidance.

8. As an agent to the Government, you should be aware that the authority delegated herein shall not be redelegated. If you depart from your authority, you may become personally liable for any additional costs incurred by Government.

9. Government property in the possession or control of the contractor or subcontractor (consisting of Government furnished property (GFP) and/or contractor acquired property (CAP) vests with the Government) is the total responsibility of the contractor. It is a contractor's responsibility to maintain the official Government contract records of such property (unless an exception has been authorized due to special circumstances) in accordance with provisions of the GFP clause of the contract and subpart 45.5 of the AFARS. You may be assigned additional responsibilities by the Contracting Officer. If no duties are assigned, you shall have direct responsibility to report promptly to me any loss, damage, destruction, or abuse of contract Government property which comes to your attention.

10. If the contract contains DD Form 254, Contract Security Classification Specification, and requires access to Sensitive Compartmented Information (SCI) then Secure Environment Contracting (SEC) procedures apply to the contract. As COR, you are responsible for ensuring classified deliverables are IAW the contract SOW and terms and conditions. **As part of your required COR reports, you will specifically certify acceptance of classified deliverables with a statement as follows: "Deliverables are in**

ATZS-DKO-I
SUBJECT: Designation of Contracting Officer's Representative (COR) for Advanced Research Projects Agency Contracts accordance with the technical requirements of the contract."

11. Should you receive directions or orders from chiefs of staff sections, commanders, or any person not in the contract administration chain of command, which you consider to be contrary to these instructions, you shall notify the undersigned immediately.

12. Termination of the above designation, without prejudice to any action taken thereto, shall be effective upon satisfactory completion of the above referenced contract unless terminated sooner in writing.

13. All correspondence or reports concerning this contract will be addressed to the undersigned at: Directorate of Contracting, ATTN: ATZS-DKO-I, P.O. Box 748, Fort Huachuca, AZ 85613-0748.

14. If there are any questions or doubts concerning your authority in any particular area, please contact the undersigned at (602) 533-1398. This will obviate the possibility of exceeding your authority and preclude any embarrassing situation which may result therefrom.

15. In accordance with AFARS 42.9004(a), request you acknowledge receipt of this designation letter, and return the original to the Contracting Officer.

Patricia Woznick

Encls

PATRICIA WOZNICK
Contracting Officer

RECEIPT AND ACKNOWLEDGEMENT

I hereby acknowledge receipt of my letter of appointment and fully understand my responsibilities as COR.

10 Aug 94
Date

Contracting Officer's Representative

REQUEST/CHECKLIST FOR COR DESIGNATION	DATE	CONTRACT NO.
	8 August 94	See ENCL 1
THRU:	TO: (CONTRACTING OFFICER) PATRICIA WOZNICK	
NOMINEE/ADDRESS AT25-CDT-T TELEPHONE: 538-2319 MAL Chernow	VICE TELEPHONE:	

RECOMMENDED DUTIES (SCOPE):

[X] 1. Issue written interpretations of the technical requirements of Government drawings, designs, specifications or statements of work.

[X] 2. Review the contractor's efforts to ensure the contractor is meeting the technical requirements and intent of the contract.

[X] 3. Ensure that the contractor is not arbitrarily enlarging the scope of the contract/delivery schedules, thereby obligating the Government to defray unanticipated costs (cost-type contracts).

[X] 4. Review contractor's proposals and advise the Contracting Officer of their technical adequacy, correctness, and reasonableness of work estimates and costs, and assure there is no duplication of work or cost.

[ ] 5. Review the contractor's make-or-buy program to determine technical necessity for subcontracts and reasonableness to work estimates and costs.

[ ] 6. Certify as to contractor's progress.

[X] 7. Notify the Contracting Officer in writing of deficiencies observed during surveillance of the contractor's performance and direct appropriate action to effect correction. Record and report to the Contracting Officer any incidents of faulty work performed by the contractor.

[X] 8. Furnish technical advice to the Contracting Officer for the purpose of establishing a basis for certifying payment of allowable costs under cost reimbursement contracts.

[X] 9. Assist designated Government inspectors or the Contracting Officer in the test, evaluation, inspection of items, programs, or systems to include final acceptance of deliverables.

(Continued on Reverse)

CONTRACTING OFFICER APPROVAL:

Encl 3

[X] 10. Contact the source of supply for Government-furnished property and ensure that such property is available when required.

[X] 11. Monitor property and **security matters** as requested by the appointed property administrators, security officers, or the Contracting Officer.

[X] 12. Monitor quality control and report discrepancies to the Contracting Officer.

[X] 13. Certify that selected material, supplies, and services are necessary and of the quality contemplated by the contract.

[X] 14. Review tasking for the contractor to ensure that the requirement is within the existing scope of work and coordinate with the contractor accordingly.

[ ] 15. Certify receipt/acceptance of equipment or services received from third party contractors. Such certification shall be effected by completion of DD Form 250, DD Form 1155, or other appropriate document.

[X] 16. Other duties:

a. Serves as proponent point of contact for all users of this contract.

b. Reviews and monitors any classified deliverables for compliance with terms and conditions of the contract and compliance with any security issues.

Statement of Qualifications. Cite those which substantiate the qualifications to perform as a COR such as:

1. COR course attendance (TRADOC COR Guide, para 2-4)

2. Previous experience as a COR.

3. Knowledge of the product or services under contract.

SEE ATTACHED

CONTRACTOR'S PERFORMANCE EVALUATION
(CCAI 715-1)

CONTRACTOR Bolt, Beranek and Newman (BBN)

CONTRACT NUMBER DABT63-94-C-0017

CONTRACTING OFFICER'S REPRESENTATIVE Dana E. Beach

NOTE: This evaluation serves as a historical record of the contractor's overall performance and may have a bearing on award of future contracts to the firm. Cite any significant factors, both positive and negative, which you feel should be brought to the attention of the Contracting Officer.

DESCRIPTION OF CONTRACT REQUIREMENT

Develop and demonstrate a micropower, wireless Body-area LAN.

DELIVERY ANALYSIS

Quarterly R&D Status reports submitted per contract.

GOVERNMENT-FURNISHED EQUIPMENT (DELIVERY AND CONDITION)

N/A

CONTRACTOR'S QUALITY CONTROL PROGRAM

N/A

PERFORMANCE OF CONTRACTOR'S PERSONNEL ASSIGNED TO THE CONTRACT

Principal Investigator - Philip Carvey: Excellent

CONTRACTOR'S PERFORMANCE OF TEST AND EVALUATION PROGRAM

N/A

CONTRACTOR'S ABILITY TO UNDERSTAND SCOPE OF THE TECHNICAL REQUIREMENTS

Excellent. Low power requirements reflected throughout project.

ANALYSIS OF CONTRACT'S VALUE ENGINEERING PROGRAM

N/A

OVERALL PERFORMANCE APPRAISAL (IF OUTSTANDING OR UNSATISFACTORY, FURNISH DETAILS)

Excellent.

RECOMMENDATIONS (SHOULD CONTRACTOR BE CONSIDERED FOR FUTURE AWARDS)

Contractor should be considered for future awards.

FOR

12/29/94
DATE

FILE COPY

ATZS-CDS 24 October 1994

MEMORANDUM FOR Chief, Science and Technology Office

SUBJECT: COR Visit to BBN, Contract #DABT63-94-C-0017, Cambridge, MA, Wireless Body-area Lan

1. Purpose: The purpose of this visit was to receive a briefing on the status of the research outlined in the proposal and contract.

2. Attendees: The meeting at BBN was scheduled for 19 October, and was a one-on-one session with the Principal Investigator, Philip Carvey. Mr. Carvey had presented a status report at the July WAMIS PI meeting in Virginia, and I introduced myself as the COR at that time.

3. Objective: The goal of BBN, under this contract, is to develop and demonstrate a micropower, wireless Body-area Lan allowing communications between multiple "Personal Electronic Accessories" (PEAs) and a "Personal Digital Assistant" (PDA). Preliminary PEAs include: health sensors; ring sensors (magnetic and gravitational fields, acoustic rangefinder); sports training aids; wristwatch display; microphone; ear speakers.

4. Summary:

a. Characteristics of BodyLan: short-range wireless communications; ultra low power consumption; spatial reuse; unobtrusive; compliance with FCC part 15; small lightweight; reasonable cost; flexible bandwidth assignment; autonomous operation.

b. When Mr. Carvey gave his presentation in July, the project was still primarily conceptual. During the past three and a half months BBN has made considerable progress in the hardware designs and coding, and it is apparent that the low power requirement for BodyLan is reflected throughout.

5. Action Items: None.

6. POC for this action is the undersigned, (602) 538-2373.

Dana E. Beach, COR
Science & Technology
Office

cc:
ATZS-DKO-I

ATZS-DKO-I (715h)

AUG - 8 1994

MEMORANDUM FOR Dana Beach, U.S Army Intelligence Center, ATTN: ATZS-CDT-T, Fort Huachuca, AZ 85613-6000

SUBJECT: Designation of Contracting Officer's Representative (COR) for Advanced Research Projects Agency Contracts

1. Pursuant to the authority vested in me by AFARS 42.9001, I hereby designate you COR for the contracts highlighted at enclosure 1. You shall exercise strict adherence to the instructions set forth herein. All personnel engaged in contracting and related activities must conduct business dealings in a manner above reproach and shall protect the U.S. Governments interest and maintain its reputation for fair dealings with contractors. While the Contract Officer has the legal responsibility for contract administration, certain portions of this authority may be delegated to a COR. The COR is responsible to the Contracting Officer and close communication should be maintained.

2. The limitations and scope of your authority are contained in AFARS subpart 42.9002 and TRADOC Pamphlet (encl 2) entitled "Guide for Contracting Officer's Representatives." Further information on COR responsibilities/duties can be obtained in the DOD 5500.7-R Joint Ethics Regulation, August 1993 and AFARS 3.101. A checklist on your specific COR responsibilities/duties is provided in this letter (encl 3).

3. Signing the COR letter constitutes certification that the regulations stated above have been read and understood. Your COR files must be kept current. A copy of this letter shall be placed in said file.

4. You shall thoroughly familiarize yourself with the terms and conditions of the contract.

5. A Contractor's Quarterly Progress Report (see Appendix C, encl 2) shall be prepared and submitted to this office within 10 calendar days following the end of the reporting quarter. Deficiencies, delinquencies, or problems noted should be identified (contractor must be immediately advised of these problems) and all related correspondence summarized and referenced therein. Upon completion of the contract or termination of your appointment, whichever occurs first, you shall prepare and forward to this office, one copy of the Contractor's Performance Evaluation Form 40-R (encl 4).

6. Your instructions and directions to the contractor shall be thoroughly documented. Verbal instructions and directions shall immediately be reduced to writing and placed in your files. Copies of all correspondence with the contractor shall be furnished to the undersigned with the Contractor's Quarterly Progress Report. Each communication to the contractor shall contain the following statement: "This instruction/direction/clarification shall in no way affect the price, delivery, quantity, or quality under the terms of the contract." Each file referred to herein is a part of the contract administration files. These files shall contain only one copy of each document. Your file shall bear the legend and disposition instruction as follows: 715K Contract Actions (FORWARD TO CONTRACTING OFFICER UPON COMPLETION).

7. The instructions, directions, and contract clarifications given to the contractor shall not be:

a. contrary to the contract, statutory or regulatory authority or,

b. in conflict with command policies and guidance.

8. As an agent to the Government, you should be aware that the authority delegated herein shall not be redelegated. If you depart from your authority, you may become personally liable for any additional costs incurred by Government.

9. Government property in the possession or control of the contractor or subcontractor (consisting of Government furnished property (GFP) and/or contractor acquired property (CAP) vests with the Government) is the total responsibility of the contractor. It is a contractor's responsibility to maintain the official Government contract records of such property (unless an exception has been authorized due to special circumstances) in accordance with provisions of the GFP clause of the contract and subpart 45.5 of the AFARS. You may be assigned additional responsibilities by the Contracting Officer. If no duties are assigned, you shall have direct responsibility to report promptly to me any loss, damage, destruction, or abuse of contract Government property which comes to your attention.

10. If the contract contains DD Form 254, Contract Security Classification Specification, and requires access to Sensitive Compartmented Information (SCI) then Secure Environment Contracting (SEC) procedures apply to the contract. As COR, you are responsible for ensuring classified deliverables are IAW the contract SOW and terms and conditions. **As part of your required COR reports, you will specifically certify acceptance of classified deliverables with a statement as follows: "Deliverables are in**

ATZS-DKO-I
SUBJECT: Designation of Contracting Officer's Representative (COR) for Advanced Research Projects Agency Contracts accordance with the technical requirements of the contract."

11. Should you receive directions or orders from chiefs of staff sections, commanders, or any person not in the contract administration chain of command, which you consider to be contrary to these instructions, you shall notify the undersigned immediately.

12. Termination of the above designation, without prejudice to any action taken thereto, shall be effective upon satisfactory completion of the above referenced contract unless terminated sooner in writing.

13. All correspondence or reports concerning this contract will be addressed to the undersigned at: Directorate of Contracting, ATTN: ATZS-DKO-I, P.O. Box 748, Fort Huachuca, AZ 85613-0748.

14. If there are any questions or doubts concerning your authority in any particular area, please contact the undersigned at (602) 533-1398. This will obviate the possibility of exceeding your authority and preclude any embarrassing situation which may result therefrom.

15. In accordance with AFARS 42.9004(a), request you acknowledge receipt of this designation letter, and return the original to the Contracting Officer.

Patricia Woznick

4 Encls

PATRICIA WOZNICK
Contracting Officer

RECEIPT AND ACKNOWLEDGEMENT

I hereby acknowledge receipt of my letter of appointment and fully understand my responsibilities as COR.

8/10/94
Date

Contracting Officer's Representative

REQUEST/CHECKLIST FOR COR DESIGNATION	DATE 8 Aug 94	CONTRACT NO. See ENCL 1
THRU:	TO: (CONTRACTING OFFICER) PATRICIA WOZNICK	
NOMINEE/ADDRESS DANA Beach ATZS-CDT-T TELEPHONE: 538-2373	VICE TELEPHONE:	

RECOMMENDED DUTIES (SCOPE):

[X] 1. Issue written interpretations of the technical requirements of Government drawings, designs, specifications or statements of work.

[X] 2. Review the contractor's efforts to ensure the contractor is meeting the technical requirements and intent of the contract.

[X] 3. Ensure that the contractor is not arbitrarily enlarging the scope of the contract/delivery schedules, thereby obligating the Government to defray unanticipated costs (cost-type contracts).

[X] 4. Review contractor's proposals and advise the Contracting Officer of their technical adequacy, correctness, and reasonableness of work estimates and costs, and assure there is no duplication of work or cost.

[ ] 5. Review the contractor's make-or-buy program to determine technical necessity for subcontracts and reasonableness to work estimates and costs.

[ ] 6. Certify as to contractor's progress.

[X] 7. Notify the Contracting Officer in writing of deficiencies observed during surveillance of the contractor's performance and direct appropriate action to effect correction. Record and report to the Contracting Officer any incidents of faulty work performed by the contractor.

[X] 8. Furnish technical advice to the Contracting Officer for the purpose of establishing a basis for certifying payment of allowable costs under cost reimbursement contracts.

[X] 9. Assist designated Government inspectors or the Contracting Officer in the test, evaluation, inspection of items, programs, or systems to include final acceptance of deliverables.

(Continued on Reverse)

CONTRACTING OFFICER APPROVAL:

Encl 2

X	10. Contact the source of supply for Government-furnished property and ensure that such property is available when required.
X	11. Monitor property and **security matters** as requested by the appointed property administrators, security officers, or the Contracting Officer.
X	12. Monitor quality control and report discrepancies to the Contracting Officer.
X	13. Certify that selected material, supplies, and services are necessary and of the quality contemplated by the contract.
X	14. Review tasking for the contractor to ensure that the requirement is within the existing scope of work and coordinate with the contractor accordingly.
	15. Certify receipt/acceptance of equipment or services received from third party contractors. Such certification shall be effected by completion of DD Form 250, DD Form 1155, or other appropriate document.
X	16. Other duties: a. Serves as proponent point of contact for all users of this contract. b. Reviews and monitors any classified deliverables for compliance with terms and conditions of the contract and compliance with any security issues.

Statement of Qualifications. Cite those which substantiate the qualifications to perform as a COR such as:

1. COR course attendance (TRADOC COR Guide, para 2-4)

2. Previous experience as a COR.

3. Knowledge of the product or services under contract.

SEE ATTACHED

********** -COMM[redacted]URNAL- ********** DATE JUL-07-20[redacted] **** TIME 10:57 *********

MODE = MEMORY TRANSMISSION START=JUL-07 10:56 END=JUL-07 10:57

FILE NO.=408

STN NO.	COMM.	ABBR NO.	STATION NAME/TEL NO.	PAGES	DURATION
001	OK	[redacted]	67036962200-869424	002/002	00:01:05

-USAIC FH -

********** -ATZS RMM - ***** - 520 533 1195- **********

DRM COVER SHEET

DSN 821-2288/CML (520) 533-2288
FAX--DSN 821-3102 or 821-1195
CML (520) 533-3102 or 1195

Kelly
Here's another
FY5 you can pull
T10 A8411
$ 9889.28

USAG, FORT HUACHUCA
DIRECTORATE OF
RESOURCE MANAGEMENT
Fort Huachuca, AZ

TO: Kelly FAX: _____

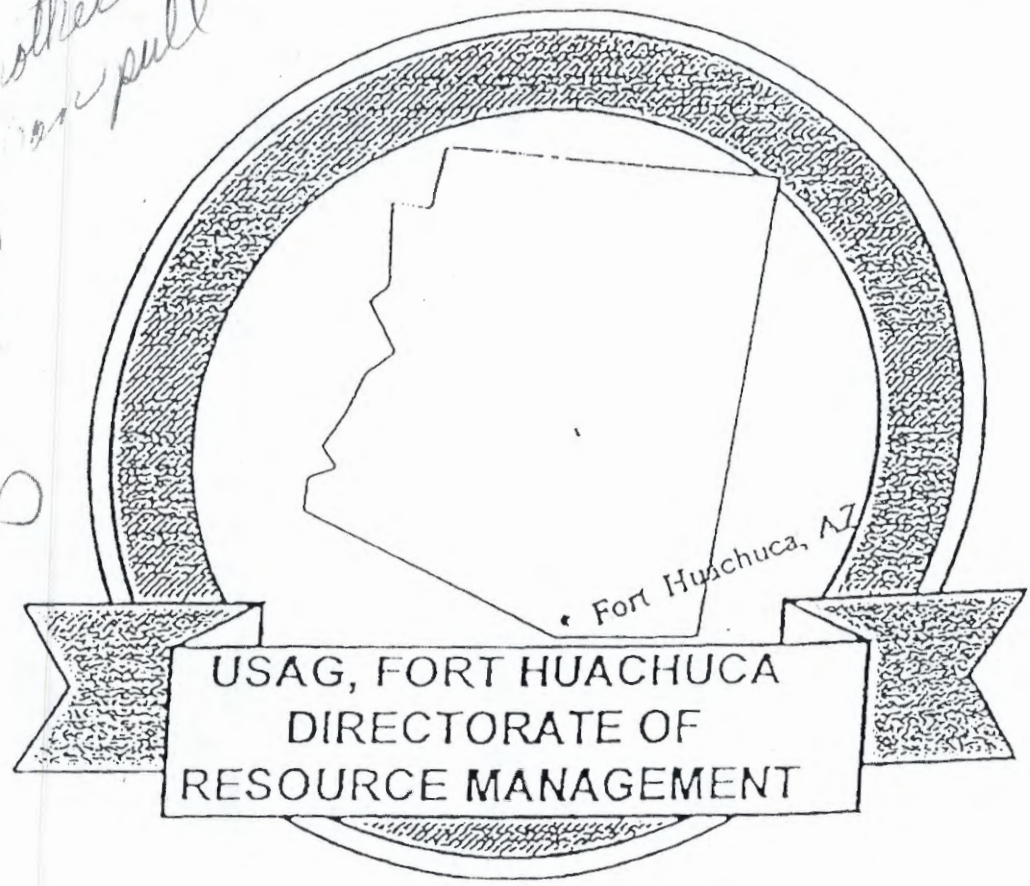
FROM: Clara

TELE: Pgs 4+1

DRM COVER SHEET

DSN 821-2288/CML (520) 533-2288
FAX--DSN 821-3102 or 821-1195
CML (520) 533-3102 or 1195

Kelly
Here is another one pull
FY5 Ya...
TIO A84111
$ 9889.28



TO: Kelly FAX: _____

FROM: Clara

TELE: Pgs 41

BBN Technologies
Contract Closeouts
87 Fowcett Street
Combridge, MA

24 Mar 99

FAX COVER SHEET

TO: **Francie Mills, Fort Huachuca**
Phone: (520) 533-0932
Fax: (520) 533-1195

FROM: **Pat Murphy, BBN Technologies**
Phone: (617) 873-3056
Fax: (617) 873-4857

RE: Contract # DABT63-91-C-0038 BBN Ref # 11404/2731
Contract # DABT63-94-C-0017 BBN Ref # 11592

Number of pages, including cover sheet: 2

Deor Francie,

As you requested, attached is a copy of the letter I sent to Liz Amatulli a week ago.

If you have any additional questions or concerns, please contact me at the number noted above.

Sincerely,

Pat Murphy
Contract Closeouts

Latest funds for A12001 + 91C001 as of 3/15
Will Pat Murphy + left msg for her to call me.

March 17, 1999

Attention: Ms. Liz Amatulli
Procurement Technician
Department of the Army
United States Army Intelligence Center
Fort Huachuca, Arizona 85613-6000

Subject: **Contract # DABT63-91-C-0038**
BBN Ref # 11404/2731
Contract # DABT63-94-C-0017
BBN Ref # 11592

Reference: Fax received March 11, 1999 containing copy of letter dated August 22, 1996

Dear Ms. Amatulli:

This is to confirm your request concerning close out of the above referenced contracts. The most recent year for which we have final negotiated overhead rates is fiscal year 1995. The performance period of the referenced contracts include costs through fiscal year 1997.

BBN has elected not to close out any contracts on a basis other than rates agreed to with DCAA. When such rates are settled, final vouchers will be issued. However, since we do not anticipate having final rates for fiscal years 1996 & 1997 in the immediate future, you may choose to have your contract closed out using our submitted rates (quick closeout). If this is what you wish to have done, please forward a written request for quick closeout of both of these contracts to my attention.

Should you have any further questions, please feel free to call me at (617) 873-3056.

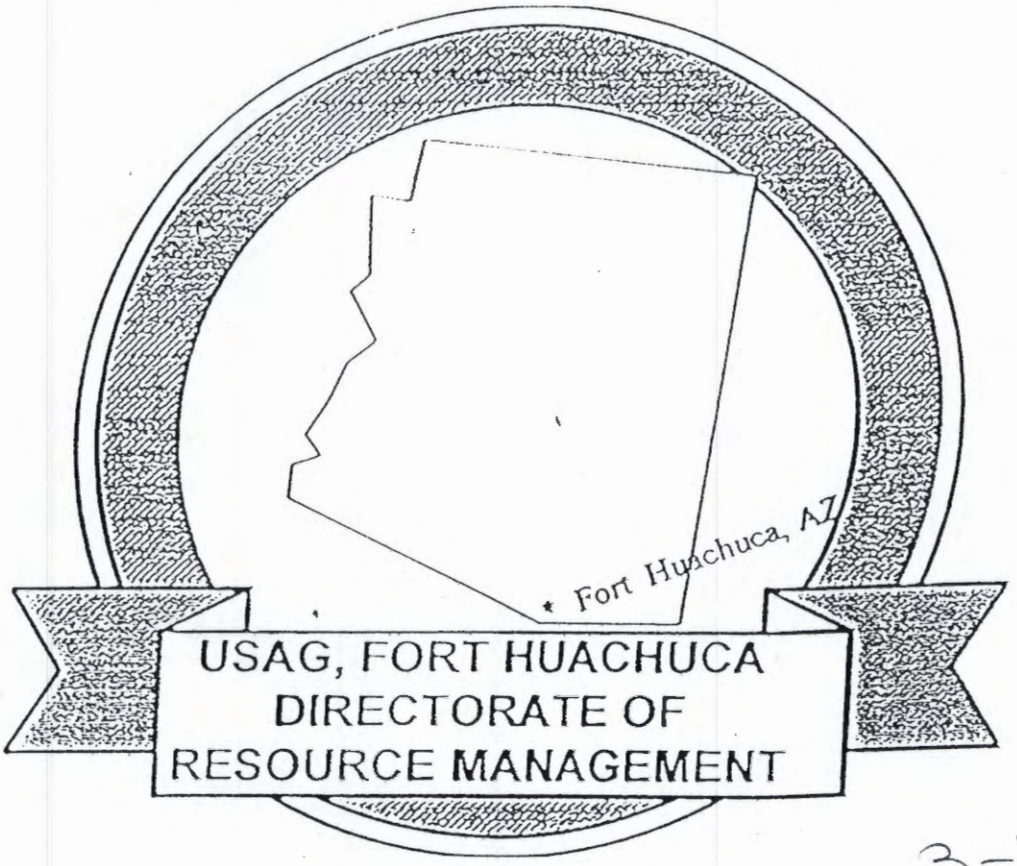
Sincerely yours,

Patricia F. Murphy
BBN Technologies
Contract Closeouts Supervisor

cc: file

DRM COVER SHEET

DSN 821-2288/CML (520) 533-2288
FAX--DSN 821-3102 or 821-1195
CML (520) 533-3102 or 1195



3-11-99

TO: M Dreblow FAX: 617-873-6091

FROM: FRANCIE MILLS

TELE: 520-533-0932 Pgs 2

FAX 520-533-1195

DEPARTMENT OF THE ARMY
UNITED STATES ARMY INTELLIGENCE CENTER AND FORT HUACHUCA
FORT HUACHUCA, ARIZONA 85613-6000

REPLY TO
ATTENTION OF

August 22, 1996

Directorate of Contracting
Operations Division - Intel

SUBJECT: Request For Final Audit

Defense Contract Audit Agency
10 Causeway Street, Room 253
Thomas O'Neal Federal Building
Boston, Massachusetts 02222-1033

Dear Sir/Madam:

This office hereby requests that a final audit be started on Contract DABT63-94-C-0017 with Bolt, Beranek, and Newman, 10 Moulton Street, Cambridge, MA 02138. The contract was completed on 31 July 1996.

Point of contact is the undersigned if further information is required. Telephone is (520) 533-1398/Facsimile 538-0415.

Sincerely,

Liz Amatulli

Liz Amatulli,
Procurement Technician

also, request was asked for 91-C-0038, same company!

=>

02/24/00 LXG - NSFOP - CLARA BILLOCK PAGE 1A
09:29:08 DETAIL

FY	APC	DOCUMENT	OBLIG	ACCRUAL	DISB
5	JWBL	HJ150042480535	$9,889.28-	$0.00	$0.00
	JWBL	HJ150043480535	$201,397.00	$191,507.72	$191,507.72
TOTAL FY 5					
			* $191,507.72 *	$191,507.72 *	$191,507.72
* GRAND TOTAL					
			* $191,507.72 *	$191,507.72 *	$191,507.72

---------- LAST PAGE ---------- =>

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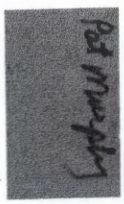

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43480535

CONDITIONS CAUSING REPORT

ACCRUAL GREATER THAN OBLIGATION
DISBURSEMENT GREATER THAN OBLIGATION AND/OR ACCRUAL
NEGATIVE OBLIGATION RECORDED

SOURCE FILE	BLK TAA	DO NUM VOUCHR	OBLIGATION AMOUNT	ACCRUAL AMOUNT	DISBURSEMENT AMOUNT	OBLIG DATE	ACCRU DATE	DISB DATE	FAC	ACR FNL	DSB FNL	L I	LED CODE	STAT FLAG
U/O			9,889.28-			0048	0000	0000	3			K	25	
TODAY DET	231	WWC	9,889.28-			0048	0000	0000	3			K	25	
TOTAL			9,889.28-			0000	0000	0000						

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03/09/00 NXG -- CURRENT MONTH HISTORY CLARA BILLOCK PAGE 1A
14:20:05 DETAIL

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					*	$9,889.28-		
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5	2581	JWBL	2	HJ150042480535	POOO5	$9,889.28	WW7	00055
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5	2581	JWBL	2	HJ150043480535	POOO5	$9,889.28-	WW7	00055
TOTAL TA 23								
					*	$0.00		

---------- MORE .... ---------- =>

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<PF5> NO TOTALS <PF6> STATS <PF7> BACKWARD <PF8> FORWARD
<PF9> GRAPH <PF10> SEND <PF11> LEFT <PF12> RIGHT

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03/09/00 NXG -- CURRENT MONTH HISTORY CLARA BILLOCK PAGE 2A
14:20:05 DETAIL

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TOTAL TA 40						*	$8,830.98		
* GRAND TOTAL						*	$17,661.96		

---------- LAST PAGE ---------- =>

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_1-Grand Total	.....	....	..		3339.76							0																	.....
_2-Grand MnHrs	.....	....	..		0.00							0																	.....
_3-SubTot Obl	.....	....	..		0.00							0																	.....
_4-SubTot Acc	.....	....	..		1669.88							0																	.....
_5-SubTot Exp	.....	....	..		1669.88							0																	.....
_6-SubTot Disb	.....	....	..		1669.88							0																	.....
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_7-SubTot TA23	.....	....	23		0.00							0																	.....
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Total records printed: 17

ATZS-CDT-STO 4 February 1994

MEMORANDUM FOR Director of Contracting, ATZS-DKO-I, (Gloria Bickler), US Army Intelligence Center and Fort Huachuca, AZ 85613-6000

SUBJECT: Acceptance of Proposal

1. The following listed Proposals are accepted in behalf of the Advanced Research Projects Agency:

TRW, Inc., Wireless, Adaptive and Mobile Information Systems Low Bandwidth Distributed Systems, dated July 9, 1993.

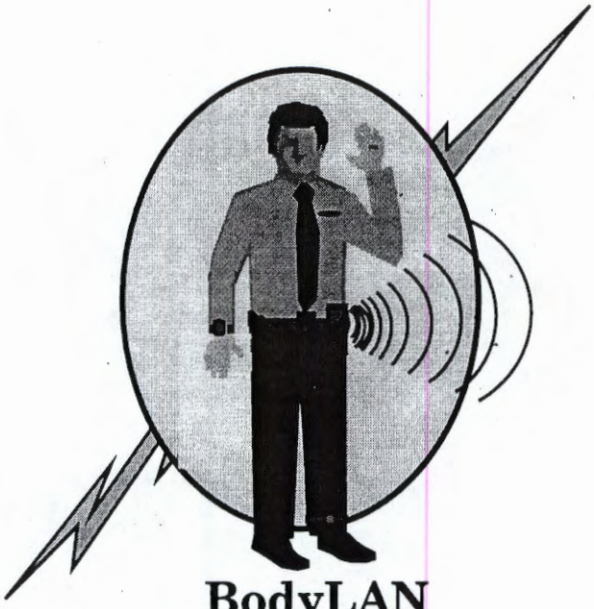
BBN, Body Lan, A Wireless Body Local Area Network, undated, (for accounting purposes this office has given the document a date of 4 February 1994).

2. Point of contact is the undersigned at 8-7500, FAX 8-7692.

ROBERT D. BOLLING
COR
Director, Science and Technology Office

BodyLAN

A Wireless, Body-Local Area Network



Principal Investigator:
Philip P. Carvey

Co-Principal Investigator:
Julio Escobar

Technical Report April 15 - July 1, 1994

Prepared For:

Advanced Research Projects Agency
Electronic Systems Technology Office
Contract No. DABT63-94-C-0017

TECHNICAL POINT OF CONTACT:

Philip P. Carvey
Bolt Beranek and Newman Inc.
10 Moulton Street
Cambridge, MA 02138
tel: (617) 873-3208
fax: (617) 873-3776
email: pcarvey@bbn.com

ADMINISTRATIVE POINT OF CONTACT:

Marguerite DiBlasio
Bolt Beranek and Newman Inc
10 Moulton Street
Cambridge, MA 02138
tel: (617) 873-3153
fax: (617) 873-3776
email: mdiblasio@bbn.com

I. Project Description

The overall goal of this research project is to develop the means for very-low-power wireless communications over a human body area. This development will comprise: the theoretical basis for the communications protocol, interface standards between body computer and modem, interface standards between sensor/transducer and modem, a prototype system demonstrating the technology, and a performance evaluation. Preliminary work done by BBN suggests that by using spread spectrum techniques and a communications protocol especially suited for low power implementation, wireless modems can be constructed occupying less than a 1000 cubic millimeters and consuming less than a hundred microwatts.

The key technical issues addressed in this project are:

- Operation at microwatt power consumption levels.
- Immunity to interference from similar and dissimilar wireless systems.
- Sub microsecond synchronization of all BodyLAN devices.
- Wireless operation in compliance with FCC Part 15 Regulations.

Motivation for this development is easy to find in both military and commercial applications, e.g. health sensors, special mission accessories, and training aids. Numerous sources have forecast that hip-worn computers, integrated with wired and wireless broadband networks, will fundamentally change the way people interact with their environment. Individuals will wear computers like clothing and jewelry. This evolution is not ten years out but is currently underway. Recently a "wearable computing" fashion show was presented in New York.

Apple Computer has named these computing devices, Personal Digital Assistants (PDAs) and has introduced an initial implementation called Newton. As technology evolves, there will be a steady evolution to smaller, lighter, and cheaper PDAs having more powerful processors, more storage, and seamless communication with the information infrastructure. The technology being proposed here may enhance this evolution. Bolt Beranek and Newman Inc. has trademarked this technology as "BodyLAN™".

We envision an environment in which a PDA would be worn on a soldier's hip or carried in a person's pocket. This PDA would not be used directly as are today's laptop computers; rather it would communicate with ultra-lightweight devices called Personal Electronic Accessories (PEAs). Routine interactions with one's PDA would be accomplished exclusively via these sensors/transducer PEAs. A PEA display device can be created today small enough to be worn like a wrist watch. Another PEA could include a gravitational and magnetic field sensor crafted to look like finger rings. These devices could be used to allow sign-language-like direct communications to the PDA. A PEA worn in the ear could give auditory feedback from the PDA. Low power health applications are too numerous to list.

Open standards for communication between PDA and PEAs (possibly from different vendors) are central to the success of this vision. Part of the proposed work is to:

- Formalize the BodyLAN communications architecture and develop a theoretical framework for its expected error rate under conditions of multiple near-field BodyLANs, narrow band jammers, and component aging.

- Produce a specification document describing the systems and hardware interface to the PEA modem, the interface to the PDA modem, and parameter initialization protocols.

- Build a digital PEA plus a pseudo random sequence generator/checker, a microprocessor-driven PDA modem, and an interface to one of the existing PDAs. All hardware will utilize existing RF, field programmable logic devices, and microprocessor components.
- Evaluate the robustness, ease-of-use, and performance of the prototype systems.
- Develop a plan for integrating the PEA and PDA modem functionality into a single IC.

1.1 Summary of Project

To any engineer who has struggled to comply with the Part 15 FCC specification limiting radiated emissions, sending a signal a few meters might seem trivially easy. For example, a 1-turn coil, 15 millimeters in diameter, having a 400 MHz, 20 milliampere sinusoidal current, generates an electric field of 2500 microvolts per meter at three meters distance. This signal is 19 times greater than the radiation allowed by the Part 15 specification. A receiver dipole of length 20 millimeters generates a voltage of 32 microvolts at that field strength, or 100 times that required by a low cost receiver. When antenna sizes are very small, higher frequency is a big win because of the cubic dependency of efficiency on frequency; the same example at 1200 MHz would result in a signal 27 times as large. The question is, "if it's so easy, why hasn't someone already done it?".

The answer to this question is that technology heretofore did not provide the motivation to look. With the emergence of wearable computers, wireless communications, and low cost, high frequency, high density semiconductor chips, we now can look into the practicality of a very-local-area, wireless network, the BodyLAN.

The radio frequency spectrum is crowded and highly regulated. More than 30,000 channels are licensed by the FCC just in the Northeastern part of the United States (under 1000 MHz). With the exception of the television bands, all these channels are narrow band FM. While the number of channels is very large, they are infrequently used. Only the FM radio, TV, and cellular radio bands are in constant use. Forty percent of the spectrum under 1000 MHz is dedicated to television. Of the 67 TV bands, only about 16-18 are typically occupied. Fire, police, amateur radio, and other bands are even less utilized.

For BodyLAN, we need to find a way to coexist with these licensed channels in such a way that the FCC will accept BodyLAN emitters and existing licensees will not object. Part 15 specifies bands under 1000 MHz in which emission can be intentional but of limited field strengths. Typical field strength maximums are 100 to 200 microvolts per meter at three meters. For the remaining bands (all the television bands for example), the FCC allows zero intentional emissions.

For long distance transmissions, narrow band FM benefits both receiver and transmitter--hence its popularity. The receiver benefits from the narrow band because it receives less noise from natural and man-made noise sources and only the licensee is allowed to transmit power in that band. Since a transmitter's cost is normally highly dependent on its peak power, sending continuously (i.e. narrow band) maximizes the energy per unit of information transmitted. Narrow band transmission incidentally maximizes the number of dedicated channels. This maximization of precious radio spectrum is one of the most important benefits of narrow band transmission.

For short distance unlicensed transmissions, as in BodyLAN, the benefits of narrow band FM disappear. In any narrow band, the receiver may find interfering signals from narrow-band transmitters (which we shall call jammers) and from other BodyLANs. A BodyLAN transmitter receives no cost reduction benefits from narrow-band operation because of the severe FCC limits on transmitted power. Accordingly, a new mode of operation now becomes desirable: pulsed operation (i.e. wideband), and, as described below, using a combination of AM and FM.

An emitter having a maximum field emission of 20,000 microvolts per meter pulsed one microsecond on and 99 microseconds off has an average field strength of 200 microvolts per meter. If a wideband receiver is synchronized to the transmitter and only samples the received signal when the transmitter is sending, then it "sees" a 20,000 microvolts per meter field, not the 200 microvolts per meter average.

An important advantage of short distance communications is the comparative ease of synchronization. Maximum PEA/PDA separation distance is expected to be less than 1.4 meters (55 inches) for a hip-worn PDA. This corresponds to less than 10 nsec of temporal uncertainty for a PEA anywhere within the 2.8 meter diameter sphere surrounding the PDA. If the RF pulses are on the order of 500 nanoseconds, none of the complexity associated with ranging must be implemented. In long distance communications, say 10 kilometers, the temporal uncertainty is 7,000 times larger. This requires either the data rates be kept unacceptably low or ranging compensation be incorporated.

Pulsed operation is desirable from a power conservation standpoint because transistors need large bias currents to obtain low noise, high gain, and high frequency operation. By employing fast startup linear circuits operating at low duty cycles, low power consumption is obtained.

Synchronization between PEAs and the PDA is the key to the entire BodyLAN concept. It is also the most challenging protocol problem to be solved. Principal requirements of a synchronization protocol are low power consumption, low complexity, the ability to quickly reacquire synchronization after losing synchronization, without disturbing other PEA/PDA communications, and sharing with data the single receiver in the PEA modem. From a power consumption standpoint, the PDA can expend only a small amount of its power consumption and transmitted power budget on synchronization.

There are several operational constraints in the use of PEAs which critically affect the architecture and protocols. The first and foremost is that PEAs employing BodyLAN modems be autonomous. A PEA owner must only be aware of two constraints: first PEA batteries become discharged and must be replaced or recharged, or the PEA be disposable, and second, PEAs must be in reasonable proximity to the home PDA. All other aspects such as synchronization, power management, initialization, error reporting, synchronization sequence changeover, etc, must be handled by the Finite State Machines in the PEAs and PDA. Since PEAs are intended to be very small, they do not have a keyboard, connectors, nor any other mechanism for conveying information to the PEA other than through BodyLAN. We assume even the initialization procedure which sets the PEA's personalization perameters is handled via the BodyLAN.

In use, PEAs of one BodyLAN must share the same physical volume of adjacent BodyLANs. We require that adjacent BodyLANs not interfere with one another catastrophically but will allow some increase in error rate. In normal operation, the PDA will monitor the received power level and error rates. It adjusts the transmitted power levels of itself and the PEAs to achieve the desired error rate. Thus PEAs close to the PDA would transmit at lower power levels than PEAs further away from the PDA. This power management tends to limit the effect of one BodyLAN on another. Moreover, the "FM Capture Effect" causes a receiver to completely "capture" the stronger of two FM signal having the same carrier frequency. This effect will also reduce the interference of adjacent BodyLANs.

For some geometries, the FM Capture Effect will work against us. Consider the case of BodyLAN-equipped persons A and B shaking hands with one another. If person A has a finger-ring PEA(A) on his outstretched hand, it would probably be closer to PDA(B) than say person B's PEA(B) ear microphone. This requires that the transmission protocol must allow a few relatively strong interfering BodyLANs and still maintain a prescribed error rate.

Figure 1 illustrates the BodyLAN system. The architecture relegates sensor and actuator functions to PEAs and processing functions to one PDA. This helps minimize the size and weight of the PEAs

which are typically worn on a non-load bearing part of the body (such as the fingers or in the ear). PCMCIA card implementing the BodyLAN hub modem plugs into the user's PDA. Control of tl BodyLAN is implemented in a low-power processor residing on this PCMCIA card. Applicatio interacting with the ensemble of PEAs are executed on the PDA.

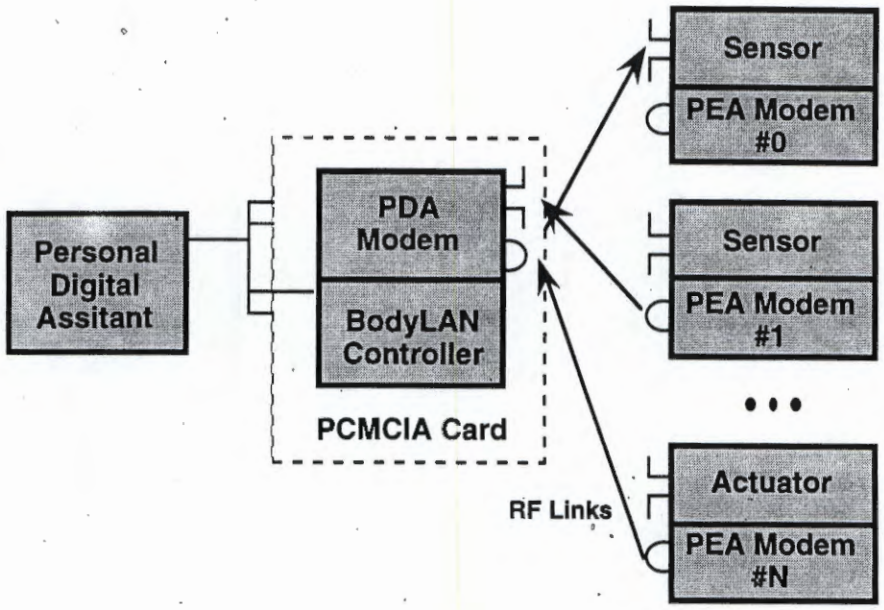


Figure 1 BodyLAN System

BodyLAN has a star topology where PEA modems can only communicate with the PDA modem not with each other. The current architecture supports full duplex communications at 32 Kb/s i each direction using Time Division Multiplexing Access (TDMA). Each 23 millisecond TDM "superframe" is composed of 768 bits. Each bit can be allocated to a PEA in two arbitrary lengt groups. Each group can be assigned to PEA->PDA or PDA->PEA communications. Thus eac PEA can receive data from the PDA in increments of 42 bits per second and can send data to th PDA in increments of 42 bits per second. To reduce power consumption and simplify the PE modem design, we require that a "PEA" not send and receive simultaneously. Thus the maximun aggregate bandwidth of any one PEA is 30Kb/s while that of the PDA modem is 64 Kb/s.

While a PEA modem supports both PDA->PEA and PEA->PDA communications capability, mos PEA applications are either one or the other. One exception is the ear PEA which, like a hearing aid "plugs" into the ear. It would have an antenna which slips around the ear and could also have a integrated microphone. Others, like finger ring PEAs which measure the arrival time of acousti bursts or the rings' orientations relative to the earth's gravitational and magnetic fields would use 3 4% of the PEA->PDA aggregate bandwidth. A 256 X 128 display device could be completel repainted in about two seconds using one-half the PDA->PEA bandwidth.

The BodyLAN architecture utilizes a 2.5 MHz-wide Pea->Hub sub-band in the 320-360 MHz ban and a 2.5 MHz-wide Hub->PEA sub-band in the 360-400 MHz band. A BodyLAN system ca dynamically select one of five sub-bands in each band to minimize interference. Synchronizatio beacons and Hub->PEA user data share the same sub-band.

Naturally occurring noise from the environment (i.e. from auto ignitions, electric motors transmission lines, etc.) and thermally generated noise acting alone should give us virtually error fre

channels and still comply with FCC maximum-power transmission requirements. Multiuser interference among adjacent BodyLANs and narrow-band jammers are expected to be the main source of channel errors. Our design uses spread spectrum communication with 64 chips per bit and Optically Orthogonal Codes (OOC) to combat these error sources. The combination of spread spectrum and OOCs not only reduces the error rate but also make it possible for us to meet FCC regulations and reduce power consumption.

1.2 Standardization

As illustrated in Figure 1, BodyLAN is composed of a PCMCIA card on which the BodyLAN control processor and the PDA modem are mounted, and several PEA modems integrated with their sensor/actuators. Firmware in the control processor will control all BodyLAN communication activities such as power management, initialization, error detection, and synchronization. We envision application code exclusively executing on the PDA's processor.

We envision the PDA component of BodyLAN as a generic component implemented on a PCMCIA card. This card would plug into a PDA of the user's choosing. It contains the PDA modem, a control processor with memory, and an interface to the PCMCIA bus. Processing power of the control processor is budgeted only to execute the communications activities of BodyLAN. It will process the data input from all PEAs, plus any external or application data fed to the PDA but not any transducer specific functionality. Thus standardization of the PDA component appears achievable. The diversity of PEA form factors and transducers will make standardization of the PEA component more difficult.

For the PEA component, we envision standardizing only the PEA modem portion of the PEA. To achieve some measure of standardization. we propose the interface between PEA modem and transducer as a full duplex serial communication with clock and a frame pulse sourced by the PEA modem. In addition, a low data rate full duplex overhead channel will also be provided to provide a communication path with the PDA processor.

We envision that the commercial version of the BodyLAN will require a single chip implementations of the PEA and PDA modems, to reduce size, weight, and power consumption. We propose however only to implement a multi-chip implementation of the modems using off-the-shelf chips to demonstrate feasibility of the BodyLAN concept and characterize the channel and operational properties.

1.3 Communication Channels

The choice of spectrum window must take into account naturally occurring noise, man-made noise, and FCC regulations. The 320 MHz to 400 MHz band, among others, is assigned to military aircraft. Other transmissions in this band are allowed as long as they do not exceed 200 microvolts per meter field strength at a distance of three meters, as measured by a quasi-peak detector. Since this detector has low pass filter properties (contrary to what its name implies), BodyLAN's spread spectrum signals make it possible to satisfy FCC regulations.

Channel errors will affect the quality or accuracy of the transducer connections. We expect the two major sources of channel errors to be multiuser interference among adjacent BodyLANs and narrow-band jammers. For multiuser interference, we have chosen spread spectrum signals known as Optical Orthogonal Codes. To reduce the effect of narrow band jamming, the RF pulses are transmitted at either of two frequency tones. The tones are 1.25 MHz above and below the center frequency of the band. Thus, the combined spread spectrum signal with a two MHz chip rate occupies approximately 2.5 MHz of spectrum.

BodyLAN's hierarchy of signals is shown in Figure 2. The figure shows the TDMA format with 6 frames per superframe, 128 slots per frame, one bit per slot, and 64 spread spectrum chips per bit. Six synchronization beacons are spred amongst 768 slots and repeated each superframe. The locations of these six beacons within a superframe form a codeword unique to each BodyLAN.

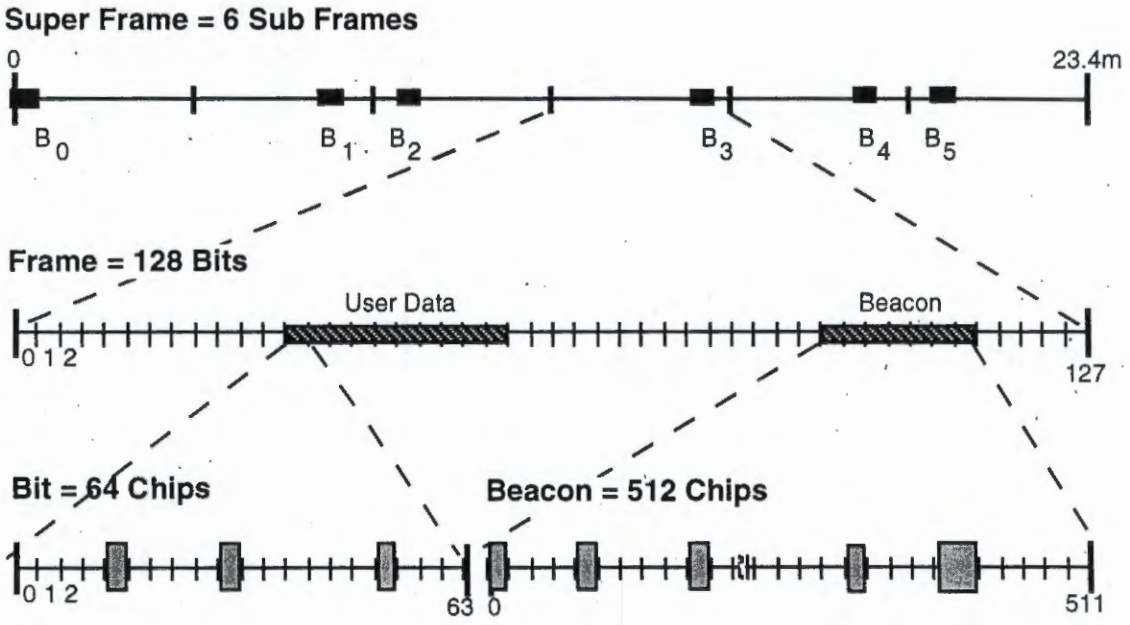


Figure 2 BodyLAN Superframe Format

1.4 Spatial Coexistence Among Adjacent BodyLANs

BodyLAN must operate within range of other BodyLANs. It uses spread spectrum transmissions to provide near-orthogonality among signals from adjacent BodyLANs. We have chosen a form of pulse-position spread spectrum signal known as Optical Orthogonal Codes (OOCs). OOCs are pulse patterns designed to have low cross-correlation among themselves (i.e. few pulse positions overlap for any shift of the codewords). Hence they are unipolar signals, i.e. symbols do not cancel out each

other in any sense, and use a sparse number of pulses in their spread spectrum chip sequence. When an RF pulse is transmitted, its "value" is either a one if the frequency is 1.25 MHz above the carrier or a zero if the frequency is 1.25 MHz below the carrier.

Choosing the OOC for BodyLAN is still ongoing. One problem with optimum OOCs is that they yield a high error rate when too few codewords are available. Ideally, we would like to assign a unique code word to each BodyLAN. Unfortunately, the number of codewords in a maximum size Optically Orthogonal Code is typically very small. In the (63,3,1) code, there are only 10 (module cyclic shifts) out of 1.84e19 possible codewords. An optimum (63,5,1) code has even fewer codewords. Increasing the correlation factor to two (i.e. any two code words can have two coincident pulse for an arbitrary shift) greatly increases the number of codewords (over 100) but still results in far fewer codewords than possible users. Cyclic shifts of the codewords, however, satisfy the same low cross correlation properties and hence can be used to our advantage (see Section 4.8).

1.5 Synchronization

Synchronization of PEAs to the PDA is accomplished by the PDA periodically broadcasting beacons on the Hub->PEA frequency band. Six beacons are transmitted in each 768-slot superframe, one in each frame but starting at bit positions which are quasi-unique to each BodyLAN. Each beacon is a 512-chip OOC having 38 separate RF bursts and one double chip RF burst near the end of the sequence which has a 0->1 FSK transition for fine grained synchronization. The Beacon code is designed to have low autocorrelation with itself and with the OOC words used for normal data transmission.

All BodyLANs use the same beacon chip sequence. They differ from one another in the position of the sequence of 6 beacons per superframe and in the sequence of ones and zero FSK Tones of the beacon chips. There are more than 10^20 different combinations of beacon position and beacon code to provide adequate diversity (though some are simple shifts of others). Coarse synchronization is accomplished by turning on the receiver continuously and oversampling the FSK signal output. The FSK output is then passed through a digital matched filter. The output of the matched filter gives the number of one/zero FSK Tone matches out of 38. A match greater than 34 for example, allows three errors to occur and still retain a match. Coarse synchronization can thus occur very rapidly, (typically in less than one superframe) regardless of the starting point of the crystal oscillator frequency. After the PEA has adjusted its frequency to lock onto the coarse synchronization, it uses the Beacon's 0->1 transition to achieve phase locking.

1.6 Modes of Operation

Each PEA has three major modes of operation: dead, sleeping, and active. A PEA is dead, such as after a battery replacement, when its internal control parameters are uninitialized. When sleeping, the PEA is also unsynchronized with the PDA. Our current plan calls for requiring that the PEA be physically moved close to the PDA such that the field strength emitted by the PDA is larger than a threshold. Note that this procedure is required only when the PEA's power source is disconnected (i.e. dead mode).

The user then activates the PDA initialization procedure. This procedure causes beacons to be transmitted at prior known positions within each frame. The PEA can then synchronize to the PDA without having to know the BodyLAN identification code. Only when the signal strength exceeds the threshold will the PEA accept the initialization sequence. The PDA then repeatedly sends out a programming sequence to initialize the PEA. When the PEA finally has been programmed, it then acknowledges that it has been programmed by transmitting on the PEA->PDA control channel, that the initialization was completed, and enters the sleep state.

In its sleep state, the PEA has been initialized but it is not synchronized to the PDA. This state can be entered by the PEA when the PDA is shut down for battery charging or the synchronization channel error rate is sufficiently high that the PEA's synchronization is suspect. We expect a transition from sleep to active to be autonomous. Thus by simply turning on the PDA in the morning, the PEAs will wake from their sleep and become active. This sleep to active transition after a lengthy period of sleep can be slow. While in a deep sleep, a PEA will listen very infrequently for the synchronization beacon. Our current plan calls for a beacon scan once every four seconds.

II. Accomplishments in the Last 10 Weeks

2.1 Summary

During the first 10-weeks we have concentrated on "visiting" each major component of the BodyLAN to ensure there are no major flaws in the architecture and to come to a better understanding of the relationship between error rate, power consumption, and code diversity. We have concentrated on the transmitter and receiver RF design, the various oscillators and their phase locked loops, the design for Hub/PEA synchronization, and bit error analysis. We also successfully hired an MIT graduate student to work on simulations, OOC generation, and system simulation.

2.2. Hardware Design

The game plan in this initial phase is to visit each section of the modem, create a preliminary design, "spice" simulate that design to allow estimation of power consumption, noise, and parameter sensitivity using a BiCMOS process as if we were going to create a chip. This allows us to make a determination of where the power dissipation goes and what are the major problems to solve. Hopefully this procedure will also establish some measure of credibility on overall potential power consumption and the feasibility of a single chip solution. It also allows us to better understand how to choose the off-the-shelf devices which will be used in the prototype construction.

Specifically, we have examined architectural and implementation issues including:

1) Choice of Pea processor
2) Transmitter circuit and spice sensitivity study
3) Transmitter Frequency modulating circuit and spice simulation
4) Transmitter frequency locking model
5) Design and simulation of negative voltage charge pump for frequency adjustment with hyper abrupt tuning diodes
6) Receiver low noise amplifier
7) Receiver local oscillator design and simulation
8) Receiver mixer Design and simulation of receiver
10) Receiver third order maximally-flat filter using design
11) FSK demodulator simulation
12) Review of about 40 papers relevant to receiver implementations
13) Study of standard products which may be used for the implementation chosen

At this time, we have examined enough of the receiver and transmitter to judge that the hard part is going to be the generation of stable transmit and receive side oscillators. On the positive side, the literature study has paid off handsomely by giving starting circuit topologies for virtually every part of the receiver design. The I & Q channel processing technique with direct demodulation (borrowed from a paper on pager design) appears to give the lowest power consumption. In addition, the section power consumption estimates suggest a substantially lower power consumption than was originally estimated.

2.3 Analysis

We have probabilistic models of OOC codes and a study of alternative signaling schemes, in particular a "symmetric" scheme where bit 1 and bit 0 both use "pulse codewords" and an "asymmetric scheme" where bit 0 uses a "no pulse codeword." If the demodulator/detector circuit can distinguish noise from pulses, the asymmetric wins out by a good margin.

We are coming to understand the FM quadrature demodulator with limiters. Detecting the FM tones is equivalent to determining the rotation of a vector whose components are the in-phase and quadrature demodulator arms. This can be done in one quarter of a period. When interference is present, the vector length changes with time and its trajectory is more like an ellipse. The direction of rotation seems to be given by the strongest signal (capture effect). Detecting the sense of rotation in the presence of interfering BodyLANs will require 1/2 wavelength.

When lack of chip synchronization among of interferes is taken into account, detection of the rotation over several FM periods (at the expense of high power consumption) appears to improve bit error performance. We now have models for performance in the face of asynchronous interference both for asymmetric schemes with detectors able to distinguish noise from pulses, and for symmetric schemes.

2.4 Prototype

We have contacted various vendors about getting PCMCIA slots for our desktop computers and have tentatively chosen a PC development system for purchase. Several vendors have expressed an interest in helping develop the PCMCIA interface card and in establishing its compliance. We have hadestablished discussions with Palmtree, Globe Mfg Sales, Databook, S-MOS systems, Centennial and IBM about possibly partnering in the prototype development.

III. Milestones for Next 12 Months

- Receiver circuit design
- Optical Orthogonal Codes (OOC)
- Power budget analysis
- Simulation and tests of transmitter and receiver stages
- BodyLAN system SPECIFICATION (VERSION 0)

End of SEP 94

- BodyLAN performance simulations
- ANALYSIS AND DESIGN REPORT
- Transmitter and receiver circuit specifications
- Begin software writing

End of DEC 94

- PCMCIA software driver
- Tester software (e.g., bit error rate, synchronization)
- HARDWARE SENT TO FABRICATION
- PDA software

End of MAR 95

- Test transceiver prototype
- BodyLAN prototype beta software ready
- BodyLAN BETA PROTOTYPE
- Begin performance testing

End of JUN 95

- OOC and Synchronization performance characterization
- Single and multiuser performance characterization
- BodyLAN DEMONSTRATION
- FINAL REPORT

End of SEP 95

IV. Detailed Progress Report

4.1 BodyLAN Hardware

BodyLAN hardware components consists of a Hub modem interfaced to a Personnel Digital Assistant (PDA) and one or more Personal Electronic Accessory (PEA) Modems. The current plan calls for the Hub modem to be implemented on a PCMCIA card. This card would be generic to all BodyLAN systems regardless of which PEAs are chosen. We envision that in later revisions, the Hub modem function will be built into the PDA to reduce cost and free the PCMCIA card for other functions. Any applications would typically couple a transducer to PEA modem.

Many of the sections comprising the Hub and PEA modems are identical. The main difference between Hub and PEA modems is that the Hub is required to both transmits and receives simultaneously while that the PEA modem never transmit and receive simultaneously. This reduces power consumption in the PEA modem because of the very limited battery size.

Common modem components consist of a timing generator, receiver, transmitter, and microprocessor controller as shown in Figure 1. There are three separate time multiplexed channels for transmitting user, control, and synchronization information from Hub to Pea. All three channels are broadcast by the Hub on one 2.5MHz frequency band. The receiver converts the FM modulated RF bursts within this band into a logic level data sequence and then into a byte stream suitable for input to the microprocessor. Similarly, there are two separate time multiplexed channels for transmitting user and control information from Pea to Hub. Both these channels are broadcast by the Pea on one 2.5MHz frequency band widely separated from the receive-side band. The transmitter converts a byte stream sourced by the microprocessor into a sequence of equal duration FM modulated RF bursts at time positions signaled by the timing generator. All user interface, synchronization control, and modem tuning is handled by the microprocessor.

In the PEA modem, additional circuitry is added to allow receipt of beacon information broadcast by the Hub to affect synchronization even when the PEA modem is totally unsynchronized with the Hub. In addition, the PEA has alarm clock circuitry which allows the PEA to wake up after entering ultra low power modes to sense whether to become active. A user interface is implemented in part with special circuitry to minimize the amount of time that the microprocessor must be in its high power active mode. On the Hub side, a PCMCIA interface provides a high speed interface between the Hub modem and the PDA. Unlike the PEA side, this interface is powered whenever the PDA processor is executing.

We are designing the modems using Spice parameters from a 0.8 micron BiCMOS process described in ISSC Vol 29 #3, March 94. This design process is intended to give some credibility to the power estimates achievable if the modem were to be implemented using a single BiCMOS chip. The prototype will be constructed using-off-the shelf components based on the design.

Both Hub and PEA modems share many components including the transmitter, receiver, reference voltage-controlled crystal oscillator, sub-bit and chip clock generators, component adjustment circuits, interface to the modem microprocessor, power converters and bias generators. The following sections describe at least one embodiment of several of these sections with and estimate of power consumption based on a PEA->Hub user channel bandwidth of 2K bps.

4.2 Transmitter Design

The transmitter circuit attempts to create a sine wave oscillatory signal in the loop antenna at the carrier frequency +/- 1.25 mhz in response to a pulse enable signal from the controller. Ideally, we would like the sinusoidal current to smoothly increase to its maximum value in a small fraction of the chip period and collapse after the enable signal is negated in a small fraction of the chip period.

We would like to be able to digitally select the maximum value of the antenna current. Other transmitter specifications are:

- 5k microvolts/meter (RMS) at 1.4 meters 320-360 MHz
- 2.4 volt battery operation
- power selectivity 16 dB in 4 increments
- carrier frequency control +/- 8%
- FSK +/- 1.2 MHz digitally controlled
- frequency stability +/- 100KHz
- synchronization to 131072 Hz reference oscillator
- Tx harmonics less than 375 microvolts/meter at 2nd, 3rd, higher
- full power turn on time 75-100 nsec
- antenna coil inductance 50-70 nh
- antenna Q > 400
- power consumption less than 10 nJoules/bit
- few external components
- all components except the antenna to be small

BodyLAN antennas occupy less than .0006 radiansphere in space (a radiansphere has a radius=wavelength/2*pi and is the space occupied by the stored electric or magnetic field). Thus BodyLAN antennas are essentially an electric dipole C or a magnetic dipole L or a combination of both. The radiation power factor (PF) is ratio of the radiated power to the reactive power stored in the radiansphere. For any shape of small electric or magnetic dipole, the radiation PF at one frequency is proportional to the volume. Moreover it is nearly equal for the two kinds of dipoles if they occupy the same volume.

Both electric and magnetic dipoles radiate by driving a current into the input terminals of the antenna. For a small loop antenna, the current at its terminals is essentially uniform around its circumference whereas for a small electric dipole, the current tapers linearly to zero. Both antenna types exhibit ohmic losses due to skin effect crowding. These ohmic losses are typically much larger than power radiated so that the Q of the antenna is virtually the same as a non-radiating antenna. For both electric and magnetic dipoles the Q is very high (typically in the several hundreds).

The large Q associated with very small antennas has both positive and negative aspects. For the transmitter antenna, the very narrow bandwidth associated with a large Q means unwanted harmonics will be severely attenuated. On the negative side, the very narrow bandwidth means that the bandwidth of the driven signal must also must be very small. In BodyLAN, we exploit the high Q of the transmitter antenna by making the TX antenna part of a resonant circuit and dynamically changing the resonating capacitance to modulate the frequency. Using this approach, the antenna is always operating near its maximum radiation power factor.

From a theoretical standpoint, the radiation emitted from an equal volume magnetic and electric dipoles are essentially equal. From a practical standpoint, this theoretical equality is difficult to achieve. An electric dipole equivalent to 0.02 meters long has a radiation resistance more than 14 time that of a single loop antenna 0.02 meters in diameter. Thus for the same approximate size, the electric dipole is much more efficient than the loop. A two turn loop can reduce this ratio by a factor of four but typically has a self resonant frequency only slightly above the transmission band. This would suggest using a dipole over a loop for the TX antenna.

The impedance looking into the terminals of a dipole is more than 10 times that of a loop. Thus, for the same driving voltage, the loop radiates over seven times the power that the dipole radiates. To match the high impedance of the dipole to the low impedance of a typical driver requires series resonating inductance with a very large Q and high self resonating frequency. This inductance is very difficult to create and physically would be very large to achieve a high Q.

Our current plan is to utilize a hybrid antenna combining a half-dipole and loop. This hybrid will be constructed to be self resonating somewhat above the transmission frequency band. Experimentation is required to achieve the best matching between half-dipole and loop. For the purposes of Spice simulations we have been assuming a transmit antenna of a single loop having an inductance of 60 nanohenrys and Q of 150.

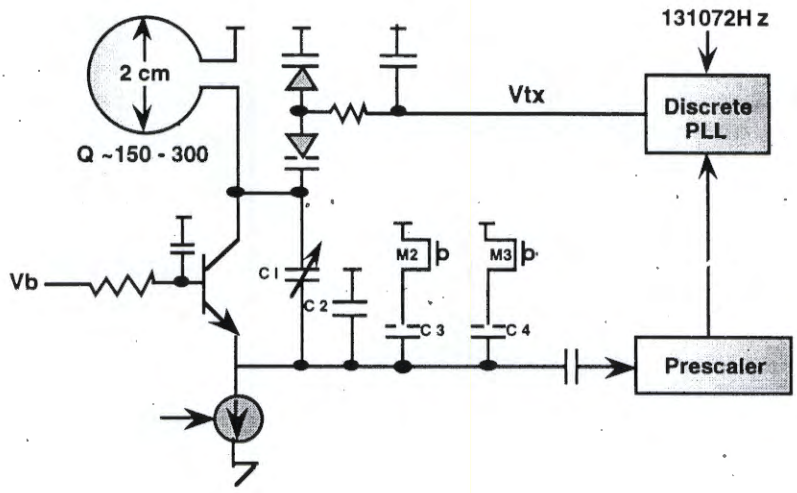


Figure 3 BodyLAN Transmitter

A modified Colpitt's circuit is used as the transmitter antenna driver. This circuit (shown in Figure 3) has shown the best stability, conversion efficiency, and power-up performance of any of the circuits examined.

To FM-modulate the carrier, transistors M2 and M3 are both turned on or both turned off. When M2/M3 are both on, the capacitors C3/C4 are added in parallel to C2 and thus the frequency is lower than the carrier. When M2/M3 are both off, the capacitors C3/C4 are placed in series with the drain overlap capacitance of transistors M2/M3. This increases the frequency of oscillation.

We currently plan to enable the transmitter for about 125% of a chip period to allow for some timing uncertainty between PEA and Hub modems. Assuming 5 chips per bit, and 2000 b/s data rate implies a transmitter duty cycle of 0.006. A bias current of 200uAmps is sufficient to generate the 5000 microvolt/meter radiation at 1.4 meters. This implies a power consumption of just 4.5 uWatts.

When bias current is applied to the transmitter transistor, oscillatory buildup occurs at exponential rate. These oscillatory buildup times do not satisfy our 75-100 nsec turn-on time. To improve this time we need to increase the transistors bias current. The basic idea is to increase the bias current to 4*Ibias at the turn on time and have it exponentially decay to Ibias.

A similar problem occurs when the bias current is removed due to the high Q of the antenna. Here the antenna rings with a time constant proportional to its Q. Since the antenna radiates during the time that it rings, we would like to dampen the ringing. By connecting the drain of a dampening transistor to the antenna, and on immediately after removing the bias current, the antenna can be dampened.

Figure 4 shows the antenna current without oscillatory build-up enhancement and dampening and after using an Ibias(0) = 4* Ibais with an 16 nsec exponential decay.

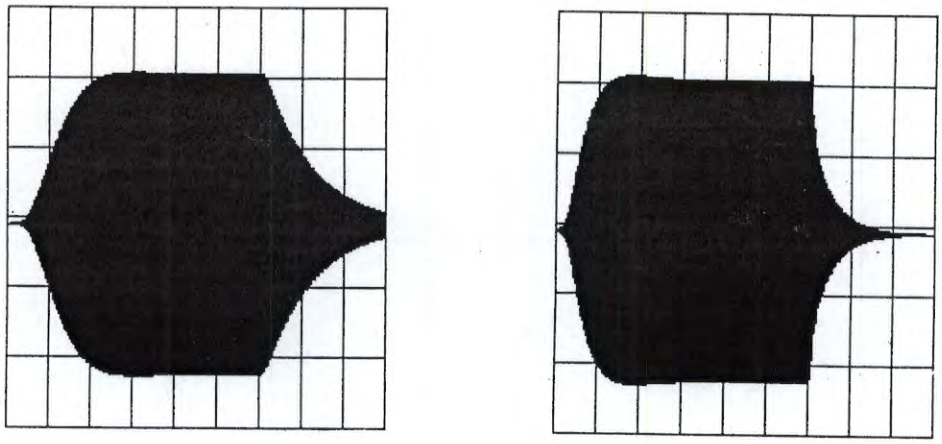


Figure 4 Transmitter Antenna Current With & Without Pulse Shape Enhancements

While the protocol is relatively insensitive to carrier offset, the carrier frequency must be controlled quite tightly. The +/- 100KHz carrier frequency specification represents +/- 310 PPM tolerance. While compared to narrow band channels, this frequency tolerance is very coarse, it is by far the most challenging aspect of the transmitter design.

Tuning the transmitter involves turning transistors M2 on and M3 off and adjusting the varacter voltage Vtx (see Figure 3). The first problem is that when we enable the transmitter during the frequency adjustment procedure, we must do so for a relatively long period of time to allow phase locking the transmitter to the 131072 Hz reference oscillator. Even more troublesome is the fact that during the transmitter frequency adjustment procedure, power is being radiated by the antenna.

From the Spice simulations, non-linearities in the varacters cause about 500 KHz variation in the resonant frequency as the power level is increased from minimum to maximum. Thus the simple approach of biasing the transmitter at its lowest power setting for tuning and counting on frequency stability for full power output is not an option.

Another concern is providing a constant resonant frequency over the duration of the RF pulse. Spice simulations have shown that during the transition time between power-off and power-on, the frequency will vary by as much as 200 KHz depending on the varacter control voltage. When the bias current is turned off, the high Q antenna will ring at a resonant frequency about 1.5 MHz higher (due to reduced collector capacitance). This is well outside of the 200Khz specifications. Adding dampening will reduce the amount of time in this off->on transition.

4.3 Receiver Design

The function of the receiver in BodyLAN is to convert the microvolt signals sourced by the receiver antenna into logic signals which are further processed by the digital hardware. With an antenna height of approximately 0.01 meter and a minimum field strength of 5k microvolts/meter at 1.5 meters distance, we expect the minimum voltage generated by the antenna to be about 50 microvolts

RMS. When the receiver is brought in near proximity to the transmitter, the received voltage increases dramatically. At 0.05 meters distance, the expected voltage will increase to about 2000 microvolts RMS.

The expected input referred noise of the receiver must be fairly low to achieve a reasonable error rate at the minimum field strength. At this time we do not know the relationship between error rate and signal to noise ratio. For non-coherent binary FSK modulation, a 10^-4 error rate requires a 12.5 dB signal to noise ratio. In the BodyLAN system, we are always sending multiple chips for each bit of information. For fairly low noise induced error rates, (i.e. 10^-4), the probability that a sufficient number of chips get error hits to cause the entire bit to get an error hit is much less than the expected non-coherent FSK binary error rate. We may reasonably expect to get by with an S/N ratio of approximately 6-9 dB. Neglecting the redundant coding of each data bit, a 12.5 dB S/N ratio requires the receiver to have an input referred noise voltage of less than 11.8 microvolts RMS.

We employ a single stage direct conversion approach to minimize power consumption. In direct conversion, the antenna voltage is first amplified by a low noise amplifier before being fed to an I/Q mixer stage. The I and Q mixer outputs are then each separately filtered by a low pass filter to remove any non-BodyLAN signals received off the antenna. The I and Q channel filter outputs are then further processed. While direct conversion requires twice the power consumption to process the I and Q channels, the processing is done at the lowest possible frequency. Only three blocks, the local oscillator, the LNA and the mixer, must process information at the carrier frequency. We expect this approach to yield the lowest power consumption.

There is a problem with direct conversion due to parasitic coupling between the local oscillator and the receiver input. This coupling can occur directly between the external passive devices which control the local oscillators resonant frequency, or indirectly through parasitic capacitive coupling in the receiver itself. To address this problem we plan on both injecting a compensating local oscillator signal into the mixer and including a transmission zero at DC in all I and Q processing stages. This has the advantage of making the receiver insensitive to spurious radiation at the carrier frequency caused by the transmitter tuning its TX antenna.

Because the antennas are easily implemented and very small, we plan on having a receive antenna different from the transmit antenna. For the 0.02 meter size envisioned for BodyLAN antennas, a simple dipole antenna generates a significantly larger voltage than a single turn loop antenna. At this time it is unclear whether a dipole or loop antenna will be utilized for the receiver. Most pagers utilize small loop antennas thus suggesting that the reduced antenna voltage can be overcome by tuning the loop to the carrier frequency. Since we plan on adopting some form of frequency hopping to avoid a heavily congested band, tuning the loop would require yet another tuning mechanism, this time for the input antenna. In theory, a loop antenna can generate a very large voltage into a high impedance load by resonating the loop with a corresponding high Q capacitance. The Q of such an antenna could be on the order of 50-100 thereby generating a voltage to the receiver of Q*Effective_Height*Efield_Strength. The choice of receiver antenna is thus still open.

A block diagram of the receiver is shown in Fgure 5. It consists of a local oscillator with frequency locking, local oscillator phase shifter and amplitude adjustment, a low-noise amplifier, I/Q channel mixers, low pass filters, and I/Q channel processing.

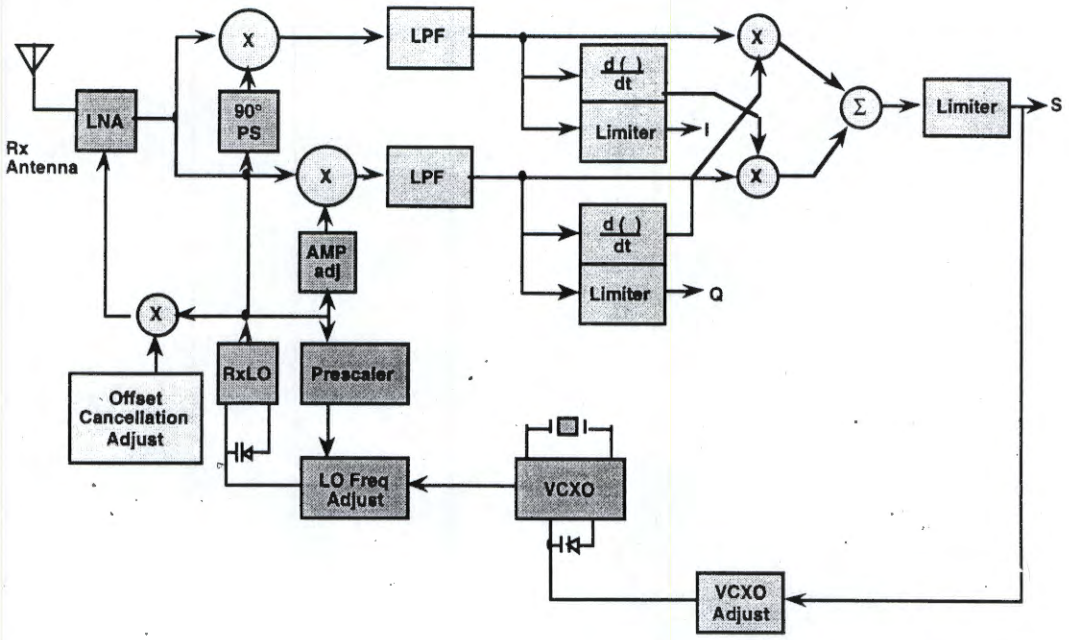


Figure 5 BodyLAN Receiver Block Diagram

S is greater than zero for frequencies above the local oscillator frequency and less than zero for frequencies below the local oscillator frequency. S is totally insensitive to phase differences between the I and Q channel mixer inputs as well as differences between the I and Q channel mixer amplitudes. Unfortunately S throws away phase information about the phase relationship between the I and Q channels. We hope to be able to use the this zero crossing information from the I and Q channel limiters to detect collisions between RF pulses transmitted by two different BodyLANs

4.4 Low Noise Amplifier

BodyLAN employs a low noise amplifier (LNA) serving three functions. First it adapts the high impedance capacitive antenna source to the mixer. Secondly it provides low noise amplification. Finally, it provides variable attenuation to allow high E fields from saturating the receiver's downstream processing. All these function must be accomplished using only a fraction of the allocated power consumption and function over the complete range of process, temperature, and voltage tolerances.

The transimpedance amplifier is a commonly used topology to couple an electrically small antenna to the mixer stage in high performance receivers. One implementation of the amplifier is shown in Figure 6. The amplifier has relatively low input impedance and flat gain characteristics because of the capacitive feedback. Important specifications for these amplifiers include equivalent noise voltage, overload level, bandwidth, power dissipation, and power-supply rejection.

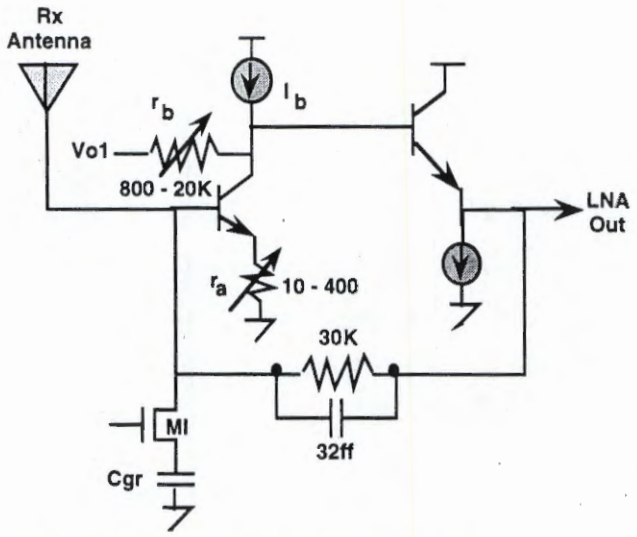


Figure 6 BodyLAN Low Noise Amplifier

For Ib=200 uAmps, the gain of the LNA is about 14.5 dB with an input referred noise of 2.65 nanoVolts per root hertz. For a 2.5 megahertz passband bandwidth, the noise voltage is 4.2 microvolts RMS. Thus to achieve a 12 dB SINAD, the minimum antenna voltage must be greater than 16.2 microvolts. Because subsequent noise terms are reduced by the LNA gain (i.e. 5.3 in its maximum gain mode), the LNA will dominate the overall receiver noise. We expect the overall receiver noise to be about 6 microvolts thus leading to a 23 microvolts minimum input signal needed to achieve 12 dB SINAD. This corresponds to a received field strength of 2300 microvolts per meter at the 0.01 meter effective height of the receiver antenna.

By simultaneously decreasing Rb, increasing Ra, and turning on mosfet M1, the gain can be reduced from 14.5 dB to -21 dB, a reduction of 35 db, and the maximum input signal can be increased to 580 millivolts RMS. This corresponds to an input field strength of 58 volts/meter (i.e. radiated power of a one killowatt source at 3 meters). For operation in an environment with this large of a field strength, the filtering would have to attenuate the unwanted, very high field-strength signal by 95 dB. For the moment, we intend to implement an LNA with gain control to limit the output voltage excursion, but not the Cgr input capacitance needed to allow very high field strengths. This will limit field strengths to about 4 volts/meter.

4.4.1 Mixer

The proposed receiver mixer is a conventional balanced design with variable emitter degeneration shown in Fgure 7. Transistors q3/q4 form a differential pair with emitter degeneration Rea/Reb. Rea/Reb can range in value from about 10 ohms to 1k and serve to both linearize the voltage to current conversion and to allow reduction of the mixer gain.

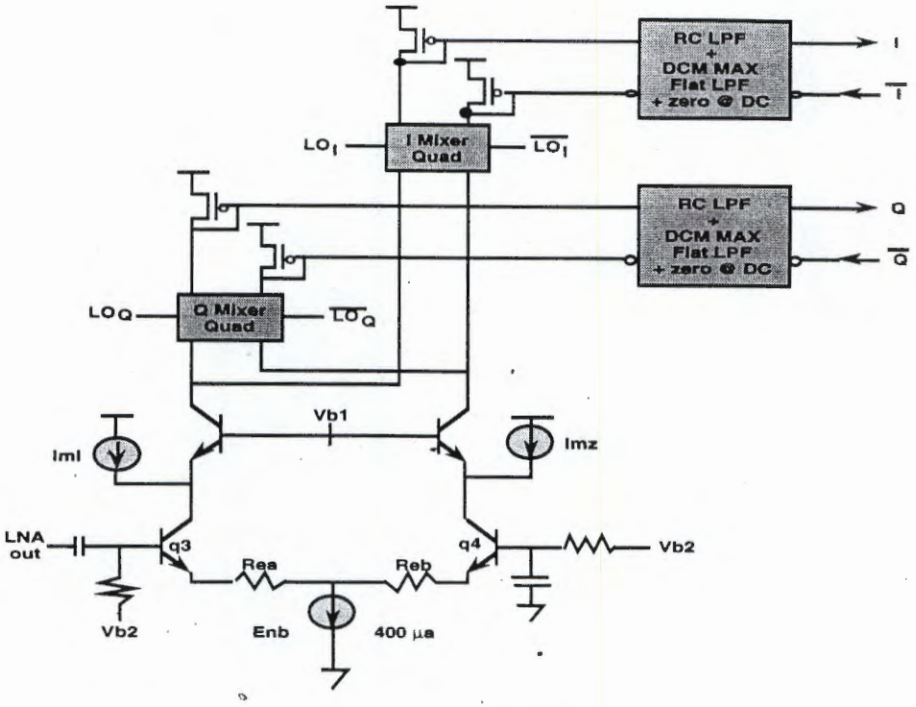


Figure 7 BodyLAN Mixer & I/Q Channel Filters

With all Pfets sized at 200/.8 and Nfets at 50/.8, a tail current of 400 microamps, and Rex=10 ohms, the differential mixer transconductance is .0026. At maximum Rex=1k, the gain is reduced by a factor of 6.8 and allows linear operation with LNA output up to 80 millivolts RMS. Thus the LNA and mixer become saturated at about the same antenna voltage. A larger dynamic range of the mixer requires higher tail currents and thus higher power consumption. The input referred noise of the mixer at maximum gain is 6 nanovolts per root hertz. This noise component is reduced by the LNA gain on an input referred basis and contributes only about 0.5 dB more noise at the input.

4.4.2 I and Q Channel Filters

The output of the balanced mixer contains a DC component caused by LO coupling with the RX antenna, a LO frequency components due to leakage of the large LO signals through the mixer quads, a very large component at twice the LO frequency, many spurious signals from non-BodyLAN and other BodyLAN transmitters and other in addition to the desired BodyLAN signal. The I and Q channel filters must pass through the desired signals and attenuate all other signals.

If we require that the unwanted signals be at least 20 dB less than the desired signal, the stopband attenuation must be significantly larger than 20 dB. For example, the twice LO frequency mixer byproduct signal is on the order 100 uAmps. With a minimum BodyLAN signal of 0.05 uAmps, the filter must provide 85 dB of rejection of the 2X LO signal.

There are many different types of passband attenuation profiles. For BodyLAN, we believe that a filter having 0 dB attenuation in the passband and infinite attenuation in the stopband with zero transition between passband and stopband is not ideal. This is because the delay as a function of frequency of such a "brick wall" filter will approach infinity near the transition frequency. In BodyLAN, we want the delay of the demodulated RF burst to be constant regardless of small variations in either the transmit frequency or the receiver local oscillator frequency. The nominal FSK frequency offset is 1.25 MHz. Including tolerances in both the transmit and receiver oscillators implies that the FSK frequency offset will be 1.25 MHz +/- 0.2 MHz. Since fine scale

synchronization is derived from the transition between carrier frequency minus the FSK offset to the carrier frequency plus the FSK offset, we would like the delay through filters to be constant. A constant delay suggests a linear phase or maximally flat filter.

Our current plan utilizes a cascade of two on-chip filters of increasing complexity. Each stage reduces the level of interfering signals to within the dynamic range of the following filter. The first filter is a passive RC network at the mixer output to remove the large 2X LO frequency components. These RC filters have good dynamic range but their 3 dB frequency is dependent upon on-chip capacitors and resistors. The cutoff frequency is thus expected to thus have +/- 15-20% tolerance. If we adopt a cutoff frequency of about 9 MHz, the 2X LO frequency is attenuated by a factor of 8000 and only 15 degrees of phase shift is introduced.

The next stage is a fourth order, linear phase filter (0.5 degree passband ripple), fully differential filter with a 3dB frequency at 1.25 MHz. The attenuation versus frequency of this filter is:

frequency MHz	attenuation dB
1.25	6
2.5	26
3.75	42
5.0	53
7.5	63
12.5	80

We expect BodyLAN sub-bands to be separated by about 8.4 MHz. Thus adjacent BodyLAN bands will be attenuated by about 70 dB.

Designing on-chip I and Q channel filters is straightforward as illustrated by many articles on continuous time filters. The major design issue in BodyLAN is power consumption. Power consumption is proportional to the number of poles, edge frequency, dynamic range. The number of poles and edge frequency is fixed by the signaling architecture whereas the dynamic range is an free parameter.

On-chip filters are constructed from integrators whose unity frequency is proportional to the transconductance and inversely proportional to the capacitance. For the BodyLAN filters, a capacitance of 2-3 pf would be the minimum allowed capacitance to achieve reasonable tracking. This requires a transconductance on the order of 15 microamps/volt. A 12.8/3.2 Nfet biased at a 0.5 microamps has a transconductance of about 20 microamps/volt. If a typical balanced integrator requires about four transistors of comparable transconductance thus giving an overall minimum power consumption of about 2 microamps per pole. We would thus expect a minimum power consumption for both I and Q channel filters of about 16 microamps.

The problem with a realization employing such low bias currents is its very small dynamic range. If the mixer output current is .05 microamps, a current mode integrator realization would provide a dynamic range of 10 to one. While the signal to noise ratio is still adequate, the filters will quickly saturate for any but the smallest input signals. Increasing the bias currents of a current mode integrator by a factor of 20 would increase the dynamic range to equal the 200 to one range in BodyLAN signals. There would be no headroom however for preventing saturation from higher signal strength out of band signals however.

The channel filters can also be implemented in the voltage domain. For a mixer gain of 12 dB, the minimum output signal is about 1250 microvolts RMS. Typically, a voltage mode integrator will provide about 600 millivolts of linear range at BodyLAN supply voltages. Thus implies a 170 to one dynamic range which is almost enough to satisfy the 200 to one dynamic range of BodyLAN signals. This rough estimate does not include the effect of Q multiplication where internal integrator nodes

have higher RMS voltages than the filter input. In addition, the 600 millivolt limit cannot be easily increased where in a current mode filter a simple bias voltage change can double the bias currents. We have thus tentatively elected to implement the channel filters using current mode integrators.

4.5 Bit Error Rate Analysis

We have made significant progress in analyzing the bit error rate for the BodyLAN channel. This includes stochastic models and bit error analysis under alternative design assumptions. This section describes the spread spectrum signals, the dynamics of detecting the pulses within the spread spectrum signal, and the probability of error analysis given alternative detection rules for the spread spectrum signals. Work is still in progress.

We choose Code Division Multiple Access (CDMA) for data transmission "within" a BodyLAN to simplify coexistence with nearby BodyLANs. CDMA is based on spread spectrum signals of low mutual cross correlation. Transmissions in one BodyLAN are nearly transparent to those of another nearby BodyLAN. For spread spectrum we chose Optical Orthogonal Codes [Chung89]: a family of codewords consisting of a sparse set of short pulses over the bit period. This means that the duty cycle of the transceivers over a bit period is low (e.g. 3 pulses out of 64 possible pulse positions), which contributes to low power. Optical Orthogonal Codes (OOC) are robust again "near-far" situations because their information is encoded in the pulse "positions." Their spread spectrum nature also facilitates meeting FCC power-constraint regulations.

An exact characterization of CDMA bit error rate for Optical Orthogonal Codes falls in the domain of simulation and experimentation. At this stage of the project we consider it sufficient to model the interfering OOC signals as a stochastic process describing the presence of interfering pulses on the channel. The models facilitate signal design and bit error analysis. A particularly simple and useful model treats interfering pulses as Bernoulli trials with a low probability of pulse presence [Escobar88]. A more accurate but less tractable model considers a fixed number of pulses per signal, with pulse positions assigned as a uniform random variable over the possible positions in the signal. Here we report primarily results obtained from the Bernoulli approach.

The first part of the bit error analysis consists of a characterization of the pulse detection circuitry at the receiver. BodyLAN uses Frequency Shift Keying and FM quadrature demodulation. The pulses in the OOC are transmitted one of two possible frequency bands. (The system can extend to M bands.) The pulse detection circuit exhibits a capture effect: when several pulses are received at the same time, detection tends to favor the strongest signal present. We have explored this process under several circuit design assumptions and taken into account the lack of synchronization between signals from different BodyLANs. For this report we concentrate on one simple circuit. The end product is the probability of correctly determining the FM tone for a pulse of interest in the presence of interference. We will also survey possible improvements from possible design alternatives.

Given this pulse detection probability we can compute the probability that a specific pattern of pulses is being received in the presence of interference. This gives the bit error probability. For the simple model, the bit error probability presented is an upperbound, as will be discussed. However, it serves to analyze alternative circuit designs and potential improvements. Thus, one issue we are exploring is the appropriate trade-off between circuit complexity and bit error rate.

4.6 Optical Orthogonal Codes

BodyLAN signals a bit" zero" or bit "one" using sparse patterns of pulses similar to pulse position modulation systems. The same pattern is used for both bits, but each pulse is a Frequency Shift Keying signal produced by FM modulation. The frequency pattern of the pulses for bit zero are the opposite than the pattern for bit one. The frequency pattern for each bit is "balanced," in the sense

that both FM frequencies are used approximately equally often. Desirable CDMA signals mus interfere little with each other, so the bit signals are designed as "Optical Orthogonal Codes."

Optical Orthogonals Codes [Wei] are a family of codes with low cross correlation properties and lo off-peak autocorrelation properties. Each codeword in the code corresponds to a spread-spectrur signal. A codeword of length n corresponds to a spread-spectrum signal of n chips (i.e., spreadin factor = n). Pulses are transmitted at selected chip positions, while the remaining chip position remain empty (silent). The code design consists of selecting an appropriate set of pulse positions i the codewords such that the correlation properties are desirable.

Figure 8 shows two sample codewords from a code of length n=7, number of pulses w=2 an maximum cross-correlation of 1. Such code is denoted as (7,2,1). Any relative "cyclic" shift o these codewords results in at most one pulse overlap among them. Any relative cyclic shift of one o these codewords relative to itself also results in at most one pulse overlap.

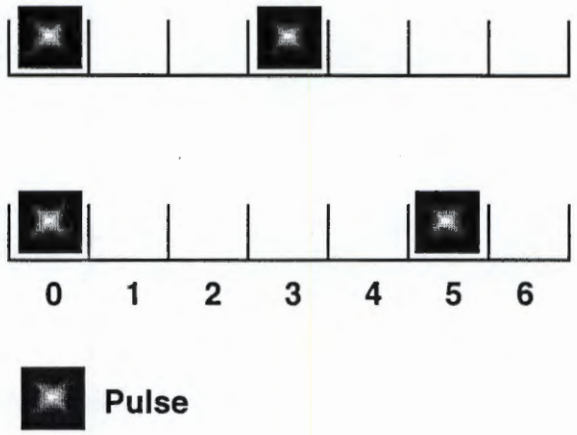


Figure 8 Two sample codewords from a (7,2,1) OOC

There are several methods to generate (n,w,a) OOCs, including computer searches and an algebrai mechanism based on Projective Geometry. We favor the latter because the properties of the code ar explicitly controllable by the algebraic Galois Field structure in which they are based, and becaus there are results in the literature regarding how to obtain the largest number of distinct codeword (module cyclic shifts) when an (n,w,1) code is desired.

As a start, we are considering a (63,3,1) code with 10 codewords, the maximum number o codewords (module cyclic shifts) possible given the code parameters. Table 1 shows the codeword expressed as a set of pulse positions. We would trivially extend it to 64 chip positions. As we refin the design and performance of BodyLAN we expect that we will have to try codes with differen characteristics. We are also planning to use an OOC structure to prevent collisions among "timing signals ("beacons") from different BodyLAN PDAs. These beacon signals are emitted often enoug for the PEA peripheral devices of each BodyLAN to maintain chip synchronization to within 10 n or so. Chip timing is the finest grained level of a BodyLAN's TDMA architecture.

{0, 1, 21}	{0, 2, 16}	{0, 3, 27}	{0, 4, 17}	{0, 5, 31}
{0, 6, 18}	{0, 7, 28}	{0, 8, 19}	{0, 9, 29}	{0, 10, 25}

Table 1 Example of largest codeword set for (63,4,1) OOC.

Because each BodyLAN utilizes a TDMA structure, only one PEA device from each BodyLAN is active at any given time (transmission from the PDA to PEAs takes place in a separate band). Thus 10 codewords would correspond to 10 different BodyLANs. All devices in the BodyLAN use the same codeword. However, if we now consider all possible cyclic shifts of each codeword, the total number of possible patterns over one bit period becomes 10 x 64 = 640. Thus, BodyLAN can use a pseudo-random sequence of cyclic shifts and codewords with a different choice at every bit, to reduce the probability that two BodyLANs using the same codeword will choose the identical cyclic shift for a given bit. We are exploring the changes in cross correlation properties induced by this approach. The method allows much more than 640 BodyLANs since the number of possible pseudo random sequences is much higher.

We can also observe that on average two transmitters following the pseudo-random sequence method above will choose the same codeword and cyclic shift once every 640 bits. This limits the bit error probability that can be obtained. However, several further mechanisms limit the interference probability among BodyLANs. BodyLAN pulses will use one of two (or possibly M) different frequency bands, in a balanced fashion. This is an FSK system designed to improve the diversity among codewords. The BodyLAN receiver looks for the pattern of pulses and the correct sequence of frequency tones. Because of the capture effect, pulses from nearby transmitters will tend to win out since their signal will be strongest. Also, the lack of synchronization between transmitters will further reduce this probability. Finally, the duty cycle (active time) per device is typically a small fraction (e.g. 10%) which reduces the collision probability by approximately one order of magnitude.

Notice that if all pulses were transmitted at the same FM frequency, BodyLAN would be vulnerable to narrowband jamming. (For this discussion, jamming refers to a non-BodyLAN transmission.) A Continuous Wave transmitter at the pulse frequency would deny BodyLAN the ability to determine the presence of a pulse pattern. The use of 2 or m frequencies for the pulses is equivalent to frequency hopping, which gives better jamming rejection.

4.7 Pulse Detection

Because receivers and transmitters within a BodyLAN are synchronized by beacon signals, the receiver knows when to expect a pulse. The pulse detection circuitry must then determine the FSK frequency of the pulse. For FSK we favor an FM modulator and demodulator. The current demodulator under consideration exhibits capture of the strongest signal and an error will be made at the chip level if the interference present is equivalent to a signal of the opposite tone and stronger than the desired pulse. Typically the power difference will be sufficiently large that partial overlap of an interfering pulse with the desired pulse is still sufficient to cause an error if the interference is strong enough. Figure 9 illustrates this situation of partial overlap.

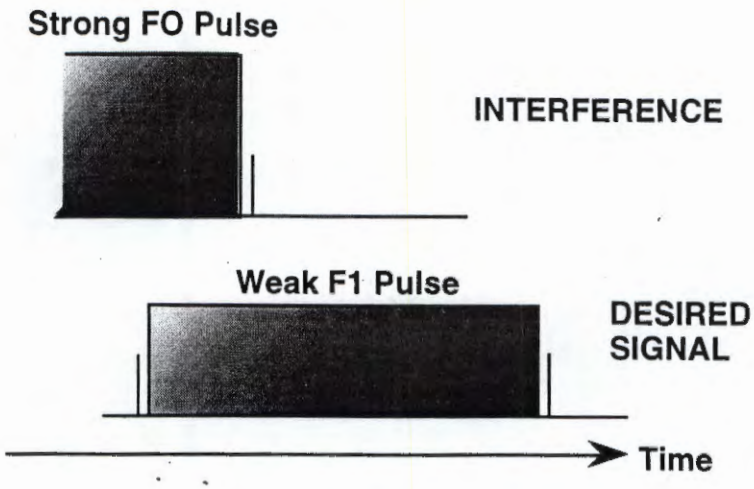


Figure 9 Partial Interference Overlap Leading to Error.

From Figure 9 we can state the "chip detection error" probability in the presence of one interfering user of strongest signal. This probability refers to deciding for the wrong pulse frequency over the desired chip interval. In the typical case two chip positions of the interfering user overlap the desired chip position. We can refer to the interfering chip that overlaps the leading edge of our desired pulse as the "leading" interference chip. Similarly, we can define the "trailing" interference chip as the subsequent chip in time. The probability of error can be found from the probability that an interfering pulse is present in the leading interference chip, plus the probability that this does not occur but that a pulse is present in the trailing interference chip.

Using a model of independent Bernoulli trials for the presence of a pulse in an interfering chip and assuming that the interfering pulse frequencies are also balanced, the chip detection error probability above becomes $q + (1-q)\, q$, where q is the probability that an interfering chip leads to an error. In other words $q = pf/2$, where p is the Bernoulli probability that the pulse is present, and 1/2 is the probability that its frequency is the opposite of the desired pulse and f reflects the fact that a partial pulse overlap leads to a lower interference probability. This statement assumes that the interfering signal is stronger than the desired pulse, since if the interfering signal is weaker it will not lead to errors. The Factor f is a parameter modeling user behaviour. It summarizes the proximity of BodyLANs, the fact that the smaller the overlap between pulses the larger the interference needed for an error. It also reflects the fact that PEAs are not active 100% of the time.

Since OOC codewords consists of a sparse pattern of pulses, signals seldom have two consecutive pulses and the error model above can be concatenated over the successive detection of pulses from a codeword. In other words, the two chip intervals from an interfering signal that overlap a chip position under detection are disjoint from the interfering intervals for the next chip position of interest, as illustrated in Figure 10. The net effect is that the chip detection error probability above can be treated as independent and with identical probability distribution function over the chip positions where we expect pulses from the desired transmitter.

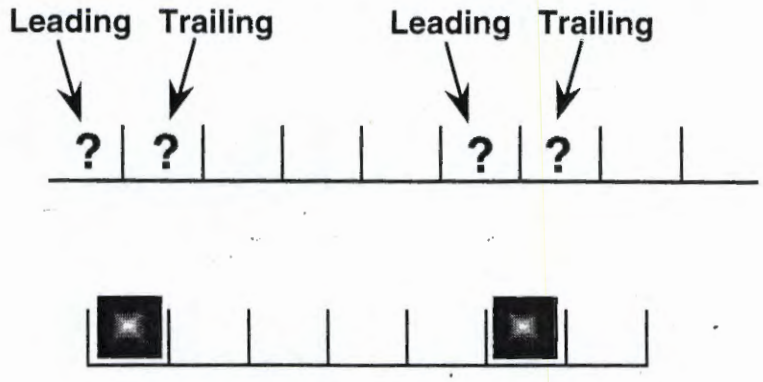


Figure 10 Independence in Asynchronous Situation for Bernoulli Interference

Before proceeding to evaluate the bit error probability based on these observations, we can discuss two alternative detection circuits. One alternative detects interference by detecting the change of frequency from the overlap region to the non-overlap region of the chip interval. This has the potential to improve performance since it would not be fooled by a situation like the one illustrated in Figure 9. It can be implemented based on an FM quadrature demodulator since this demodulators can essentially detect the received frequency at every FM signal period, and a chip period will correspond to many FM periods. The circuit however becomes more complicated since a finer grain of frequency detection is involved than before.

Another alternative worth exploring is the ability to detect that no pulse is present over a chip interval (silence detection). The current version of chip detector we are considering always decides for one frequency or the other. The ability to detect "silence" opens the possibility of using no transmission for bit zero and using a (pulsed) OOC codeword for bit one, or vice versa, or in alternating fashion over the bit intervals. A detector would look for the OOC pulse pattern, and decide if the signal received looks like silence or like the OOC codeword pattern.

The advantage of using silence detection is not so much that the average transmit power is halved, but that the number of interference pulses in the channel is halved. Since the chip detection error probability can be concatenated over the w desired pulses under detection, the bit error probability is a polynomial function of w degree in the probability p that an interfering pulse is present. Halving this probability has a significant effect in decreasing the overall bit error rate. At the moment we are exploring the extra complexity required to detect silence using an FM quadrature demodulator and the implications in term of signal design and bit error rate.

4.8 Bit Detection

The chip detection error probability is the basis for the bit error probability analysis. In the current BodyLAN design bit zero and bit one shared one OOC codeword but use opposite FSK frequencies, in a balanced manner. The detection process consists of determining the sequence of frequency tones received over the OOC-codeword pulse positions of the transmitter. A Hamming distance calculation between the received signal and the two possible transmitted bit signals identifies the "closest" bit signal, in the Hamming sense, and hence the most likely bit sent (under reasonable assumptions [Gallager68]). An example is illustrated in Figure 11.

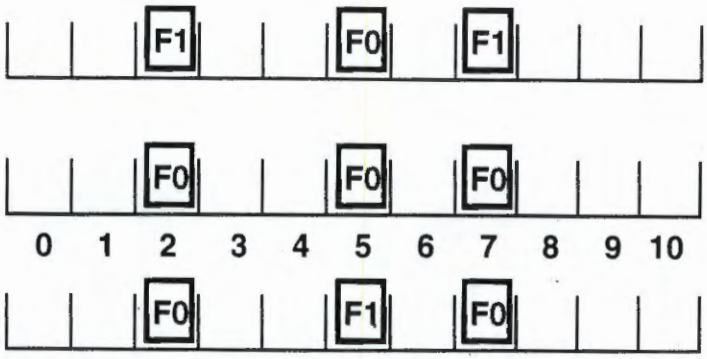


Figure 11 Example of Bit Decoding Based on Shortest Hamming Distance

The bit error probability obtained through the Bernoulli-trials model of interference can considered an upperbound for the bit error probability obtained from OOC codewords. The prima reason is that while OOCs are designed for minimum interference, the Bernoulli model is only approximation. For example, the model allows an interfering codeword to have a pulse in every cl position! Another considerations is that in extending the expression q + (1-q)q above to the case multiple interferers, we choose to neglect the possibility that one interferer could "cancel" the er produced by another. We neglect it because the probability of multiple interfering pulses is lov than that of a single interfering pulse and the approximation serves as a more tractable upperbou In spite of being an upperbound, the model is very useful as a tool to analyze design trade-offs due its analytical simplicity. We are also using more accurate models, which as a consequence are l tractable.

Here we consider a Bernoulli model for each interfering signal and a Poisson distribution for t number of interfering users whose signal is stronger than the signal received from the desi transmitter. With this model we can extend the earlier calculation of chip detection error to the c of several interfering transmitters whose signal is stronger than that of a desired transmitter. T number of such transmitters is given by the Poisson distribution (under independence assumptio and the bit error rate can be calculated from the Binomial distribution of the number of (independe chip detection errors made over the w pulse positions of interest.

Figure 12 shows parametric plots of the bit error bounds obtained this way for signals with spread factor of 64 chips and w pulses per signal on average (horizontal axis). The plots assum maximum of 5 users in the immediate vicinity and are parametrized by the value *f* average num of interferers whose signal is strongest than the desired signal times their expected duty cycle. any given plot, the bit error probability initially decreases with the number of pulses because m pulse overlaps are required for an error. The probability soon begins to increase with the numbe pulses because the load on the channel (more pulses) rapidly becomes the dominant effect. The p are also strongly dependent on *f*, which can be interpreted as a strong dependence on the behavi patterns of BodyLAN users, with close crowding tending to poor performance due to the load on channel. We expect a representative value of *f* to be consistent with bit error rates better than 10-

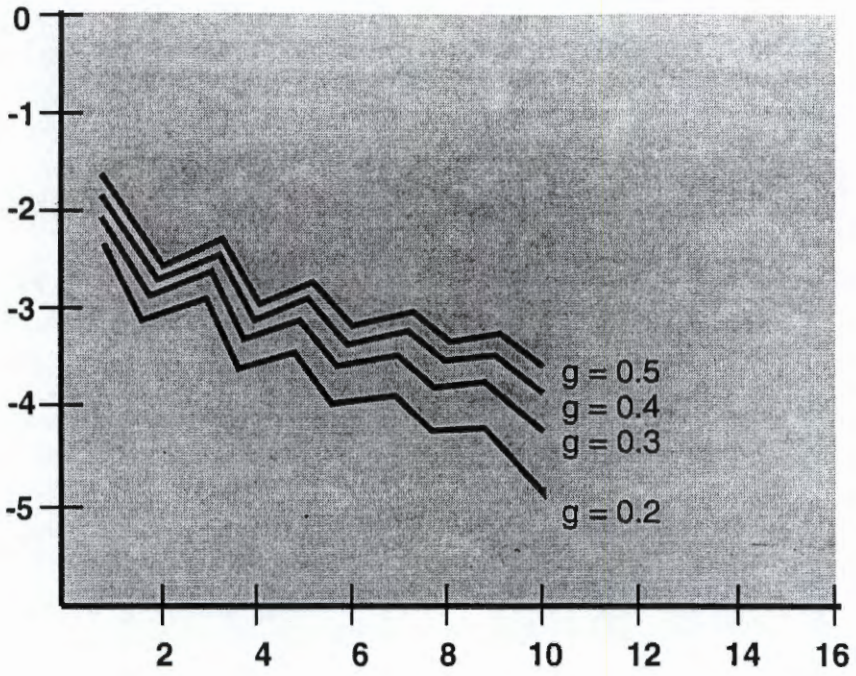


Figure 12: Bound on Bit Error Probability Based on Bernoulli Model of Interfering Pulses. The Several Plots Correspond to Varying the Average Number of Interferers Closer Than the Desired Transmitter/ Parameter g summarizes interference strenght and duty cycle, hence it determines the probability f for interference.

More accurate models that limit the number of pulses per interferer lead to lower bit error probability [Escobar88]. In fact, that the Bernoulli model is a slack upperbound can be seen from the observation that with (64,3,1) and each user using a different codeword, it would take at least two interferers to produce any error, since each of them would be able to interfere in at most one pulse position, and it takes at least two pulse errors for the Hamming distance calculation to lead to the wrong bit decision. It is worth noting here that bounds for OOC bit errors can be found in [Chung89] for the chip asynchronous case. Again the accuracy comes together with analytical complexity.

We have also investigated the potential improvement that results from a detector capable of detecting silence. Figure 13 shows a comparison of two systems: one like the one discussed so far and one capable of silence detection. Without loss of generality in the comparison, the plots in Figure 13 assumed a different distribution than Figure 13 for the occurrence of interfering pulses stronger than the desired signal and also assumed chip synchronization among BodyLANs. It is shown only for the purpose of comparison.

The system discussed this far is termed the "symmetric scheme," since the same OOC codeword is used for both bits. It shows the highest bit error probability in Figure 13, for any given number of pulses per codeword. The other system is termed "asymmetric and, in fact, ignores the FSK frequency of received pulses. It exhibits the lowest bit error probability. It could be further improved if it used a Hamming distance threshold to declare bit one even if all desired pulse positions are present.

Given the low-power and low-complexity goals of the BodyLAN hardware, it is not evident at this moment that there is an implementation of silence detection circuitry with a similar level of

simplicity than the current design under consideration. We are also exploring the performance of a receiver capable of detecting partial overlap from interfering pulses, as discussed above. For the symmetric system, it is typically best to ignore chip positions over which interference is detected. The Hamming distance is computed only over chip positions considered interference free.

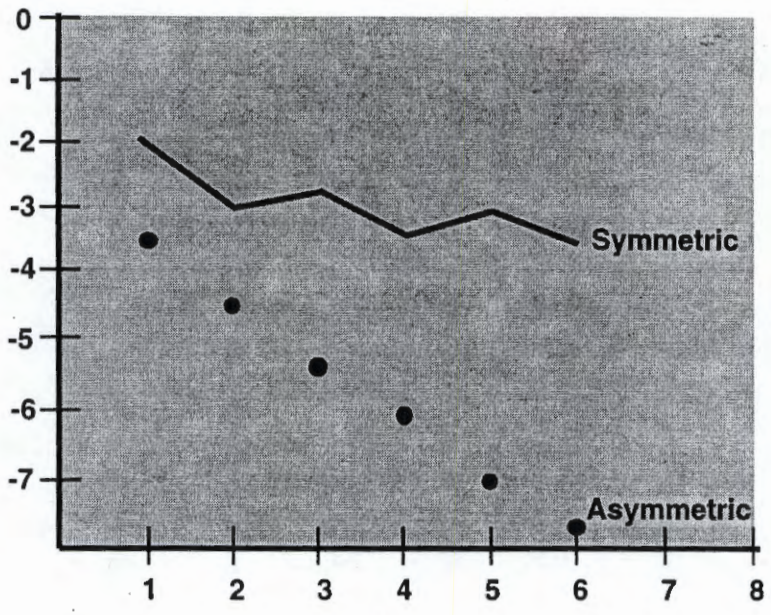


Figure 13 Comparison of Bit Error Probability Between Symmetric and Asymmetric Schemes. Asymemtric Scheme Shows Lower Bit Error Probability Because of Lower Channel Load

V. Personnel Supported

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[Chung89] F.Chung,J.Salehi,V.Wei,"Optical Orthogonal Codes: Design, Analysis, and Applications," IEEE Transactions on Information Theory, Vol 35, No.3, May 1989, pp. 595-604.

[Escobar88] J.Escobar,"Maximum Likelihood Detection for Probabilistic Models of Optical Code Division Multiple Access Channels," Ph.D thesis, MIT, Cambridge, Massachusetts, April 1988.

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October 28, 1994

Advanced Research Projects Agency, ESTO
3701 N. Fairfax, Drive
Arlington, VA 22203-1714

Attention: Dr. Kaigham Gabriel
(703) 696-2252

Subject: Quarterly R & D Status Report
Contract No. DABT63-94-C-0017
BBN Reference No. 11592 – BodyLan –

Dear Dr. Gabriel:

Enclosed is Quarterly R & D Status Report #2 covering the period July 1 through September 30, 1994 on the subject contract.

If you have any questions, or require any additional information, please do not hesitate to contact the undersigned at (617) 873-4579.

Sincerely,

Dr. Julio Escobar
Senior Scientist

cc: ARPA/ESTO/CSTO/SSTO/ASTO
B. Bolling
T. Blackadar
M. DiBlasio

JE/ro

BodyLan: A Wireless, Body Local Area Network

Contract Number: DABT63-94-C-0017

Quarterly Status Report #2

July 1994 through September 1994

Contractor:

BBN Systems and Technologies
A Division of Bolt Beranek and Newman Inc.
10 Moulton Street
Cambridge, MA 02138

Principal Investigator:
Dr. Julio Escobar
Telephone (617) 873-4579
jescobar @ bbn.com

Submitted to:

Advanced Research Projects Agency
3701 N. Fairfax Drive
Arlington, VA 02203
Attn: Dr. K. Gabriel

Table of Contents

1. PROJECT PROGRESS

1.1 OVERVIEW

Status

We have completed draft designs of transmitter, receivers, spread spectrum codes and channel access protocols, including transmitter-receiver signal synchronization. Work on bootstrap algorithms early next quarter will complete the first BodyLan specifications.

Analysis and simulations to date indicate appropriate BodyLan bit error rates, e.g., 10^-3 BER for interference 10 times the transmitter power. Before committing to our current spread spectrum codes we need to explore a few remaining performance issues.

We have begun setting up the BodyLan prototype development process. We acquired most of the development environment, excluding the Personal Digital Assistant for demo use.

At the request of ARPA, we slowed down our spending over this quarter to maintain contingency development funds for future quarters. This is reflected in the spreadsheets sent separately to K. Gabriel (ARPA) at his request (per our June review meeting in Washington). We achieved the slow-down by limiting the scope of several tasks, primarily in system and hardware analysis.

Plans for Next Quarter

In the coming quarter we plan to achieve the following milestones:

- Bootstrap algorithms
- Circuit specifications
- BodyLan specifications (version 0) and interim research report

1.2 HARDWARE PROGRESS

The primary accomplishment was to finalize an overall hardware architecture for both the Personal Electronic Accessory (PEA) modem and Personal Digital Assistant (PDA or hub) modem. This accomplishment now allows us to apply development parallelism using a combination of inside and outside development resources.

Particular BodyLan implementation activities accomplished during the quarter include:

1) Function description and detailed block diagrams of both the Hub and PEA modem electronics.
2) Design and layout of a prototype transmitter.
3) Specification document of the PCMCIA card interface to the PDA host.
4) Choosing the microcontroller to be used in both the Hub and PEA modems: the Phillips 80CL410. This micro controller implements the 80C51 instruction set and has an industry-standard IIC intra chip LAN interface. The IIC LAN can interface to about 80 existing low-power chips used in hand-held equipment and will simplify development of prototypes.

5) We have purchased all the discrete devices needed to construct prototype modems including capacitors, inductors, resistors, varactors, trim-caps, transistors, mixers, and filter components.
6) Further simulations of the Tx section, including pin parasitic capacitances and varactor non-linearities.
7) Spice simulations on two approaches to the LNA/Mixer receiver front ends, including package parasitic capacitances and bonding inductances.
8) Discrete LC-filter design and simulation for the IF filters

1.3 ANALYSIS

Generation of Optical Orthogonal Codes

Over the past quarter, MIT graduate student Thucydides Xanthopoulos (EECS department) joined the project to tackle Optical Orthogonal Code (OOC) design. He has now returned full time to MIT and we are exploring ways in which he can continue collaborating with the project. Over the coming quarter, John Zao will join the project to help in the final bit error characterization and link level performance of the system.

We have explored two ways of generating OOCs. The first method relied on Galois Field theory and Finite Geometries. Given an extended Galois Field (a mathematical construct) we can generate an optical orthogonal code (a family of spread-spectrum signals) with a spreading factor of n (i.e., n possible pulse positions), a weight of w (w pulses, $w << n$) and discrete-time cross-correlation among codewords no greater than 1. The values n and w are given by the prime number and its exponent used to generate the Galois Field.

The code is obtained by generating a geometrical space with a finite number of points, based on the Galois Field. The lines in this finite "projective geometry" represent codewords, and the coordinates of the points in the lines represent the pulse positions in the OOC. Since lines intersect in at most one point, cross correlation of two codewords is never greater than one. It can be proved that this method generates optimal codes (the number of codewords calculated is maximum.) We have developed software to automate this method.

The appeal of this method is its ability to generate the maximum number of codewords possible given the parameters n, w, and cross correlation of 1. Large codeword diversity helps reduce bit error probability. However we do not favor this approach any longer for the following reasons:

1. We do not have direct control on the n and w parameters of the code, because they depend on the Galois Field parameters, which are themselves restricted.

2. For cross-correlation values greater than 1, we have reached the conclusion that this approach does not generate optimal codes (maximum number of codewords). Since cross-correlations greater than one allow a greater number of codewords, the inability to generate optimal codes eliminates one of the leading advantages of the method.

The second method we explored relies on a greedy search algorithm. We have software that when given any spreading n, weight w, and desired cross-correlation lambda, it can search for codewords in a randomized and greedy fashion. In many cases, the code sizes generated by this program approach the theoretical upper bound, especially for low values of cross correlation. We are currently revising this software to include the ability to generate

codewords that have the appropriate cross correlation with a synchronization beacon too. This is the method that we are currently using to generate OOCs.

Code Performance Simulations

In our first quarter we had obtained analytical characterizations of the OOC bit error rate performance, which pointed to promising avenues of design. In the last quarter (2nd quarter) we have been breaking through some of the limitations of theoretical analysis by simulating code performance and exploring issues that are hard to analyze.

OOCs are constructed with an assumption of synchronous behavior, i.e., chip-aligned rise times. When they are used, however, no such synchronous behavior can be assumed. To test the goodness, or orthogonality, of OOCs under these asynchronous conditions, we created a simulation of overlapping asynchronous OOCs in order to measure the expected bit-error rates.

The simulation determined the expected bit-error rate when one "desired" code was subject to superimposition by an "interferer" code. Several factors were allowed to vary:

- Several OOC code sets were explored.
- The power ratio of the two codes was varied from 0.1 to 10.0.
- The asynchronous overlap of the two codes was varied in units of 0.1 chip over the entirety of possible overlap conditions.
- Frequency alternation of successive OOC pulses within one codeword was varied over both possible cases (e.g., for a 3-chip code, the possible frequency alternations are f1 f2 f1 and f2 f1 f2).

The simulation was done computationally, allowing each code to be the "desired" code and for each such case, all codes would take turns as the "interferer." A chip was said to be correct when there was more energy at the expected frequency than at the interfering frequency. In cases of a tie, a random choice decided. A bit was said to be correct when a majority of its chips were correct. For 4-chip codes, ties were resolved by a random choice.

General results:

- Frequency alternation of successive chips is a major advantage.
- Code diversity (i.e., more codes) reduces bit error rates.
- Theoretically poor codes (e.g., {64,4,2}) may be desirable, since the gains from frequency alternation and code diversity are greater than the loses from the autocorrelation of 2.
- Even with the power of the interferer being 10 times the power of the desired signal, and with a {64,4,2} code, bit-error rates were only of the order of 1 in 200.

We expect bit-error rates of 1 in 1000 are achievable under realistic conditions.

1.4 PROTOTYPE DEVELOPMENT

We have initiated the acquisition process and fabrication arrangements for prototype development so that development can begin in a timely manner. We have acquired or ordered the following

- IBM compatible PC equipment to serve as development environment
- Development software
- Discrete components for RF circuits

The prototype BodyLan PDA (hub) will be based on a PCMCIA card developed on a PC environment and then ported to an identical PDA environment.

We have assigned Steve Oliver to supervise the hardware fabrication process. He has assisted several previous hardware projects in this capacity.

1.5 MILESTONES FOR NEXT QUARTER

In the coming quarter we will overlap the start of prototype development and the final stages of design. We plan to achieve the following milestones:

- Bootstrap algorithms
- Circuit specifications
- BodyLan specifications (version 0) and interim research report

The bootstrap algorithm is the last significant area of design that remains to be addressed. It will enable the Personal Electronic Accessories to attach themselves to a BodyLan PDA and establish a data channel.

We will finalize circuit layouts to provide the detailed specifications needed for fabrication. Similarly, we will specify all the BodyLan parameters required to start prototype development.

2. SPECIAL PROGRAMS DEVELOPED OR MAJOR EQUIPMENT PURCHASED

Gateway P5-60 Computer System (personal computer for prototype development, cost with handling - $2,393.00)

3. CHANGES IN KEY PERSONNEL

None

4. MEETING AND VISIT HIGHLIGHTS

Phil Carvey presented a detailed BodyLan technical report at the July ARPA ESTO PI meeting. He also attended a one week course (BBN funded) on "RF IC Design for Wireless Communication Systems." This course has provided many valuable insights into the problems encountered in the integration of a modem into a chip.

We have been discussing collaboration with Michael Hawley, MIT Media Lab, on the development of BodyLan applications and PCMCIA development. Such collaboration can enhance the demonstration of BodyLan technology without requiring extra project funds. It could also serve as a seed vehicle to popularize BodyLan applications and speed their transition to the military or marketplace.

We are also exploring the use of existing PCMCIA vendors as consultants or data bus design engineers for the PCMCIA interface. We are looking at vendors who may have an interest in developing their own application and in marketing the resulting board.

We are exploring collaboration with Prof. Anantha Chandrakasan and Tom Knight of MIT EE. They and graduate students would undertake development of CMOS chips to implement BodyLan modems. Anantha specializes on ultra low-power IC design and could bring valuable insights into BodyLan development.

5. PROBLEMS OR CONCERNS WHERE ASSISTANCE OR GUIDANCE REQUIRED

It seems clear now that custom VLSI implementation will be a more effective approach to RF hardware than the Electrically Programmable Logic Array approach we originally favored. We will address this as a potential change in statement of work, though we do not think there is any cost impact.

6. FISCAL STATUS

See Attached

7. ACCOMPLISHMENTS

During this past quarter we achieved the following milestones

- Transmitter-receiver synchronization protocol
- Transmitter and receiver design, including PCMCIA interface specs
- Optical Orthogonal Code design and performance (Spread Spectrum)
- Begun equipment acquisition for prototype development
- Explored subcontractors for prototype work

The synchronization protocol uses an OOC pattern for coarse synchronization and an FM frequency transition for 10 ns synchronization, sufficient to establish OOC chip boundaries.

OOC design focused on a trade-off between codeword diversity and low cross-correlation. Both of them affect bit error rate. Simulations appear to confirm acceptable bit error rates for candidate OOC codes.

We have discussed collaboration with outside parties for the potential VLSI work (MIT EE), BodyLan applications (MIT Media Lab), and PCMCIA development (Centennial Technologies, IBM Charlotte) and we also plan to contact SystemSoft for PCMCIA collaboration.

Contract No. DABT63-94-C-0017
BodyLan: A Wireless, Body Local Area Network
BBN Reference No.11592

Fiscal Status: July 1, 1994 - September 30, 1994: Report #2

Cost Funds currently authorized	$483,684
Total Estimated Cost	$685,081
Expenditures & commitments as of Sept 30, 1994	$104,986
Estimated cost funds for Completion	$580,095
Estimated Date of Completion	10/31/95

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WAMIS
Principal Investigator Meeting

Working Toward a Micropower, Wireless Body-area LAN

July 24, 1994

Phil Carvey
Bolt Beranek & Newman

What is BodyLAN?

- Augmentation of "Personal Digital Assistant" (PDA)
- BodyLAN is the enabling technology to allow wireless communications between multiple "Personal Electronic Accessories" (PEAs) and a PDA
- BodyLAN physically consists of a PDA interface and one or more PEAs employing BodyLAN technology - sell interface and license technology
- Preliminary list of PEAs:

  - health sensors
  - ring sensors (magnetic &gravitational fields, acoustic rangefinder)
  - sports training aids
  - wristwatch display
  - microphone
  - ear speakers

- Characteristics:

  - short-range wireless communications
  - ultra low power consumption (20-100μWatts)
  - spatial reuse
  - unobtrusive
  - compliance with FCC part 15
  - small, lightweight (i.e. 10s of cubic mm)
  - reasonable cost
  - flexible bandwidth assignment
  - autonomous operation

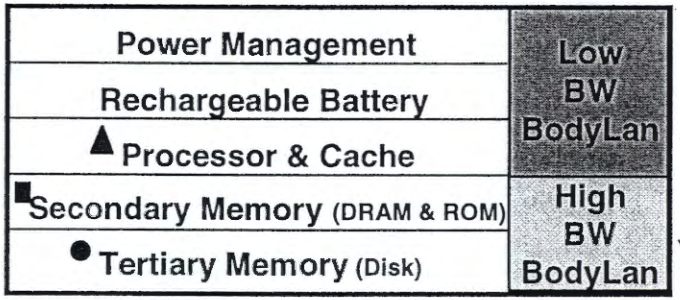
- Currently no established technology to link accessories to processing/data storage

Why Do BodyLAN?

- Provide enabling technology by which new applications (i.e. PDA code & application specific PEAs) can be developed - mimics Workstation/LAN evolution
- Excellent application to drive ultra small size and low power technology
- Dual use technology - e.g. 21st Century Land Warrier program and commercial PDA augmentation
- A need exists to couple human activities and environment to information infrastructure. Multiple sensor finger rings for pointing, virtual key boards, hand signals, 3D form shaping
- Communications & control of PEAs so small or in locations (body cavity) where it is difficult to control
- Locate sensor or transducer in physically optimal location e.g. head of golf club, ear canal, body cavity
- Provide new capability for human interaction with computers - hand gestures, toe taps, eye blinks
- It is technicall very interesting & quite challenging

Body Electronics Model

Ruggedized
Hermetically Sealed PDA



- Low BW Radio
- Heads up display (slow motion)
- Image input
- GPS
- Head orientation, direction, inclination
- Health monitors
- Speech input/output
- Wrist, forearm displays
- Body part tracking, virtual key board
- Wireless conventional laptop components, mouse, keyboard display, disk, printer, scanner, etc.

- ▲ Possibly 2,3 or 4 processors, cache coherent
- ■ 8-16 Mbytes
- ● 400 Mbytes PCMCIA II Size

- Heads up display (full motion video)
- Video input
- High BW radio

High & Low BW BodyLAN

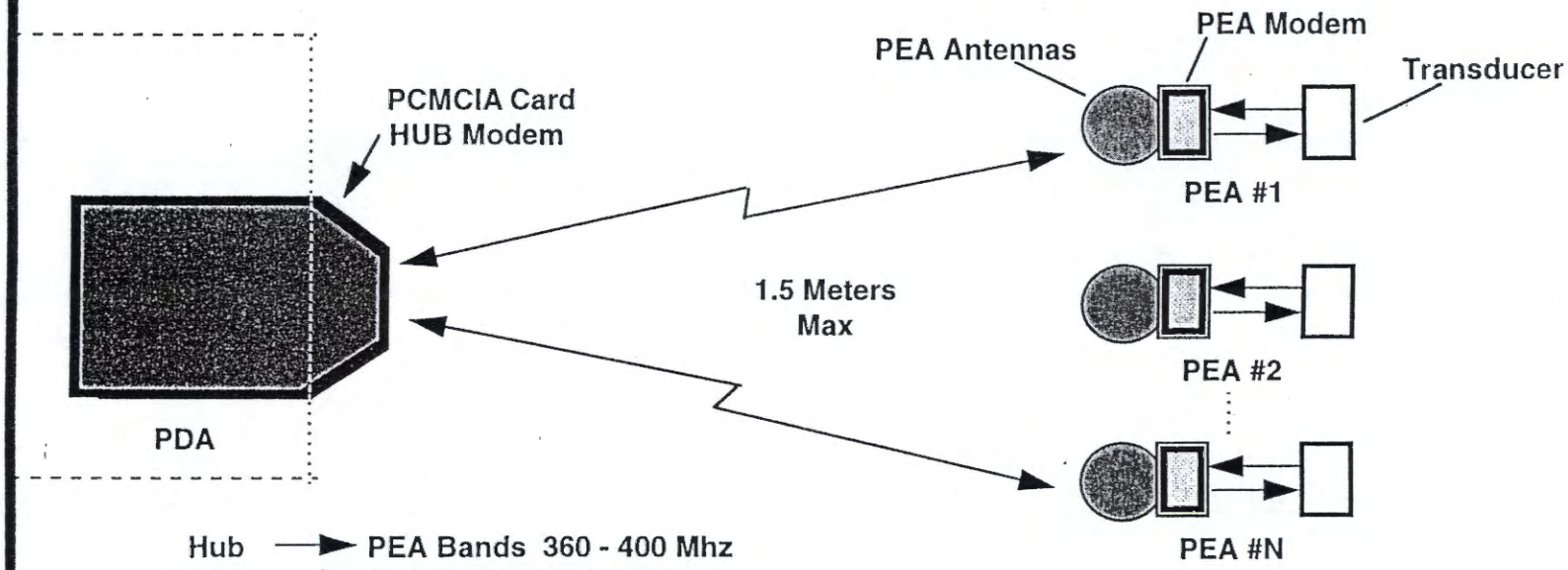
Low BW BodyLAN

- 30-50 Kb/s aggregate BW to/from PDA
- Small size (300mm^3)
- Light weight
- Small antenna size (0.01λ - 0.03λ)
- Wide diversity of PEA BWs
- Desire non-rechargeable operation

High BW BodyLAN

- 2.4 Mb/s aggregate BW to/from PDA - full motion MPEG II compressed video
- Moderate size 125K mm^3
- Moderate antenna size (0.1λ - 0.2λ)
- Small number of high BW PEAs
- Recahrgeable operation OK

BodyLAN Components



Hub → PEA Bands 360 - 400 Mhz
PEA → Hub Bands 320 - 360 Mhz
Conforms to FCC Part 15 Efield Spec
30 Kbps Hub → PEA & 30 Kbps PEA → Hub BW
BW Dynamically assignable
128 PEAS/BodyLAN
Up to 6 Users share a frequency band
Targeting 50 nwatts/bps
Totally autonomous operation
Each BodyLAN has unique transmission codes
Operation modes: unprogrammed, asleep active

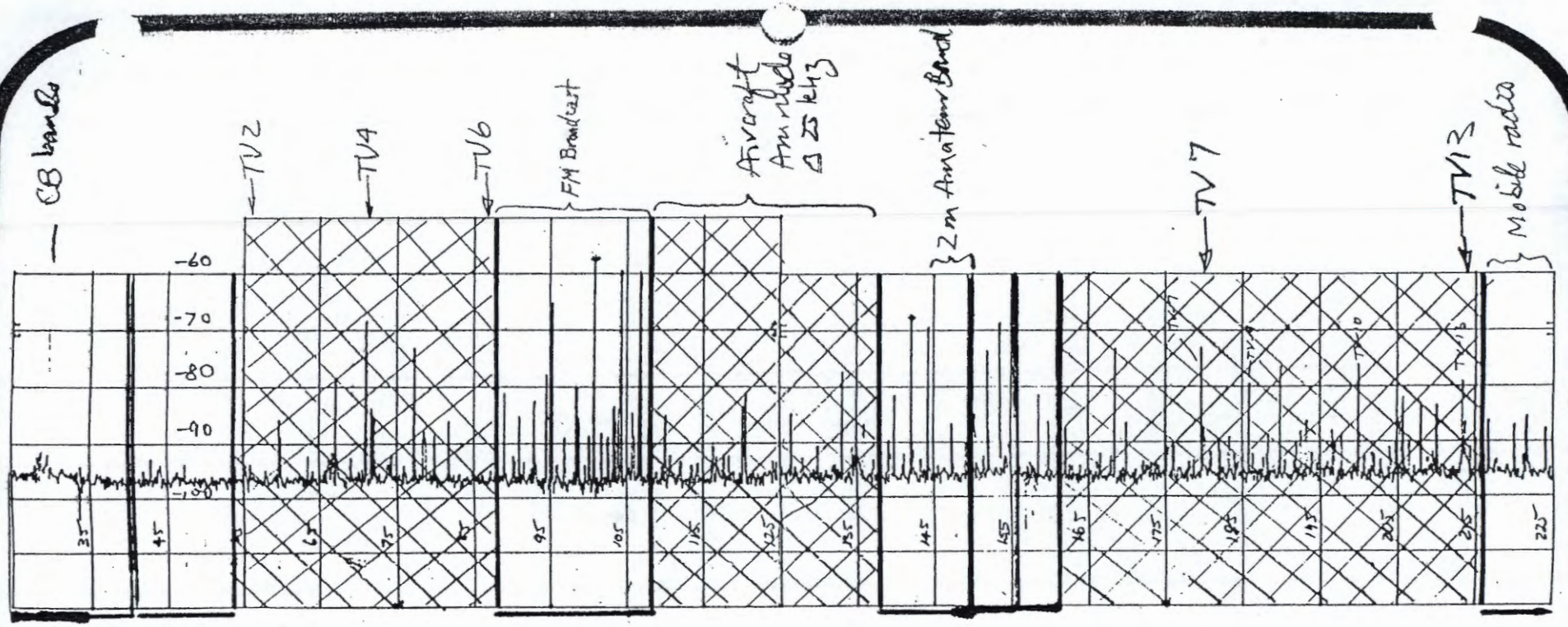
Body LAN Goals

- Demonstrate Technology and Integration
- Feasibility of Low Power, Low Weight, Low Cost Operation
- Coexistence Among Nearby Body LANs (OOC spread spectrum)
- Open and Modular Architecture
- We Will Not Make Sensors/Actuators in This Proposal

FCC Part 15 Specification

- Places limits on radiated power in certain freq. bonds based on Quasi-Peak detector (i.e. low pass filter with 1 msec rise-time, 500 msec fall-time).
- Example @ 400mhz Emax = 200 μV/meter @ 3 meters.
- For Body Lan max distance is 55" = 1.4 meters => max field strength of 3.0/1.4 x 200 = 428 μv/meter
- Exploit Quasi-Peak detection technique by pulsing @ low duty cycles. Eg., for n = 1%, max field strength = 43 mv/meter.

Band (Mhz)	Field Strength (uvolts/meter)	Distance (meters)	Bandwidth (Mhz)	Power (nanowatts)
2.2-8.3	30	30	6.1	27
8.4-13.3	30	30	4.9	27
13.5-25.5	30	30	12.0	27
25.7-30.0	30	30	4.3	27
30.0-37.5	100	3	7.5	3
38.3-54.0	100	3	15.7	3
88.0-108.0	150	3	20.0	7
138.0-149.9	150	3	11.9	7
150.1-156.7	150	3	6.6	7
156.9-162.0	150	3	5.1	7
216.0-240.0	150	3	24.0	7
285.0-322.0	200	3	37.0	12
335.4-399.9	200	3	64.5	12
410.0-470.0	200	3	60.0	12
806.0-960.0	200	3	154.0	12



- 29000 frequency assignment in NE US Police Call Radio guide

Usage	% BW	Actual Usage
TV	41.4	11.4%
Military Aircraft	18.5	1%
Cellular	6.1	6.1%
FM	2	2%

Spectrum Analyzer

9.5"	9.5"

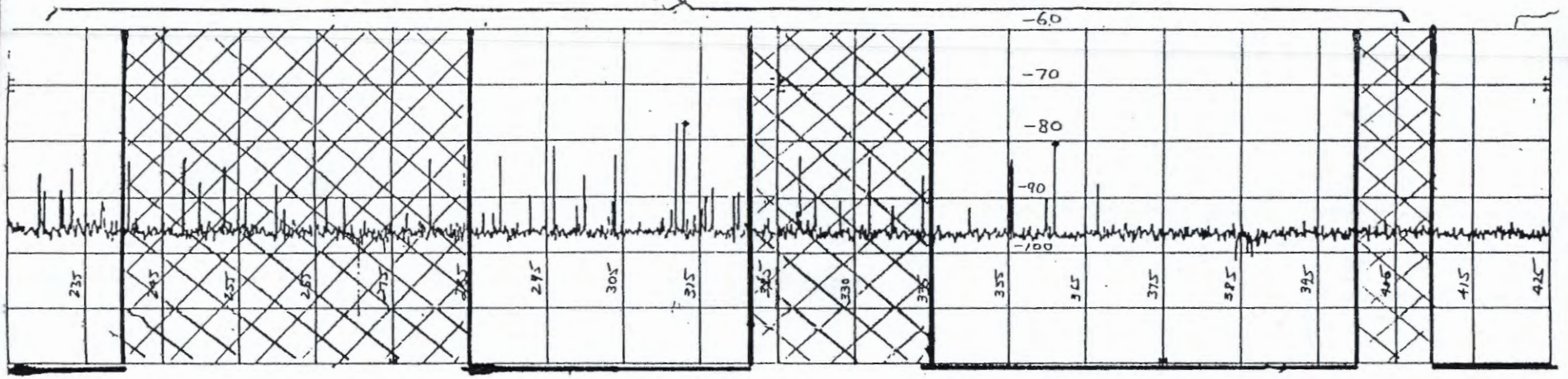
22 gauge wire

Resolution BW 3KHz
Video BW 3KHz
Sweep Time 100ms 22sec
Noise Base -96 Dbm

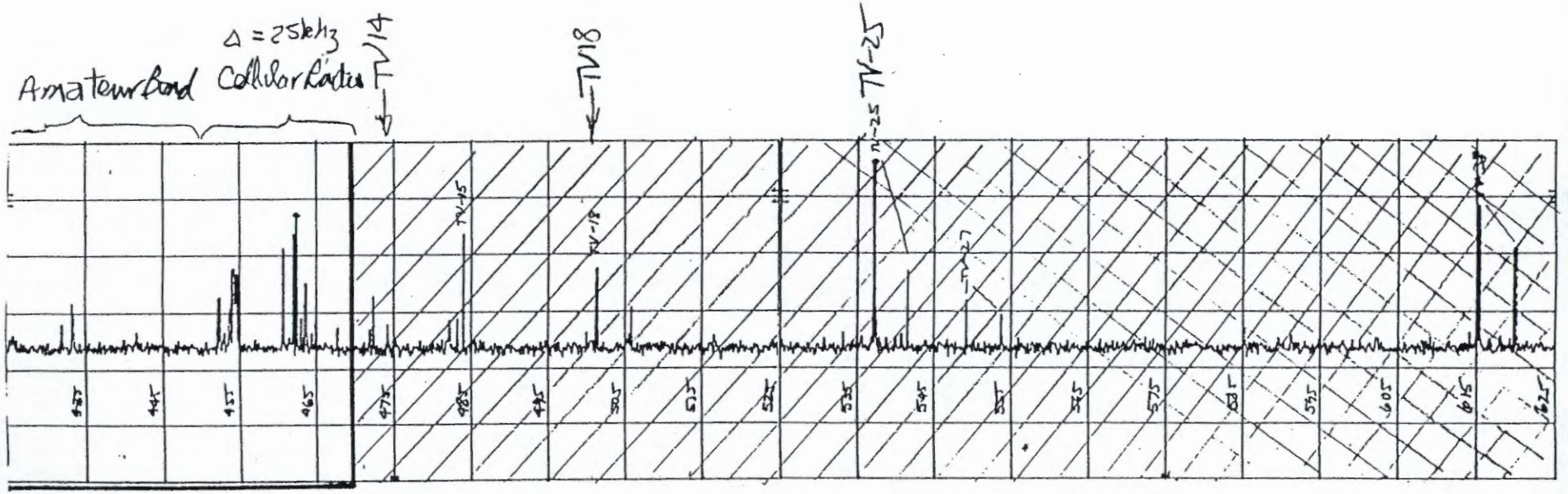
- Receiver not resonant exact @ fm 300 mhz
- Receiver not impedance matched @ any freq
- Antenna not isolated, ie metal reflector in back of antenna
- No Balun connected

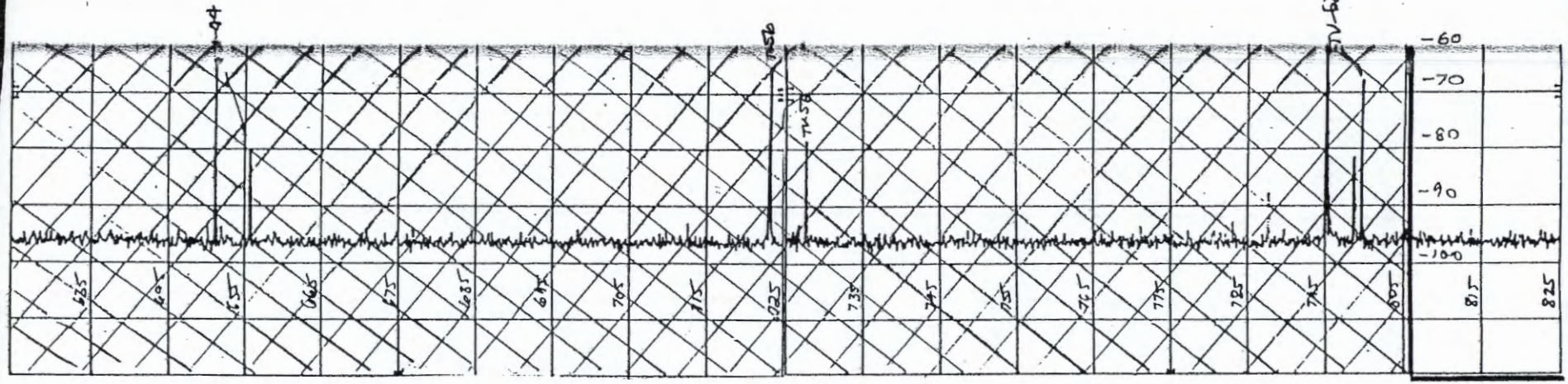
SPECTRUM

Δ = 100kHz
Military Aircraft



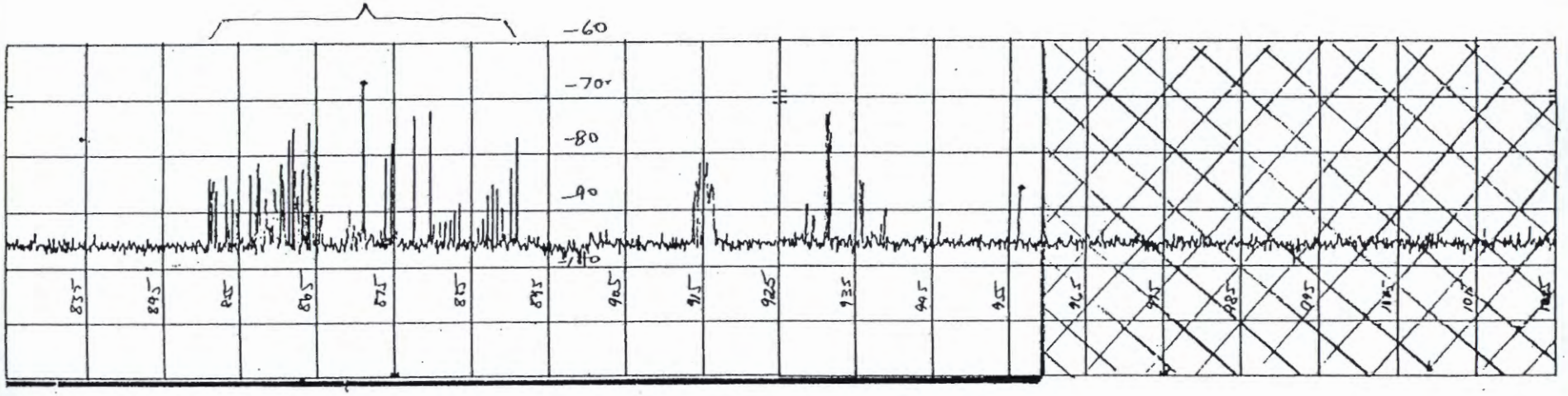
Δ = 25kHz
Amateur Band Cellular Radio





$\Delta = 25\text{kHz}$

Cellular Radio



9C

BodyLAN Solution

BodyLAN Solution

- Exploit close separation of hub & PEAs
- Comply with FCC Field Strength limit opening up large BW < 1 ghz
- Exploit low utilization of military aircraft bands in urban areas
- Design entire wireless protocol for low-power consumption
- Architect signaling protocols for simplicity of implementation
- Trade spectrum usage efficiency for simplicity and low power consumption
- Micro cell architecture like cellular networks but that can move

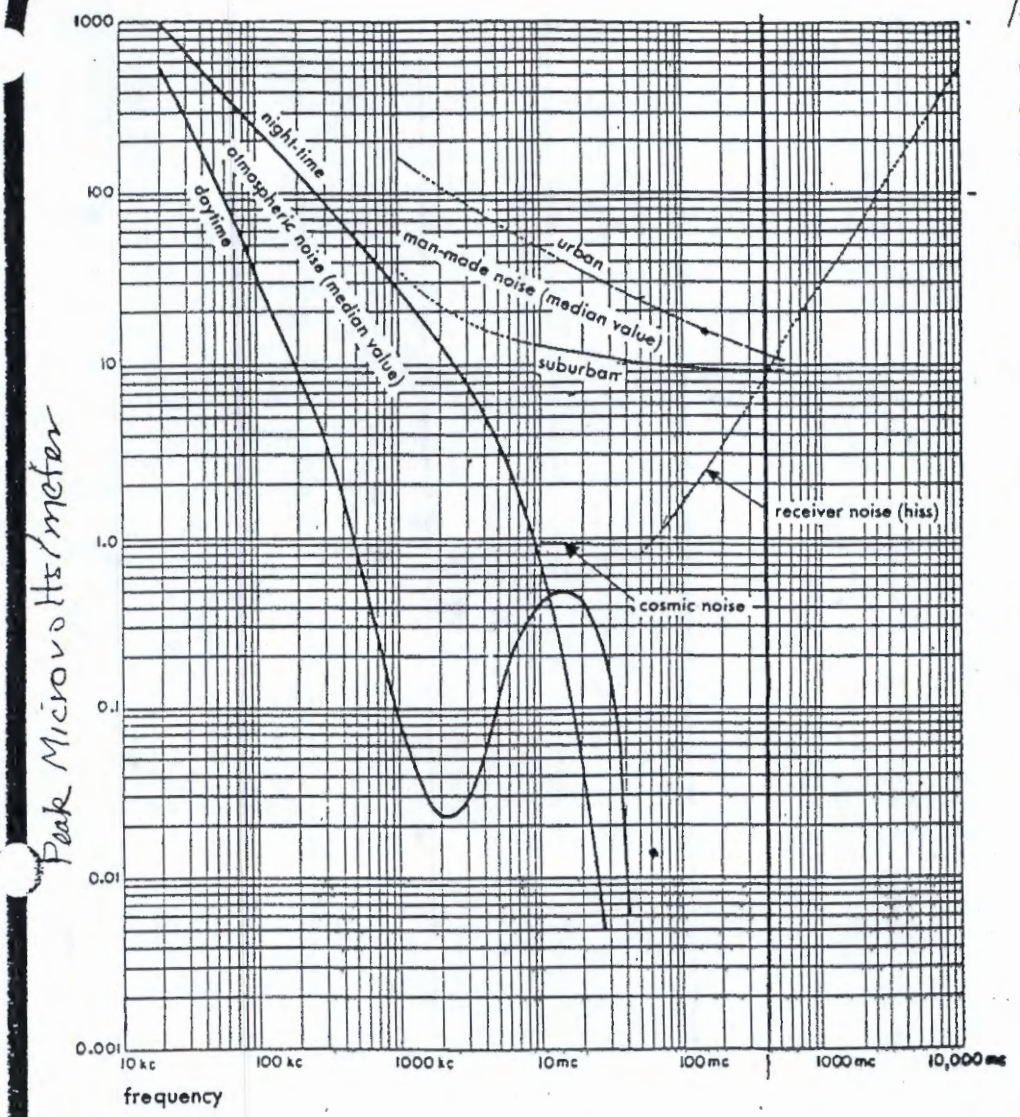
Limited Radiated Field Strength Implications

- FCC limits radiated field strength to 400 μv/m @ 1.5 meter
  - Constant envelope modulation => 12 nwatts radiated power
  - Even at 12% TX efficiency, TX power 100 nwatts
  - TX power consumption is less than watch
- Receivers today consume best case 10-20mw for constant envelope modulation
  - Rx power consumption 200,000 times FCC limited TX power consumption
- Implications
  - Must drastically reduce receiver power consumption

BodyLAN Coexistence With Licensed Transceiver Implications

- Four noise sources for BodyLAN receivers
  - Galactic & man-made noise
  - Thermal noise in receiver & antenna
  - Transmissions from users licensed to bands occupied by BodyLAN receivers
  - Other BodyLANs
- Modem receiver sensitivity of ~1μv for 60khz BW, 10 db Sinad and receiver noise figure, => thermal noise not the problem
- Transmissions from users licensed to use bands typically 20-30 db above thermal & galactic noise floor
- Implications:
  - BodyLAN must use pulsed TX operation to overpower licensed transmitters
  - At 20 to 1 duty cycle, TX power dissipation only 50μw

Noise Sources

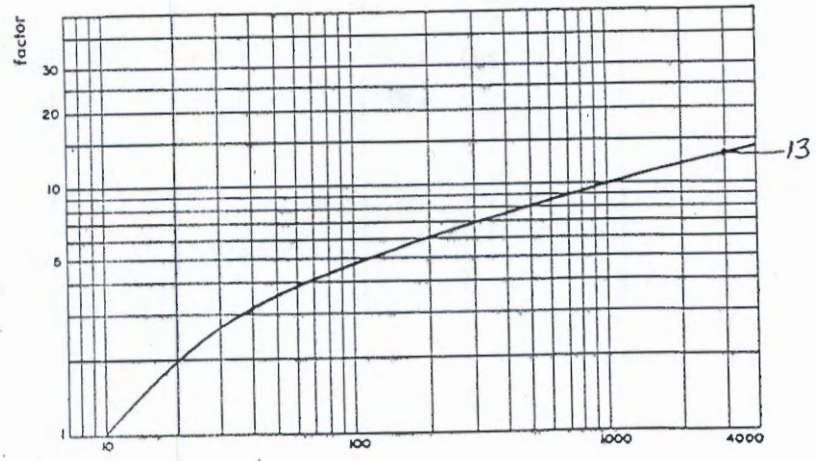


Man Made Noise Srcs
- auto ignition
- electric motor
- high-tension leakage
- electric switching gear
- median values

Noise curves assume
- 10 kHz BW
- use of λ/2 dipole antenna

Example @ 400 mHz
Urban noise 12 μV/meter @ 10 kHz BW
Urban noise 156 μV/meter @ 3000 kHz BW
@ η = 1%

$$SNR = \frac{4300}{156} = 49\,dB$$



Multiply value of man made noise by factor for BW > 10 kHz

Mobile Micro Cell Implications

- BodyLAN really a microcellular architecture having a 3 meter diameter spherical cell
- Different BodyLANs are autonomous cells not having centralized control as cellular networks do
- 4-6 BodyLANs can be in close enough proximity to one another to strongly radiate in each other's frequency band
- A PEA in one BodyLAN can be closer to a foreign hub than its home hub (e.g., shake hands, pat on back)
- BodyLAN interactions are dynamic with little ability to forecast future BodyLAN interactions

- Implications:
  - Can't control foreign BodyLANs frequency band use nor transmission intervals => can't use conventional protocols
  - Can't control which BodyLANs will interact nor the strength of that interaction

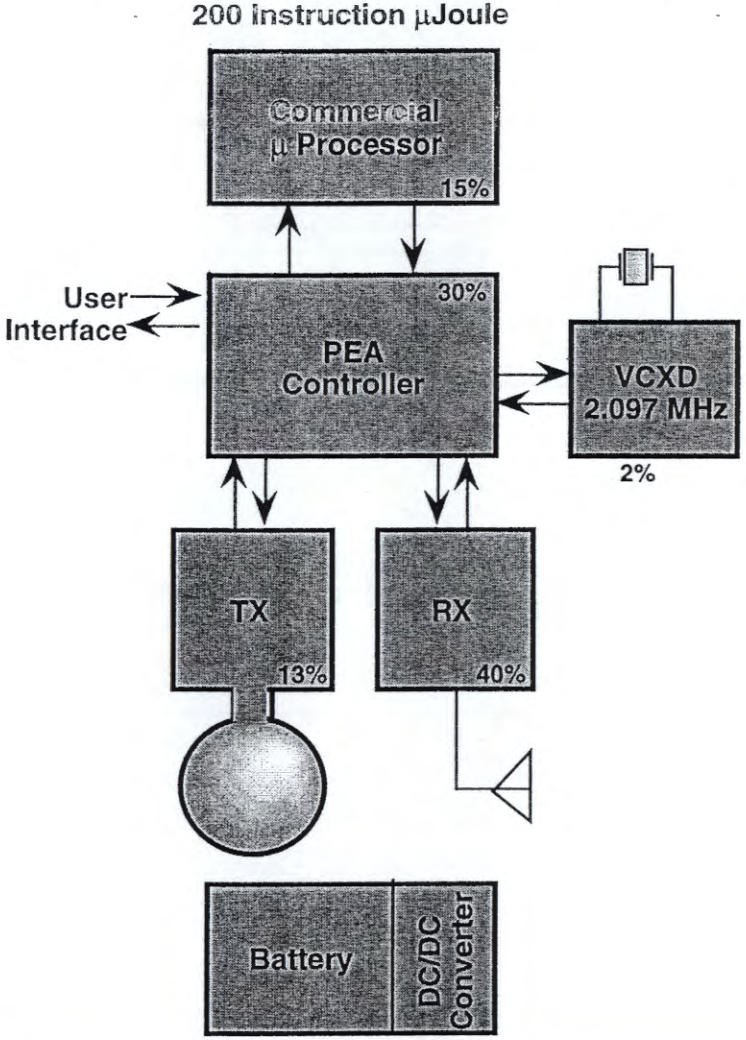
BodyLAN Architecture Assumptions

- Employ slow frequency hopping to avoid bands having high power narrow band transmissions
- Assume dominant noise source is low-power narrow band transmissions and other BodyLANs
- Graceful degradation to 1e-3 acceptible for worst case scenario
- Cannot control or interact dynamically with other BodyLANs for a coordinated spectrum usage - BodyLANs are autonomous
- Target linear relationship of PEA power consumption with data rate @ 3-4 n joules per bit

BodyLAN Foundations

- PEAs synchronize to beacons transmitted by hub modem
  - synchronize to +/- 50 nsec
  - allows efficient TDMA BW sharing scheme
- Employ low duty cycle pulse transmission
  - dramatically reduce power consumption
  - allows power consumption proportional to BW
- Employ simple FSK modulation to simplify RX & TX
  - trade off between BW utlization & simplicity
- Employ simple error correcting codes to correct high symbol error rate for strongly interacting BodyLANs
- Employ optical orthogonal code derivatives to obtain low symbol error rates uses for strongly interacting BodyLANs
- Employ signaling schemes having very high diversity

PEA Modem Block Diagram



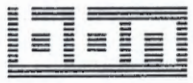
- Vcxo on continuously @ 2.097 MHz frequency locked to Hub
- 200 instructions/microjoule → PEA Controller executes low level functions
- µProcessor handles control of:
  - synchronization acquisition
  - tuning (gain control, filter cut-off)
  - monitoring
  - parameter storage
  - initialization procedure
  - error rate analysis
  - sleep mode control

BodyLAN Symbols

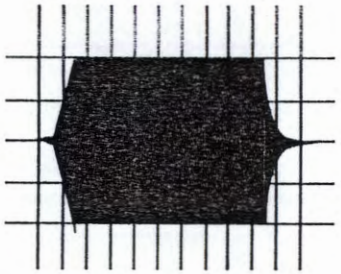
- Symbols are FSK modulated RF bursts
  - ~700 nsec duration with 100 nsec guard intervals at front and back
  - FSK tones at carrier +/- 1.25 Mhz
  - Symbol duration 476.8 nsec
- Employ direct conversion (i.e. $f_o \rightarrow$ DC)
  - 100% tolerant to I & Q channel phase & amplitude errors
  - lowest IF frequency (i.e. DC) => use 1/2 # poles in IF filter at lowest possible power consumption
  - allows simple high BW power detection

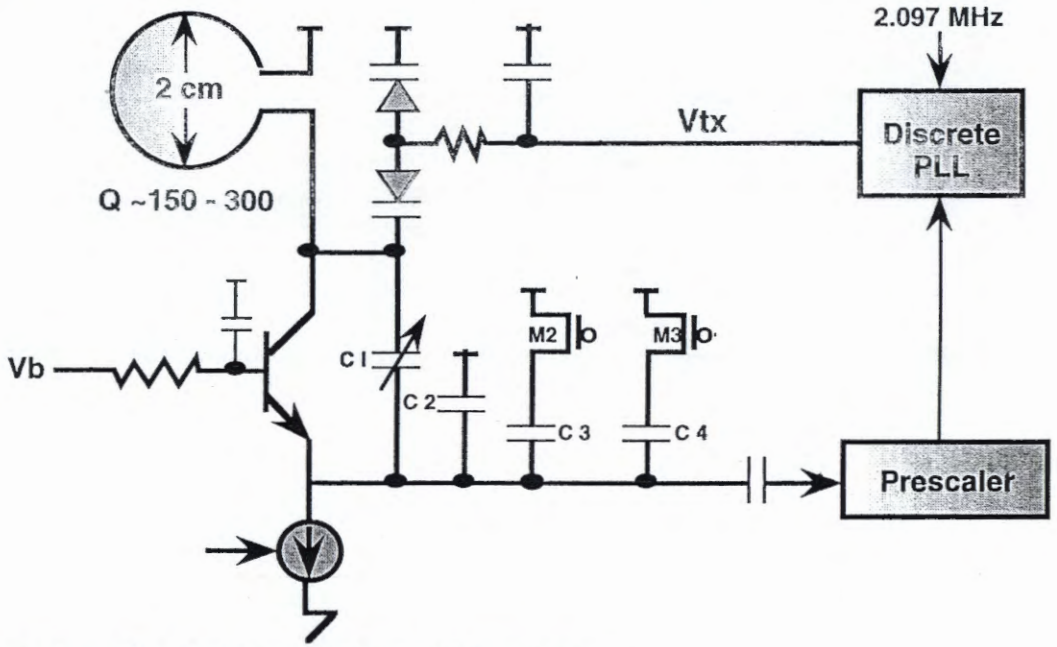
$$\underbrace{(a \sin wt)^2}_{\text{I ch}} + \underbrace{(a' \cos wt)^2}_{\text{Q ch}}$$

  - Provides mechanism for 0, 1, or X detection



BodyLAN Transmitter





- 5K μvolts/meter@ 1.5m 320-360 mhz
- FSK ± 1.25 Mhz
- Resonant frequency stability ± 100 khz
- Tx harmonics < 350 μvolts/meter
- Full power turn on/off <100 nsec
- Power selectability 16 db in 4 steps
- Power consumption < 4 nwatts/bps

Intelligent Protocols for TX & RX Symbols

- Send few symbols as possible because RX power directly proportional to # symbols received per second
  - Block code symbols to allow error connection

$$b_0\ b_1\ b_2\ \ldots b_r \longrightarrow \left\{ \begin{matrix} S_0\ S_1\ S_2\ \ldots\ S\ r+n \\ e_0\ e_1\ e_2 \ldots\ e_{r+n} \end{matrix} \right\} \longrightarrow b_0\ b_1\ b_2\ \ldots b_r$$

  - choose block coding for high symbol error rate channel
- Position symbols in TDMA frame to have low cross correlation with symbols from another BodyLAN

Block Coding

- Simplest scheme, 3 symbols -> 1 bit $\eta = 0.333$
  - no interference detection

    oox, oxo, xoo -> 0
    11x, 1x1, x11 -> 1

    correct single bit error
  - with interference detection

    00I, 0I0, I00 -> 0
    11I, 1I1, I11 -> 1
    0II, 0I0, I00 -> 0
    1II, I1I, II1 -> 1
    III -> Coin Toss
- 4 symbols -> 1 bit $\eta = 0.25$
  - no interference detection, correct all single bit errors, correct half of all double bit errors
  - with interference detection, correct all single, double, triple bit errors, half of all quadruple bit errors
- Larger block codes

			Symbols Corrected	
Block Length	Payload	η	1	2
5	2	0.4	all	half
6	3	0.5	all	half
7	4	0.57	all	half

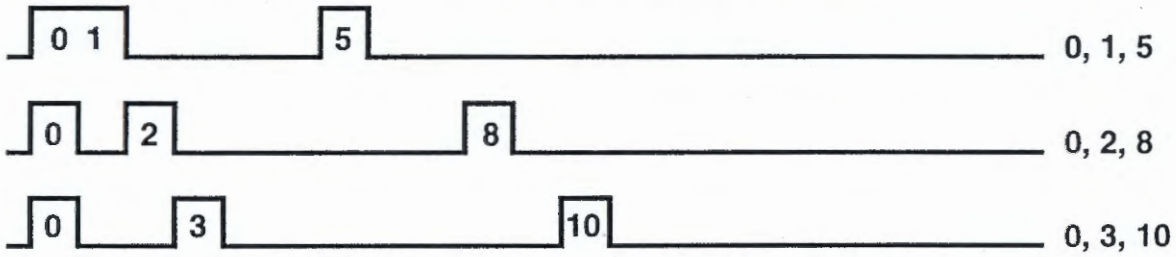
- Now exploring error correction block codes with interference detection

Optional Orthogonal Codes

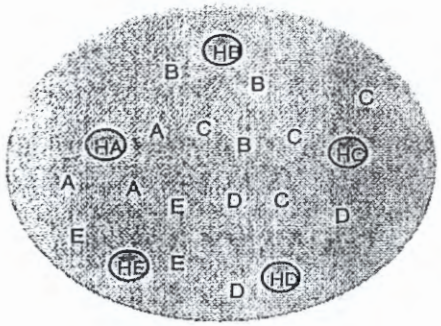
- OOC (n, w, λa, λc) code length η, weight w

Auto correlation	$\sum X_i X_{i+\tau} \leq \lambda a$	$0 < \tau < \eta$, all X in code
Cross correlation	$\sum X_i Y_{i+\tau} \leq \eta c$	$0 < \tau < \eta$, all $X \neq Y$ in code

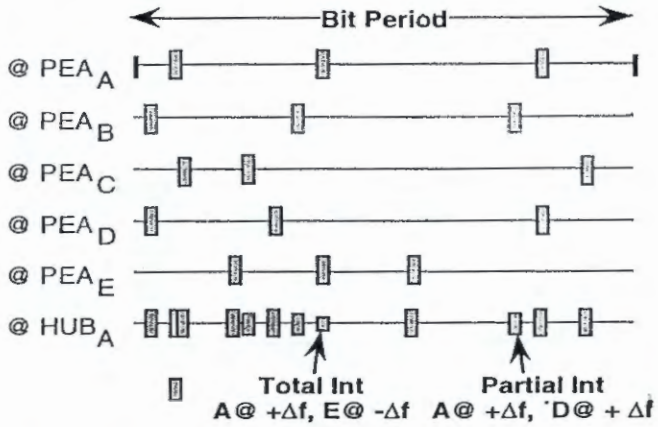
- Have 2 mechanisms for generating OCCs based on "greedy" algorithm & projective geometry
  - Projective geometry generates all possible code words but is limited (i.e. not all n, w..)
  - Greedy algorithm generates about 70% of complex codes (based on Johnson bound)
- Example $\eta = 19$, $w = 3$ $\lambda = 1$ optimal codes



BodyLAN Interference

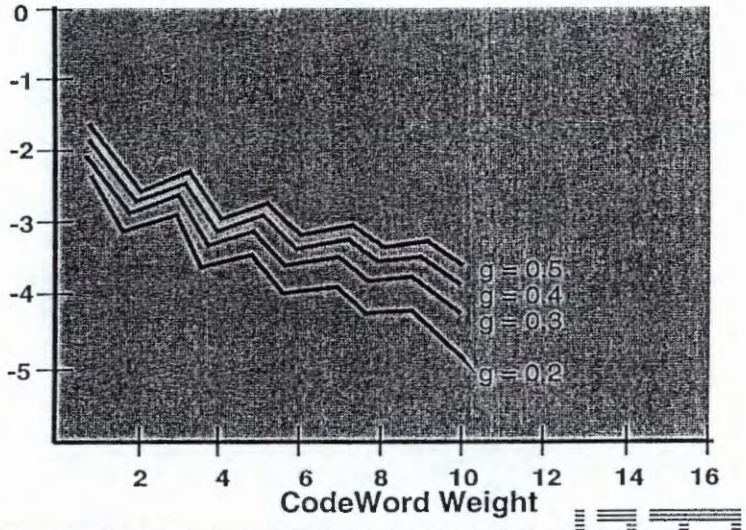


Five Interfering Body LANs
Sharing the Same Freq Bands



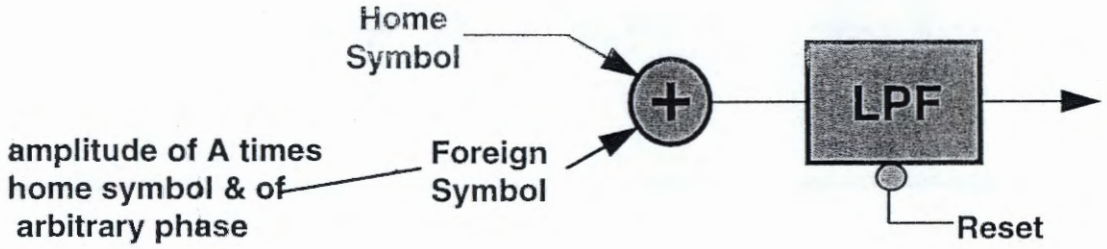
Assume:

- (64, W, 1) OOC
- Max Data Rate on All Body LANs
- Five Interfering Body LANs
- Interference Probability Pi



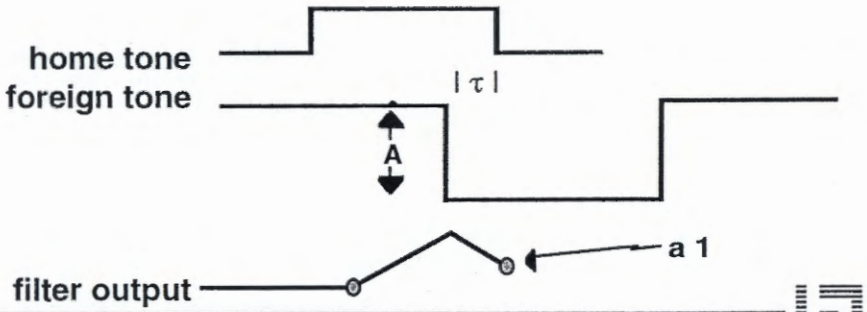
BodyLAN Interference Model Simulation

- Assume (63, 3, 1) OCC, block size = 3, η = 0.333 & additive channel



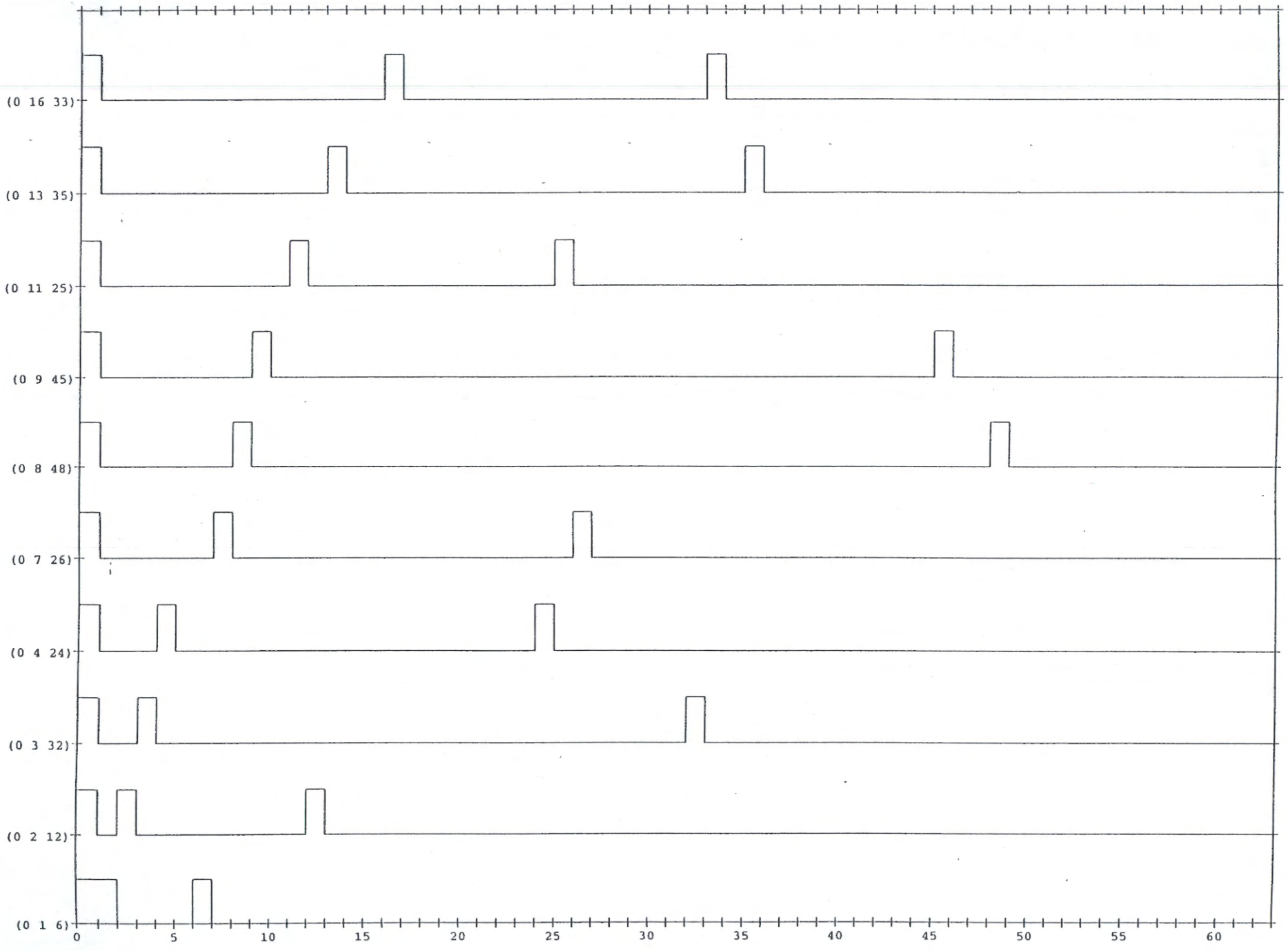
- Descrete model
  - when same tone => 0 error rate
  - when different tone => errors occur only when A > 1 because of FM capture effect

- Analog model



Symbol error
when $\tau \cdot A > 0.5$

One OOC Code Set of type {63,3,1}



EXPECTED BIT ERROR RATES
Modeled: one code being interfered with by one other

Codes: {63,3,1} padded to 64 with a trailing zero
The 1st-listed code is the desired signal, the 2nd-listed is the interferer.
The power ratio, interferer/desired, is shown in row 0.

Code pair	0.10000	0.21544	0.46416	1.00000	2.15443	4.64159	10
1-2	0.00000	0.00000	0.00000	0.00000	0.00078	0.00391	0.00547
1-3	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
1-4	0.00000	0.00000	0.00000	0.00000	0.00078	0.00391	0.00547
1-5	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
1-6	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
1-7	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
1-8	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
1-9	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
1-10	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
2-1	0.00000	0.00000	0.00000	0.00000	0.00078	0.00391	0.00547
2-3	0.00000	0.00000	0.00000	0.00000	0.00078	0.00391	0.00547
2-4	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
2-5	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
2-6	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
2-7	0.00000	0.00000	0.00000	0.00000	0.00078	0.00391	0.00547
2-8	0.00000	0.00000	0.00000	0.00000	0.00078	0.00391	0.00547
2-9	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
2-10	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
3-1	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
3-2	0.00000	0.00000	0.00000	0.00000	0.00078	0.00391	0.00547
3-4	0.00000	0.00000	0.00000	0.00000	0.00078	0.00391	0.00547
3-5	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
3-6	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
3-7	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
3-8	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
3-9	0.00000	0.00000	0.00000	0.00000	0.00859	0.01172	0.01328
3-10	0.00000	0.00000	0.00000	0.00000	0.00078	0.00391	0.00547
4-1	0.00000	0.00000	0.00000	0.00000	0.00078	0.00391	0.00547
4-2	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
4-3	0.00000	0.00000	0.00000	0.00000	0.00078	0.00391	0.00547
4-5	0.00000	0.00000	0.00000	0.00000	0.00078	0.00391	0.00547
4-6	0.00000	0.00000	0.00000	0.00000	0.00859	0.01172	0.01328
4-7	0.00000	0.00000	0.00000	0.00000	0.00078	0.00391	0.00547
4-8	0.00000	0.00000	0.00000	0.00000	0.00078	0.00391	0.00547
4-9	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
4-10	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
5-1	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
5-2	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
5-3	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000	0.00000
5-4	0.00000	0.00000	0.00000	0.00000	0.00078	0.00391	0.00547

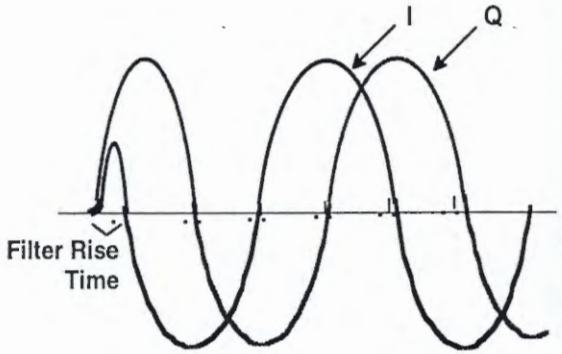
Bit Error Rates
OOC Code {63,3,1}
Power ratio (interferer/desired) = 10.0

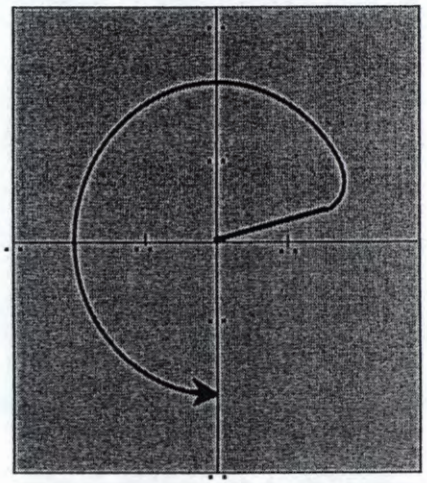
0 Code	1	2	3	4	5	6	7	8	9	10	11 MEAN B.E.R.
1 (0 1 6)	0.0135	0.0056	0.0000	0.0056	0.0000	0.0000	0.0000	0.0000	0.0000	0.0000	0.0025
2 (0 2 12)	0.0056	0.0135	0.0056	0.0000	0.0000	0.0000	0.0056	0.0056	0.0000	0.0000	0.0036
3 (0 3 32)	0.0000	0.0056	0.0135	0.0056	0.0000	0.0000	0.0000	0.0000	0.0056	0.0111	0.0041
4 (0 4 24)	0.0056	0.0000	0.0056	0.0135	0.0056	0.0056	0.0000	0.0056	0.0000	0.0000	0.0041
5 (0 7 26)	0.0000	0.0000	0.0000	0.0056	0.0135	0.0056	0.0111	0.0056	0.0000	0.0000	0.0041
6 (0 8 48)	0.0000	0.0000	0.0000	0.0056	0.0056	0.0135	0.0056	0.0056	0.0000	0.0056	0.0041
7 (0 9 45)	0.0000	0.0056	0.0000	0.0000	0.0111	0.0056	0.0135	0.0000	0.0000	0.0056	0.0041
8 (0 11 25)	0.0000	0.0056	0.0000	0.0056	0.0056	0.0056	0.0000	0.0135	0.0056	0.0000	0.0041
9 (0 13 35)	0.0000	0.0000	0.0056	0.0000	0.0000	0.0000	0.0000	0.0056	0.0135	0.0000	0.0025
10 (0 16 33)	0.0000	0.0000	0.0111	0.0000	0.0000	0.0056	0.0056	0.0000	0.0000	0.0246	0.0047

OOC Code {63,3,1}
ROW R COL C shows the inner product of the vectors in ROW R and ROW C

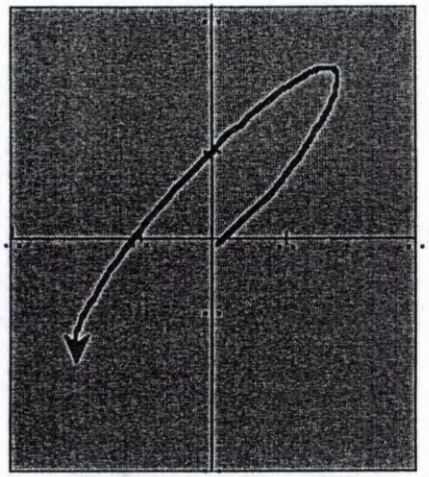
0 Code	1 Vector	2	3	4	5	6	7	8	9	10
1 0 1 6	1, 1, 0,	1	1	1	1	1	1	1	1	1
2 0 2 12	1, 0, 1,	...	1	1	1	1	1	1	1	1
3 0 3 32	1, 0, 0,	...	...	1	1	1	1	1	1	1
4 0 4 24	1, 0, 0,	...	...	...	1	1	1	1	1	1
5 0 7 26	1, 0, 0,	...	...	...	...	1	1	1	1	1
6 0 8 48	1, 0, 0,	...	...	...	...	...	1	1	1	1
7 0 9 45	1, 0, 0,	...	...	...	...	...	...	1	1	1
8 0 11 25	1, 0, 0,	...	...	...	...	...	...	...	1	1
9 0 13 35	1, 0, 0,	...	...	...	...	...	...	...	...	1
10 0 16 33	1, 0, 0,	...	...	...	...	...	...	...	...	...

Interference of Two BodyLANs

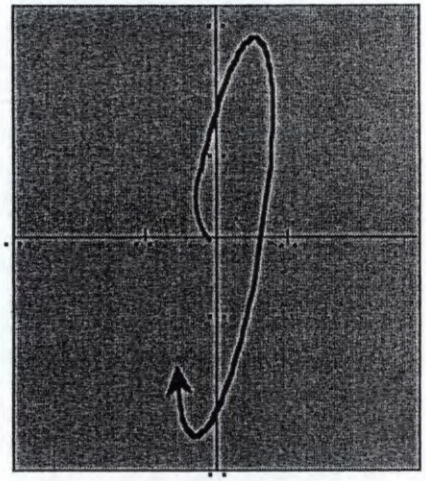




With no interference
symbol time ≥ 0.3 λ



F_1+ weak F_0



F_1+ strong F_0

With interference
symbol time ≥ 0.6 λ

Lower ΔF ->
- less noise
- lower power
- tighter Rx & Tx freq control

Protocol Enhancements

Tx using original OOC proposal

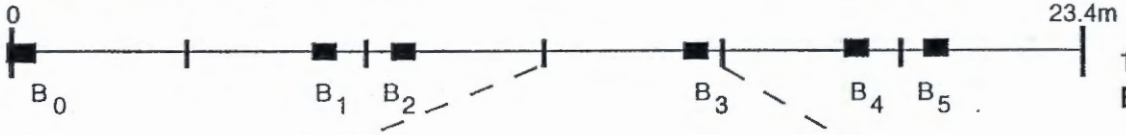
- Tx RF bursts only for ones, nothing for zeros
- 1/2 transmit power
- Fewer interfering bursts -> lower error rate
- Requires detection of no power transmitted in presence of noise

Sense pulse interference

- For each chip sense 0, 1, or I
- For (64, W, 1) code get large reduction in error rate, can sustain interference in all but one of W chips
- Matched filter for synchronization uses less power
- Requires detection of interference -> more complexity

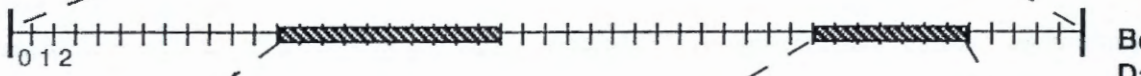
Frame Format

Super Frame = 6 Sub Frames



120^5 = 2.5E10
Beacon Position Codes

Frame = 128 Bits

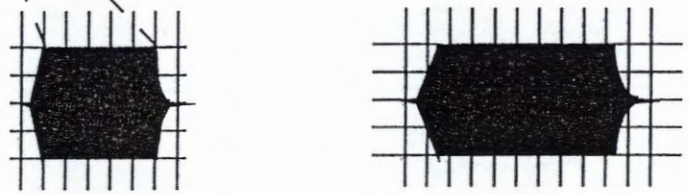


Beacon Position & Uses Data Within Subframe Programmable

Bit = 64 Chips

- 40 Bursts/Beacon
- First 38 Bursts transmitted with BodyLAN ID
- 2 ^ 38 = 2.7E11 IDs
- Last 2 Bursts for Fine Synchronization

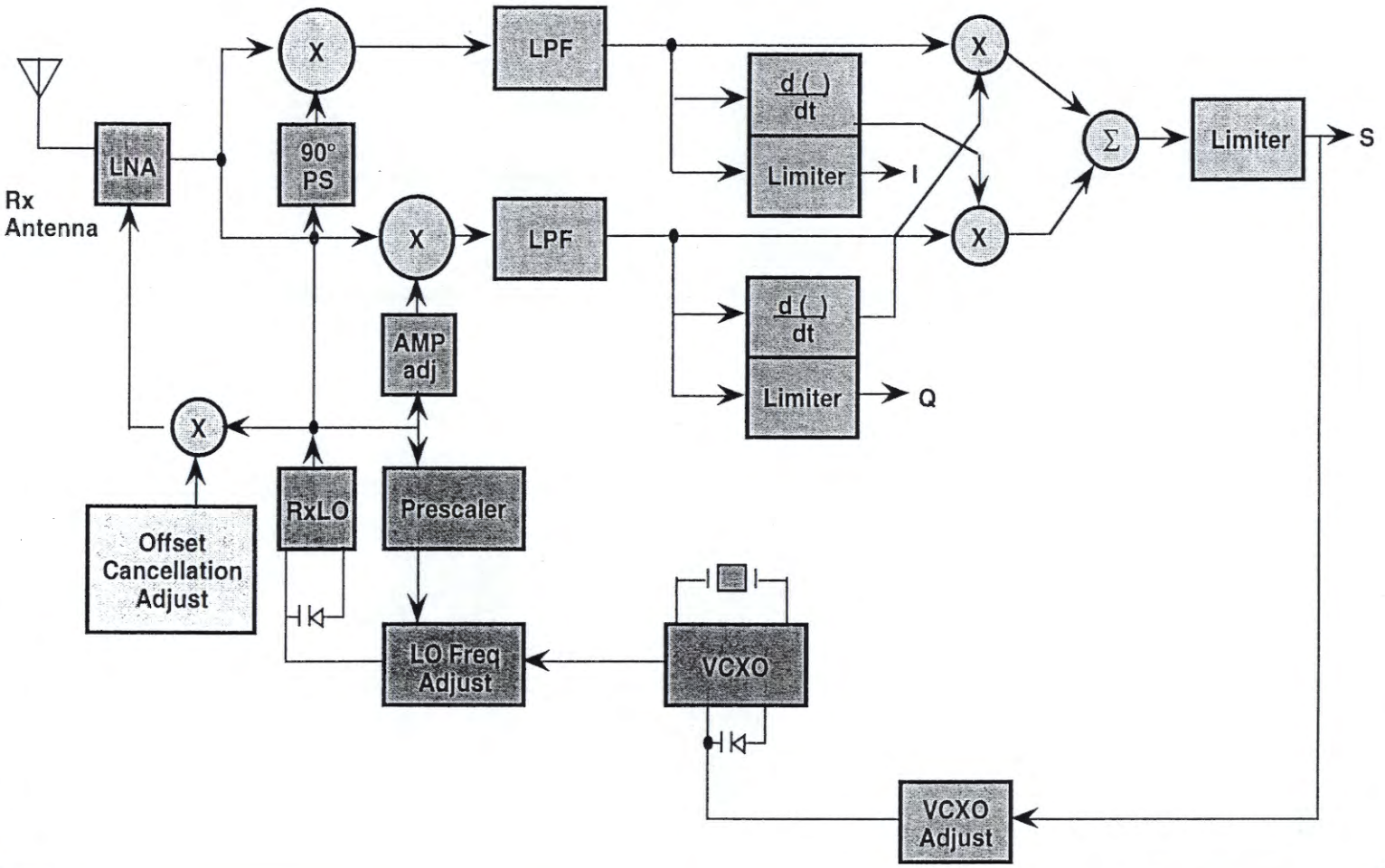
- Bursts within bit form (64,W,1) OOC
- Choose 1 of U Code words with 0-63 bit cycle rotation every bit period based on PRN seeded @ start of frame



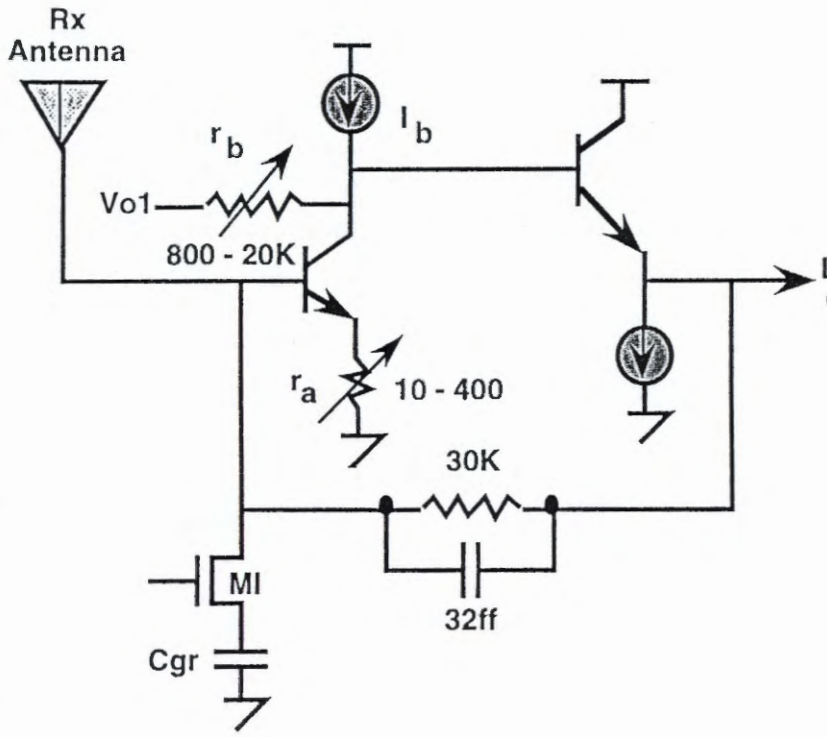
Burst @ fo ± Δf

Burst @ fo-Δf @ fo+Δf

BodyLAN Receiver RF

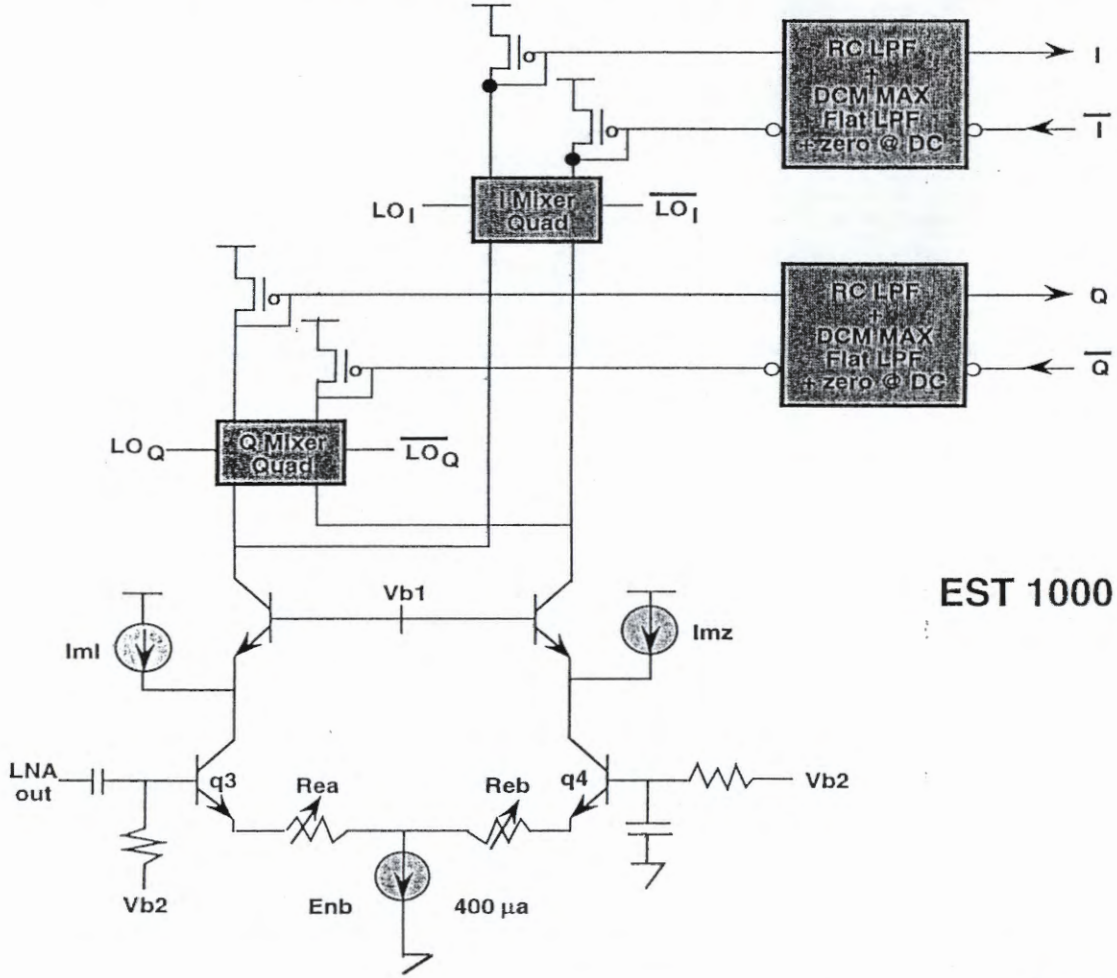


LNA With Gain Control



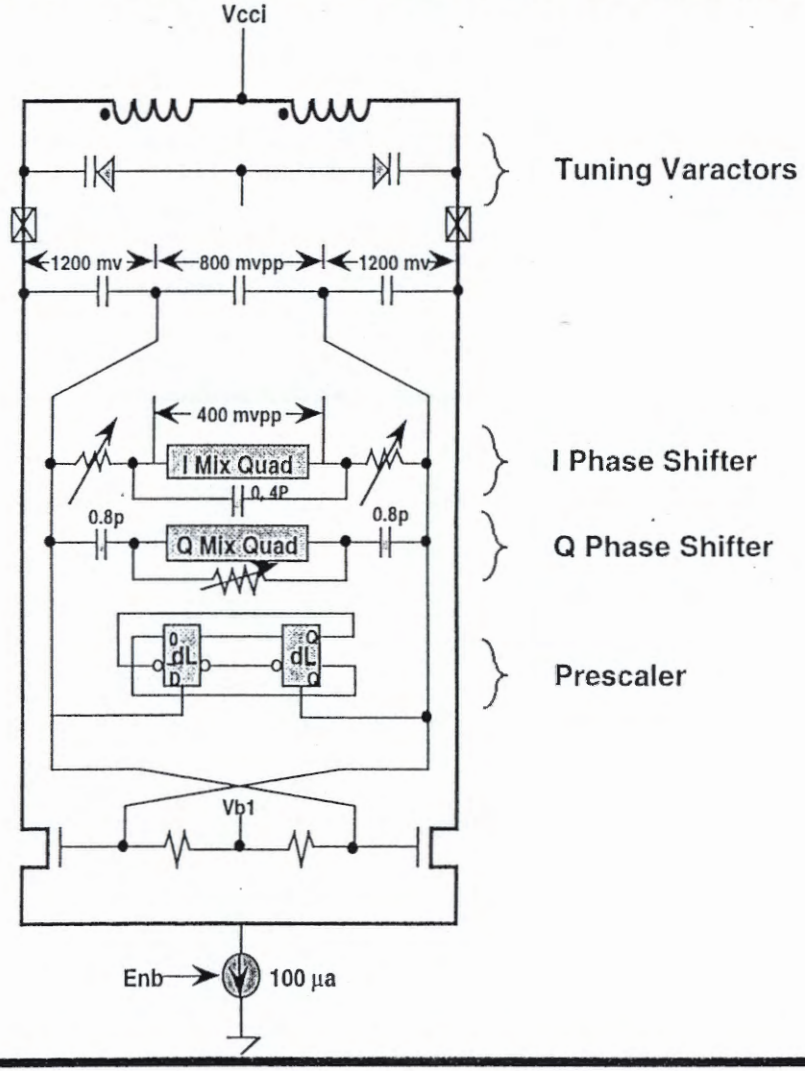
- With Ib = 200 μa, Rb = 180 Ω
  - Gain = 14.5 dB
  - en = 2.5 nVolt per root hertz
- Gain control 22 dB
- At max gain
  - dynamic range 58 dB @ 12 dB Sinad
  - 4 volts meter max E field
- At min gain
  - dynamic range 80 dB @ 12dB Sinad
  - 50 volts/meter max E Field

BodyLAN Mixer & Filter



EST 1000 µa

Receiver Local Oscillator



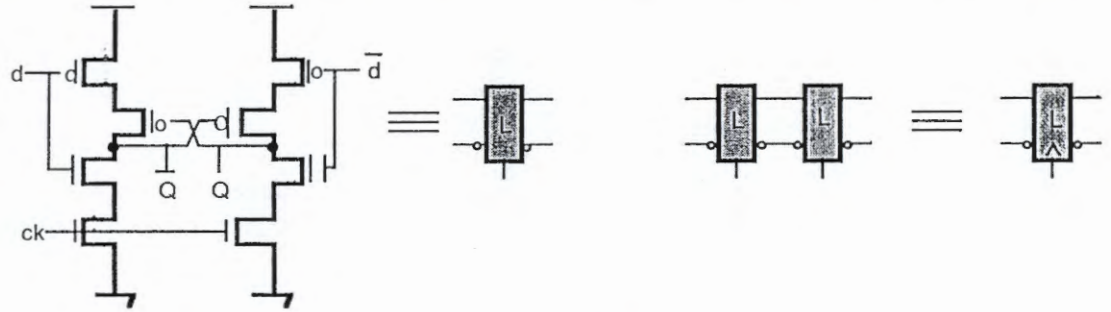
Tuning Varactors

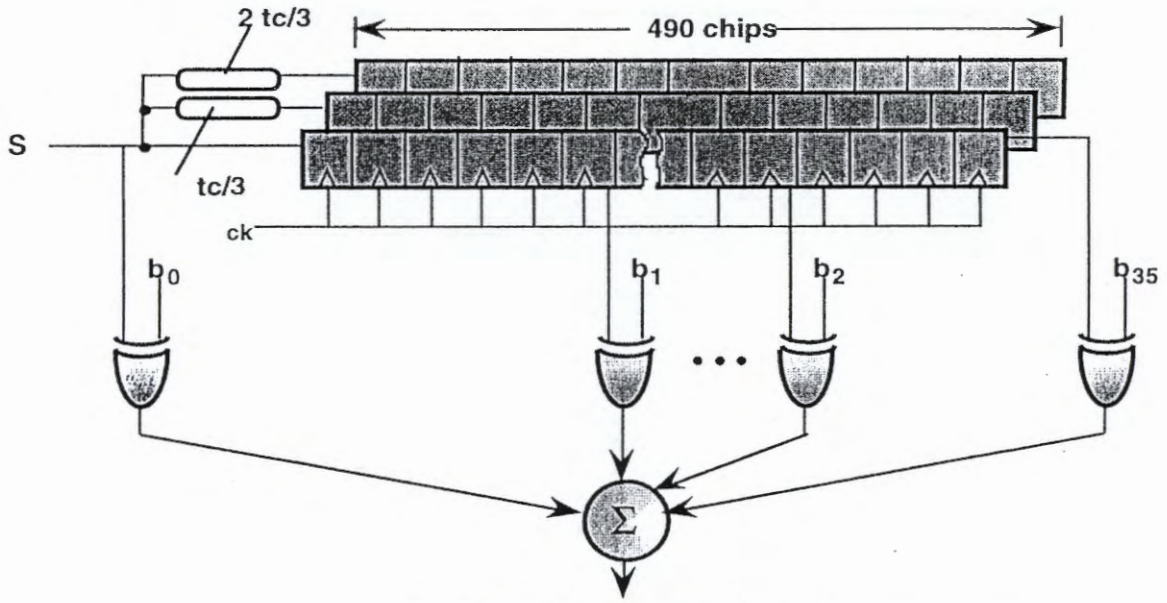
I Phase Shifter

Q Phase Shifter

Prescaler

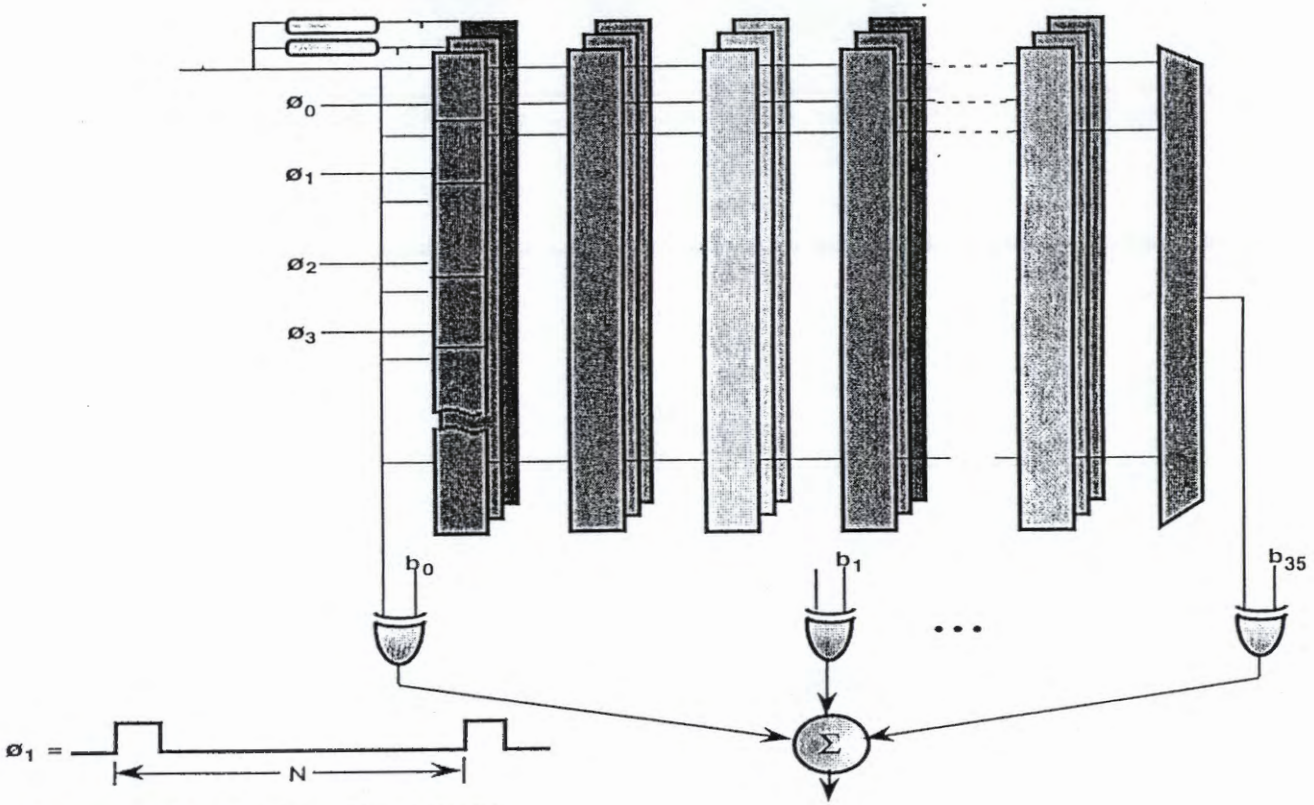
Beacon Digital Matched Filter





$\Sigma \geq 38$ - # allowed errors $\Rightarrow$ match
Power ~ 750μwatts

Low Power Beacon Matched Filter

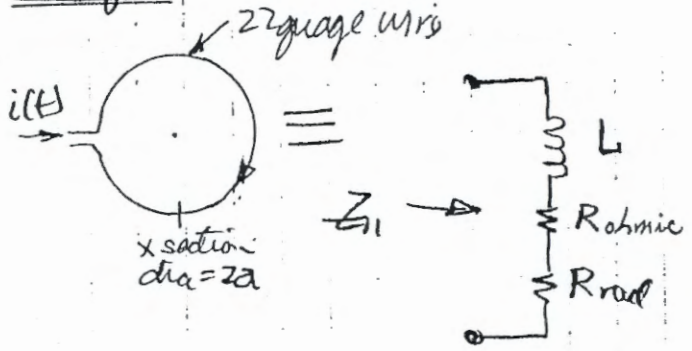


Power∝ (10 + N + log N + 1470/N)

EST 50 μw for N = 32

16 sq/1K", 25,35 mils dia

Loop



$$Z_{11} = j R_{11}\left[4\pi\, e\text{-}7\, h/m\left[\ln 8\left(\frac{2R}{2a}\right) - 2\right]\omega + R_{\Omega} + R_{rad}\right.$$

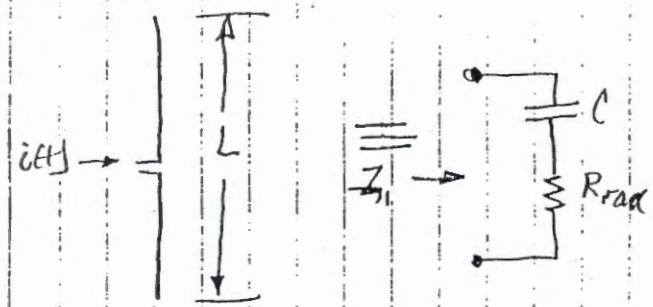
$$R_{rad} = 31200\left(\frac{\pi R^2}{\lambda^2}\right)^2 = 197\, C_{\lambda}^4$$

eg $f_o = 390\,mhz \Rightarrow \lambda = 0.769\,m$
2 cm dia loop
$L = 44\,nh$
$R_{RAD} = 0.00881\,\Omega$

$R_{ohmic} = 0.51\,\Omega$ (includes skin effect)

$$E_{\phi} = \frac{120\pi^2 I \sin\theta}{r}\,\pi\left(\frac{R}{\lambda}\right)^2$$

Center Fed Dipole



$$E_\phi = j\frac{60\pi I \sin\theta}{r}\quad \frac{L}{\lambda}$$

$$Z_{11} = 30\,[\,Cm(2\pi n) + j\,Si(2\pi n)\,]$$

(cosine & sine integrals)

for $L = n\lambda/2$

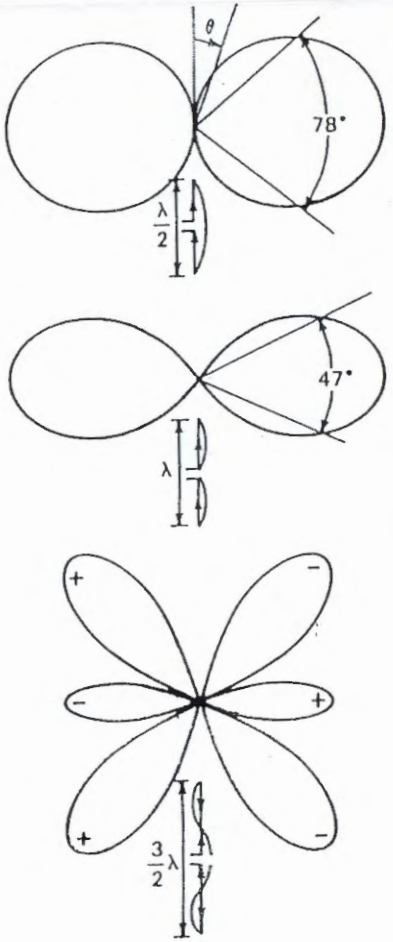
eg(1) $L = \lambda/2$ $\quad Z_{11} = 73 + j\,42.5\ \Omega$

$L = 3\lambda/2$ $\quad Z_{11} = 105.5 + j\,45.5$

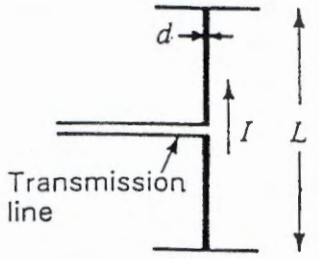
eg(2) $L \ll \lambda$ $\quad R_{11} = 197\left(\frac{L}{\lambda}\right)^2$

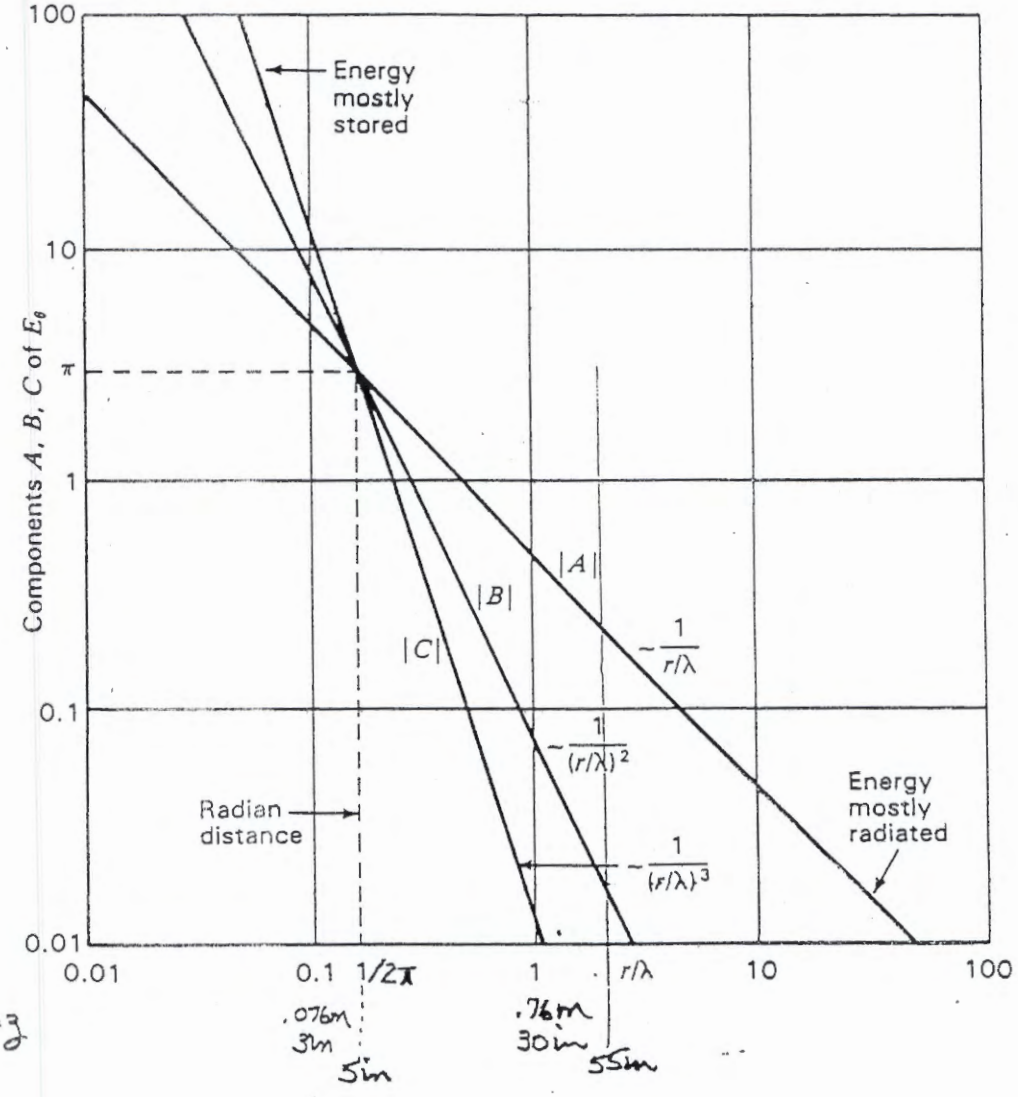
$L = 2cm$ $\quad R_{RAD} = 0.133\ \Omega$

@ $f_0 = 390\,mhz$



NEAR FIELD / FAR FIELD





@390Mhz

.076m 3in 5in

.76m 30in 55in

$$E_r = \frac{[I]L_\lambda Z \cos\theta}{\lambda}\left[\frac{1}{2\pi r_\lambda^2} - j\frac{1}{4\pi^2 r_\lambda^3}\right]$$

$$E_\theta = \frac{[I]L_\lambda Z \sin\theta}{\lambda}\left[j\overset{A}{\frac{1}{2r_\lambda}} + \overset{B}{\frac{1}{4\pi r_\lambda^2}} - j\overset{C}{\frac{1}{8\pi^2 r_\lambda^3}}\right]$$

$$H_\phi = \frac{[I]L_\lambda \sin\theta}{\lambda}\left[j\frac{1}{2r_\lambda} + \frac{1}{4\pi r_\lambda^2}\right]$$

Near Field Far Field Issue

For a short dipole $\mathcal{E}_\theta = \frac{IL}{\lambda^2}\left[\frac{j\lambda}{2\pi r} + \frac{\lambda^2}{4\pi r^2} - \frac{j\lambda^3}{8\pi^2 r^3}\right]$

@ 8 mhz $\lambda = 37.5$ meters $\Rightarrow \frac{\lambda}{2\pi} = 6$ meters $= 19.5'$

$\mathcal{E}_\theta = \frac{IL}{\lambda^2}\left[\frac{j\lambda^3}{8\pi^2 r^3}\right] = \frac{jIL\lambda}{8\pi^2 r^3}$ (near field)

$\mathcal{E}_\theta(1 \text{ meter}) = -j\,0.475\,IL$

$\mathcal{E}_\theta(1.4 \text{ meters}) = -j\,0.173\,IL$

- FCC part 15 300 μV/m @ 3 meters
- Coupling between multiple body loops drops off @ $\frac{1}{r^3}$
- Little used bands
- Cannot use spread spectrum

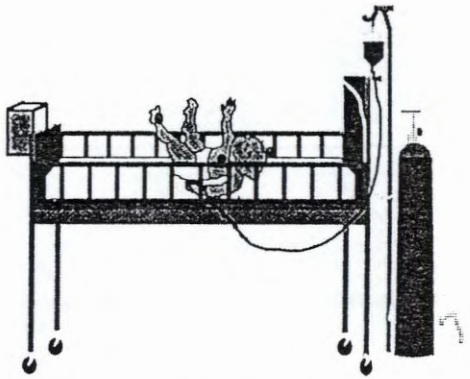
@ 400 mhz $\lambda = 0.75$ meters $\Rightarrow \frac{\lambda}{2\pi} = 0.119$ meters $= 4.7''$

$\mathcal{E}_\theta = \frac{IL}{\lambda^2}\left[\frac{j\lambda}{2r}\right] = j\frac{IL}{2\lambda r}$ (far field)

$\mathcal{E}_\theta(1 \text{ meter}) = j\,0.667\,IL$

- FCC part 15 200 μV/m @ 3 meters
- Coupling between multiple body loops drops off @ $\frac{1}{r}$
- Military aircraft band little used
- Use spread spectrum

BodyLAN Applications



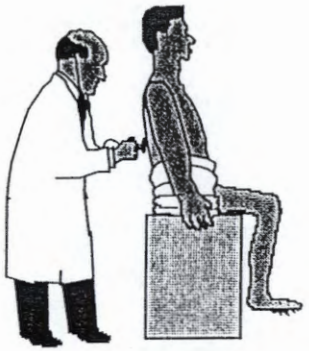
Neonatal Monitoring

Workstation Input Enhancement

Mobile Computing

Sports Training

Military



Medical Monitoring

HUB INTERFACE SPECIFICATION

1. Introduction

The PCMCIA card Hub Interface (HI) provides synchronous communications channels between the HI and one or more Personnel Electronic Assesoriry (PEA) Modems. In addition to this basic communication capability, the HI provides ancillary command and control mechanisms needed for HI and PEA configuration, PEA discovery, and monitoring. The hub interface specification was developed in cooperation with BBN Systems and Technologies to satisfy the following primary objectives:

* Provide simplex or full-duplex synchronous communications between the hub and PEA modems at baud rates from 32 b/s to 28.672 Kb/s in increments of 32 b/s.
* Allow TDMA configuring of up to 63 PEAs to share the separate Tx and Rx frequency band in any bit rate combination up to the maximum.
* Provide mechanisms for personalizing each BodyLan such that different BodyLans may share the same physical domain.
* Provide mechanisms for rapid changing the bandwidth assignments.

BodyLan communication protocols are based on a TDMA frame of 31.25 miliseconds partitioned into 1024 bit transmission intervals in both the Tx and Rx channels. Of these 1024 bits per frame, 64 are exclusively used by the hub to broadcast synchronization beacons to all PEAs. In addition, 64 are used by both the HI and PEA modems for out-of-band control signaling. Since PEAs are not allowed to both transmit and receive simultaneously, the 2048 b/s communication capability from PEA to hub during synchronization beacon broadcast and for the 1024 b/s bidirectional command and control channel is not available for user communication.

Beacons received by the PEAs are used to establish synchronization between the all PEAs in one BodyLan and its HI. This allows TDMA data communication between PEA modem and hub modem thus enabling almost total power-down operation between chip transmission/reception. For a PEA having a 2048 b/s unidiretional communication channel to the HI for example, this results in about a 450 to one power consumption reduction.

A single bi-directional command and control channel is shared between the hub and all PEAs. This channel provides a means for the hub to solicit out-of-band information from any one particular PEA using a simple request/reply protocol. This channel is used exclusively by the hub modem for a multiplicity of functions including, error rate monitoring, configuration, bandwidth assignment, and power level transmission adjustment.

The BodyLan protocol employs slow frequency hopping to avoid frequency bands which have high power jamming transmitters. It is highly probable that we will employ techniques similiar to those used by cellular telephone networks which employ slow frequency hopping. The protocol for shifting from one frequency band to another has not yet been resolved other than to suggest that fast frequency hopping (i.e. symbol by symbol, bit by bit, or even frame by frame) will not be employed.

2. Hub Interface Channels

Each PEA can have a total of four sub-channels in any combination of hub->PEA or PEA->hub. With a maximum of 64 PEAs, each BodyLan accomodates a total of 252 sub-channels. Each channel can be a multiple of 32 b/s. Thus for example, PEA(42) could be assigned two hub->PEA

sub-cahnnels of 1024 b/s and one PEA->hub sub-channel of 512 b/s with the last sub-channel unused.

Because BodyLan utilizes a totally synchronous TDMA communication protocol, the interface between Host processor and the PCMCIA card HI is simplified. The interface is based on a ping/pong dual port buffer, called the Data Buffer, with an interrupt to the host processor at the frame rate.

In response to the frame interrupt, the host processor is required to store into the Data Buffer the data that will be transmitted by the hub modem to the PEAs in the next frame interrupt period and read from the Data Buffer the data that was received by the hub modem in the last frame interrupt period. After each frame interval interrupt, the meaning of the ping/pong buffers is swapped.

Data is organized in the Data Buffer for both Rx and Tx directions as lists of bytes. The longest list is 84 bytes and occurs for a sub-channel consuming 100% of the maximum available bandwidth (i.e. 28,672 b/s). For lower bandwidth sub-channels, the list associated with each sub-channel is shorter and usually will not consists of an integral number of bytes.

Data is sent serially and assembled little-endian. Thus a sub-channel of the minimum data rate results in a one byte list with only bit 0 of the byte used. For a sub-channel of 544 b/s (i.e. 17 bits per frame), its list consists of three bytes, the first two bytes are totally filled, and the third byte has only bit 0 filled. The maximum size of one side of the Data Buffer thus occurs when 251 sub-channels have minimum bandwidth and the 252th sub-channel uses all the remaining bandwidth. The largest size needed for either the ping or pong sides of the Data Buffer is thus 304 bytes.

2.1 Hub Interface Channel Configuration

There are several tables used to configure the sub-channels in the Hub Interface. The first table, called the Sub-Channel List Pointer SLP table, contains 256 9-bit addresses which point to the particular sub-channel list within the data buffer.

For example, SLP(INDX)=245 indicates that the list associated the particular sub-channel starts at byte location 245 in both the ping and pong Data Buffers. INDX is computed by taking the channel number times four added to sub-channel number for the particular.

The second table consists of 1024 entry memories called TxPlan which assigns each bit within the frame to a sub-channel for the hub->PEA path. A corresponding table, called RxPlan, assigns each bit wihin the frame to a sub-channel for the PEA->hub direction. Note that unlike the PEA which can never send and receive simultaneously, the hub is required to both send and receive simultaneously. The third table, called the Sub-Channel List Pointer SLP table, contains 256 9-bit addresses which point to the particular sub-channel list within the data buffer.

To reduce the number of TxPlan and RxPlan accesses per frame (each access consumes power) the XxPlan entries are encoded as follows:

XxPlan entry															comments
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
c4	c3	c2	c1	c0	s7	s6	s5	s4	s3	s2	s1	s0	b2	b1	b0	c<4..0>!=0

```
  0  0  0  0  0  0 b9 b8 b7 b6 b5 b4 b3 b2 b1 b0
  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  skip to next frame
```

Where c<4..0>!=0 is the number of bits user data associated with sub-channel s<7..0> to transmit or receive and b<10..0> is the number of bits to skip at the end of sending or receiving user data. When c<4..0>=0, no user data is to be transmitted or received and the low 10-bits indicating the number of bits to skip. An all zeros entry skips to the beginning of the next frame. Sub-channels 0-251 reference a particular user sub-channel while 252-255 are reserved for the hub modem functions as follows:

s<7..0>	Modem Function
252	Synchronization beacon start
253	tuning and bookkeeping intervals
254	broadcast command/control channel
255	polling command/control channel

Since eight 8-bit duration beacon patterns are transmitted during each frame at bit positions which are quasi-unique to each BodyLan, there will be at least 8 entries in the TxPlan buffer corresponding to each transmitted beacon. As an example plan, assume that the beacons are transmitted at bit locations (relative to the frame start) {0, 100, 200, 300, 400, 500, 600, 700}. Further assume that 2038 b/s are to be transmitted to PEA 4 sub-channel 2 at 8 evenly spaced intervals across the frame (i.e. eight 8-bit groups). Assume that the Data Buffer list associated with sub-channel 18 (i.e. 4 X 4 + 2) starts at byte Db[102].

TxPlan Entry	Comment
8,252,0	Tx 8-bit Beacon starting in bit location 0
8,18,0	Tx Db[102] starting in bit location 8
0,84	skip 84 bits
8,252,0	Tx 8-bit Beacon starting in bit location 100
0,8	skip 8 bits
8,18,0	Tx Db[103] starting in bit location 128
0,64	skip 64 bits
8,252,0	Tx 8-bit Beacon starting in bit location 200
0,48	skip 48 bits
8,18,0	Tx Db[104] starting in bit location 256
0,36	skip 64 bits
8,252,0	Tx 8-bit Beacon starting in bit location 300
. . .	and so on

Both the TxPlan and the RxPlan are double buffered to allow the host processor to be constructing one TDMA plan while utilizing the other. When the TDMA plans for the hub modems and all PEAs which must have their TDMA plans changed is completed, a command is broadcast on the command & control channel to cause all TDMA engines to switch to the alternate XxPlan.

3.0 Control Registers

The Host Interface also implements control registers to provide configure the hub modem and for monitoring and control. These registers can classified into two groups. The first group sources information needed to configure the BodyLan. These register are in effect write-only and would normally be implemented using EEPROM to insure their content over power cycling. The second group includes all other control registers.

3.1 Beacon Identification Code Registers

Eight beacon sequences are transmitted by the hub during each frame at bit locations specified in the TxPlan table. Every frame starts with a beacon.

The positions of the other five beacons form a Optically Orthogonal Code word of the form {0, p1, p2, p3, p4, p5, p6, p7} where pj represents the bit position in the 1024-bit frame. These beacon position code words are designed to have low crosscorrelation with code words of other BodyLans.

Each beacon consists of 48 symbols during which energy is transmitted spread over 512 possible positions. The last two symbols are adjacent to one another but the remaining 46 chips are spread over the 512 positions in such a way to minimize their crosscorrelation with used data symbol words. The positions of 48 symbols within the 512 chip sequence is identical for all BodyLans.

The positions of the beacons within the 1024-bit frame are quasi-unique for each BodyLan. It is estimated that there are more than 1E16 different combinations of beacon positions within a frame. Thus the likelyhood of two users coming into proximity of one another and interfering is negligible. To gain further diversity and to allow simply detection of beacons transmitted by the home BodyLan hub modem, the symbols within a beacon are FSK modulated using a pattern which is quasi-unique to each BodyLan. With more than 7E13 different beacon symbol sequences to choose from, it is easy to distinguish beacons transmitted by the home hub with a simple matched filter.

The six byte wide Beacon Identification Code registers, Bic[5..0]<7..0> are loaded by the host to specify the symbol sequence. Bit positions are little-endian first meaning that Bic[0]0 is transmitted in the first beacon symbol position and Bic[1]1 is transmitted in the second symbol position and so on. To allow fine grained synchronization between the PEA modems and the hub modem, it is required that the last two beacon symbols be compliments of one another. Thus Bic[5]=10xxxxxx.

3.2 Pseudo-Random Number Generator Seed Registers

User data is transmitted using Optical Orthogonal Codes which have low correlation cross correlation even when rotated an arbitrary number of chip positions within a codeword. To gain diversity, the BodyLan protocol calls for selecting one of the codewords randomly and also selecting a codeword rotation randomly for each bit position. This means that the coding diversity is related to the product of number of codewords times the number of possible cyclic shifts times two. The larger the diversity the lower the error probability.

To achieve this pseudo-random codeword and cyclic shift selection, both the hub and PEA modems employ a 23-bit pseudo-random number generator whose low-order bits select the codeword and the cyclic shift for each new bit position. The pseudo-random number generator is seeded at the start of each new frame interval with the content of the 23-bit Pseudo-Random Number Generator Seed (PrngS) register.

The three byte wide Pseudo-Random Number Generator Seed registers, PrngS[2..0]<7..0> are loaded by the host to specify the seed. The Pseudo-Random Number Generator employs the tri-nomial x^23+x^5+1 as a generator polynomial with PrngS[0]0 loaded into bit 0 of the shift register, PrngS[0]1 loaded into bit 1 of the shift register and so on. Bits in the shift register are shifted up with the low order bit position loaded with Prn23 EXNOR Prn5 at the beginning of each new bit postion with a frame.

3.3 Status Register

It is expected that the host will interogate the 16-bit control register during each frame interrupt service routine. This register contains both read-only and read-write bits which allow the host fine grained control of the hub modem. The current bit assignments are as follows.

Bit	status register usage
7	frame interrupt enable
6	modem controller interrupt enable
5	modem controller command completion
1	receive enable
0	transmit enable

3.4 Modem Controller Mailbox

An 8-bit microcontroller (tentatively a Phillips 80CL410) is embedded on the PCMCIA card to offload complex activites from the host processor. To reduce power consumption, this microcontroller is powered off except during those periods when it must execute a strip of instructions. There is no notion of an idle process consuming power without executing any meaningful activity. Rather the clock input to the microcontroller is normally disabled. It is enabled when hub modem housekeeping funcions are required or when the host processor loads the Modem Controller Mailbox register. After completing the code strip associated with the service request, the microcontroller disables its clock and enters into the low-power mode.

A packet of information is passed from the host processor to the microcontroller in part from the Modem Controller Mailbox register and in part because the microcontroller can access the Data Buffer. Thus, the host can pass a 128-bit control packet to the hub microcontroller by first loading the 112-bit body into the Data Buffer and then loading the 16-bit packet header into the Modem Controller register. Similiarly, the microcontroller can pass a packet of information to the host processor by storing the packet of information in the Data Buffer.

When the hub modem microcontroller completes the code strip associated with activation event, it can set bit 5 of the Status register. If enabled, an interrupt will be posted to the host operating system.

4.0 Command & Control Channels

The Command & Control Channel provides for bidirectional packet type communication between the hub modem and all the PEA modems. The protocol is based on a simple master/slave polling. Functions provided are:

1) The hub modem broadcasts a packet of information to all PEAs.
2) The hub modem transmits a packet of information to one specific PEA.
3) The hub modem transmits a packet request to a specific PEA which is then expected to return information via the PEA->hub command and control channel.

The command and control channels provides a maximum of 2048 b/s link between the hub modem and all PEAs and a 2048 b/s link between one or more PEAs and the hub modem. Since this aggregate rate is in many cases comperable to or even much greater than the total data rate of the PEA device, more complex signaling protocols are utilized to reduce the amount of time that the PEA must receive data on the command and control channel.

For example, we would expect a PEA modem connected to a keyboard to produce a data rate of no greater than 96 b/s, thus requiring only three bits every frame period. A keyboard microcontroller would be expected to consume in the order of 10-20 microwatts running the keyboard with the PEA modem consuming another 5 microwatts. If the PEA modem were required to receive the entire command and control channel bandwidth, its power consumption would increase by a factor of twenty. Thus special protocols are required to communicate with very low-power PEAs.

We expect all command and control communications to be initiated by the hub microcontroller. Most of this communications will be periodic monitoring of status, received power levels, error rates. Other command and control traffic will include discovery and PEA configuration functions.

The architectural modem that can be used is that the hub modem microcontroller is the host to each PEA modem. Since each PEA modem has an integral microcontroller, fairly complex hub<->PEA protocols can be established to minimize power consumption and ensure robustness.

5.0 Discovery

PEAs can be in one of three mode of operation, unconfigured, standby, and active. In the active mode, the PEA modem is synchronized with hub modem via receipt of the beacons and can both participate in the command and control channel protocol and can transmit and/or receive used channel information as controlled by a particularized for the particular PEA. In its standby mode, it is fully configured by not synchronized with the hub modem. This state could occur for example during PDA battery charging or when the PEA is physically moved away from the radio-sphere of beacons transmitted by its home hub modem. In the unconfigured state, the PEA cannot participate in any of the home BodyLan protocols because it does not have a TDMA plan nor does it "know" the other configuration constants (i.e. the Bic and PrsgS parameters) which identify the home PEA.

The protocols which are used to configure the PEAs are described in a companion document on PEA Reconfiguration.

Dana

BBN SYSTEMS AND TECHNOLOGIES

November 14, 1994

Advanced Research Projects Agency, CSTO
3701 N. Fairfax, Drive
Arlington, VA 22203-1714

Attention: Dr. Ken Gabriel
(703) 696-2252

Subject: Quarterly R & D Status Report
Contract No. DABT63-94-C-0017
BBN Reference No. 11592 – BodyLAN –

Dear Dr. Gabriel:

Enclosed is Quarterly R & D Status Report #1 covering the period April 1 through June 30, 1994 on the subject contract. To ensure consistency in out reporting, we are resubmitting this report.

If you have any questions, or require any additional information, please do not hesitate to contact the undersigned at (617) 873-4579.

Sincerely,

Dr. Julio Escobar
Senior Scientist

cc: ARPA/ESTO/CSTO/SSTO/ASTO
B. Bolling
T. Blackadar
M. DiBlasio

JE/ro

A Division of Bolt Beranek and Newman Inc.
10 Moulton Street Cambridge, Massachusetts 02138 Telephone: 617-873-3000

BodyLAN: A Wireless, Body Local Area Network

Contract Number: DABT63-94-C-0017

Quarterly Status Report #1

April 1994 through June 1994

Contractor:

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Principal Investigators:

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Submitted to:

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3701 N. Fairfax Drive
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Attn: Dr. K. Gabriel

Table of Contents

1. PROJECT PROGRESS

1.1 OVERVIEW

Status

During the first three months we concentrated on transmitter design, receiver design, transmitter-receiver synchronization, detector analysis, bit error analysis, prototype and vendor survey.

We looked at transmitter and receiver circuitry. We concentrated on modulation and demodulation circuit design. We assessed performance, ease of implementation, and did computer simulations. Transmitter design is almost complete. We also begun design of transmitter-receiver synchronization signals and protocol. In the coming months we will concentrate on synchronization signals and completing receiver circuit design.

We created models of receiver detection and bit error probabilities to analyze design alternatives. The models include characterization of demodulation and detector output waveforms (including interference conditions), characterization of alternative spread spectrum signal schemes, and channel capacity analysis. In the coming months we will concentrate on jamming considerations, synchronization protocol, and spread spectrum signal design.

We interviewed a representative of PCMCIA product vendors (PCMCIA is a PC and laptop I/O bus interface card called for in our prototype) and surveyed some of the literature available. We found potential candidates for PDA vendors and for subcontracting PCMCIA work.

Plans for Next Quarter

In the coming months we plan to create a prototype-equipment part list and vendor list, together with a procurement schedule.

1.2 HARDWARE PROGRESS

We have examined architectural and implementation issues including:

1) Choice of Pea processor
2) Transmitter circuit and spice sensitivity study
3) Transmitter Frequency modulating circuit and spice simulation
4) Transmitter frequency locking model
5) Design and simulation of negative voltage charge pump for frequency adjustment with hyperabrupt tuning diodes
5) Receiver local oscillator design and simulation
6) Receiver mixer Design and simulation of receiver
7) Receiver limiter design and simulation
8) Receiver filter study
9) I & Q channel modeling with Mathematica
10) Review of about 40 papers relevant to receiver implementations
11) Study of standard products which may be used to implement the implementation chosen

The game plan in this early phase is to visit each section of the modem, create a preliminary design, spice simulate that design to allow estimation of power consumption, noise, and parameter sensitivity using a BiCmos process as if we were going to create a chip. This allows us to make a determination of where the power dissipation goes and what are the major problems to solve.

At this time, we have examined enough of the receiver to judge that the hard part is going to be to control the delay variation between different receivers to allow synchronization to within a few hundreds of nanoseconds. This suggests we should study the use of larger prefix and postfix chip margins.

On the positive side, the literature study has paid off handsomely by giving starting circuit topologies for virtually every part of the receiver design. The I & Q channel processing technique with direct demodulation (borrowed from a paper on pager design) appears to give the lowest power consumption.

We also begun designing signals and protocol for transmitter-receiver synchronization. We expect to use signals similar to Optical Orthogonal Codes to minimize their interference with data signals in other BodyLANs, since synchronization and data signals will share the same band. We are exploring a "chime" signal which consists of an FM frequency transition as a means of providing pulse boundary synchronization to transceivers involved.

1.3 ANALYSIS

We have probabilistic models of OOC codes and a study of alternative signaling schemes, in particular a "symmetric" scheme where bit 1 and bit 0 both use "pulse codewords" and an "asymmetric scheme" where bit 0 uses a "no pulse codeword." If the demodulator/detector circuit can distinguish noise from pulses, the asymmetric wins out by a good margin.

We are coming to understand the FM quadrature demodulator with limiters. Detecting the FM tones is equivalent to determining the rotation of a vector whose components are the in phase and quadrature demodulator arms. This can be done in one quarter of an FM signal period. When interference is present, the vector length changes with time and its trajectory is more like an ellipse. The direction of rotation seems to be given by the strongest signal (capture effect). Detecting the sense of rotation now require up to 1/2 period. When only noise is present, it seems like the output is like a degenerate elliptical "footprint," very narrow and inclined at 45 degree angle due to the strong correlation between modulator output arms. This may give a simple way to distinguish noise from FM tones.

When asynchronism of interferers is taken into account, detection of the sense of rotation over several FM periods appears to improve bit error performance. We have models for performance in the face of asynchronous interference both for asymmetric schemes with detectors able to distinguish noise from pulses, and for symmetric schemes. We are in the process of evaluating performance.

1.4 PROTOTYPE DEVELOPMENT

4/14/94
Arranged for a visit from Greg Brasso from Palmtree Products to talk about getting PCMCIA slots for our desktops, about getting technical help in the design of PCMCIA cards, and about manufacturing these cards.

Brought in Palmtree for PCMCIA help on 4/29/94

Read background literature

4/29/94
Contacted Centennial re their helping us with PCMCIA mfg. They are expecting us to call to arrange a visit.

5/13/94
Contacted Globe Mfg Sales, INC. because they make a "One piece PCMCIA kit" WCB 800 227 3258 or 908 232 7301. Spoke with George Noll. He will send us a sample and a print. Should have by 5/18.

Called Jack Bayer, Databook, 716 292 5722
He will send us some info about an upcoming IC Card Expo in Santa Clara July 25-27, some info about PCMCIA organization, and maybe some other pointers. He sounds happy to help us. Suggests that we certainly want to use his card-eval board for big PC.

Requested literature from S-MOS Systems 800-228-3964 on the S-MOS CARDIO-386 ("a full-function 386AT" apparently the size of a PCMCIA card)

Talked with IBM about getting preliminary information on their POWERPC PDA and about their PCMCIA design and manufacturing Process.

1.5 MILESTONES FOR NEXT QUARTER

Next Quarter's hardware activities will focus on completing the design and simulation of the receiver, work on the ancillary logic to create the chip patterns, and the master timing oscillator design.

For the next Quarter period we will integrate the performance models, compare performance among the different signal design alternatives in the presence of asynchronous interference and jamming, look into synchronization beacon protocols, and look into OOC (code) design.

2. SPECIAL PROGRAMS DEVELOPED OR MAJOR EQUIPMENT PURCHASED

--- NONE ---

3. CHANGES IN KEY PERSONNEL

--- NONE ---

4. MEETING AND VISIT HIGHLIGHTS

4/14/94
Arranged for a visit from Greg Brasso from Palmtree Products to talk about getting PCMCIA slots for our desktops, about getting technical help in the design of PCMCIA cards, and about manufacturing these cards.

Talked with IBM about getting preliminary information on their POWERPC PDA and about their PCMCIA design and manufacturing Process. We will be following up on both topics in June.

5. PROBLEMS OR CONCERNS WHERE ASSISTANCE OR GUIDANCE REQUIRED

PEA device suggestions. Suggestions for collaborators (hardware, RF, BodyLAN applications).

Please verify planned budget profile. [This was accomplished by K. Gabriel during our June visit to ARPA.]

6. FISCAL STATUS

See Attached

7. ACCOMPLISHMENTS

We have starting circuit topologies for virtually every part of the receiver design. The FM quadrature demodulator channel processing technique with direct demodulation (borrowed from a paper on pager design) appears to give the lowest power consumption. We have candidate signals for transmitter-receiver synchronization.

We have probabilistic models of OOC codes and a study of alternative spread spectrum signaling. We have suggestions for substantial improvement in bit error rate performance, which depend on the capabilities we can build into the demodulator/detector circuit.

We made contact with Centennial Technologies Inc., who appears willing to collaborate in the production of a PCMCIA card BodyLAN prototype.

Contract No. DABT63-94-C-0017
BodyLAN: A Wireless, Body Local Area Network
BBN Reference No.11592

Fiscal Status: April 1, 1994 - June 30, 1994: Report #1

Cost Funds currently authorized	$483,684
Total Estimated Cost	$685,081
Expenditures & commitments as of June 30, 1994	$44,905
Estimated cost funds for Completion	$640,176
Estimated Date of Completion	10/31/95

May 2, 1995

Advanced Research Projects Agency, ESTO
3701 N. Fairfax, Drive
Arlington, VA 22203-1714

Attention: Dr. Kaigham Gabriel
(703) 696-2252

Subject: Quarterly R & D Status Report
Contract No. DABT63-94-C-0017
BBN Reference No. 11592 – BodyLan –

Dear Dr. Gabriel:

Enclosed is Quarterly R & D Status Report #4 covering the period January 1995 through March 1995 on the subject contract.

If you have any questions, or require any additional information, please do not hesitate to contact the undersigned at (617) 873-4579.

Sincerely,

Dr. Julio Escobar
Senior Scientist

cc: ARPA/ESTO/CSTO/SSTO/ASTO
B. Bolling
T. Blackadar
M. DiBlasio

JE/ro

BodyLAN: A Wireless, Body Local Area Network

Contract Number: DABT63-94-C-0017

Quarterly Status Report #4

January 1995 through March 1995

Contractor:

BBN Systems and Technologies
A Division of Bolt Beranek and Newman Inc.
10 Moulton Street
Cambridge, MA 02138

Principal Investigators:

Mr. Phil Carvey
Telephone (617) 873-3208
pcarvey @ bbn.com

Dr. Julio Escobar
Telephone (617) 873-4579
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Submitted to:

Advanced Research Projects Agency
3701 N. Fairfax Drive
Arlington, VA 02203
Attn: Dr. K. Gabriel

Table of Contents

1. Project Progress

1.1 Overview

1.1.1 Progress Summary

- We have finished the design of the RF integrated transceiver, and submitted it for fabrication in late March. The circuit provides only a half-duplex radio link and will be used in both the Hub and the PEA (Personal Electronic Accessory). In doing so, we have greatly reduce the development cost of Hub and PEA hardware.

- We have designed, fabricated and tested the second RF transmitter prototype, which included both the modulator and the frequency controlling circuits. The antenna circuit and the voltage controlled oscillator were functioning properly. The modulator and the varactor charge pump did not perform due to incorrect implementation and biasing. However we believe we have understood the problem well enough to proceed directly into building the integrated transceiver based on the lessons learned.

- We have completed the architectural design of the Hub PCMCIA card, and produced a draft of its hardware specification. A high-performance common processor MC68356 (or MC68PC302 if available) will be used as the embedded controller. This will allow us to develop our resident software in C or C++ and greatly simplify the Hub development.

- We have produced design notes specifying the link protocol and the Hub device driver. The documents were also revised to accommodate hardware modifications. The final specifications will be written in parallel with software development as the documentation of actual implementation.

- We have received the first PCMIA interface prototype from Centennial Technology Inc. The prototype will be used to enable software development in parallel with the hardware work.

- We have taken actions to simplify both hardware and software design of the prototypes and to eliminate the non-essential steps in the development process. These actions were taken in order to preserve the proposed budget without affecting the system functions.

1.1.2 Plan for Next Quarter

We will focus on the goal of constructing a pair of working Hub and PEA prototypes for the first point-to-point communication test. The effort will include the programming of the micro code for PCMCIA card and the device driver residing in the PDA (Personal Digital Assistant, i.e. the host).

1.2 Hardware Design

The main accomplishments were made in the development of receiver prototype and Hub digital logic.

1.2.1 Second Transmitter Prototype

We designed and fabricated the *second* transmitter prototype in January, and tested it in February 1995. Its implementation proved more challenging and time consuming than we anticipated.

In addition to the antenna driver existing in the first prototype, the second prototype contained the varactor-controlled phase locked loop and the frequency modulator of the transmitter as well as the oscillator circuit of the receiver. It also included a digital code generator for producing test patterns for the modulator.

Our tests showed that both the antenna circuit and the voltage controlled oscillator have been functioning properly. The frequency modulator and the varactor charge pump suffered from implementation problems. As a result, the transmitter did not perform according to specifications in terms of clock output levels and frequency stability. The problem also affected the receiver oscillator.

In spite of this we identified the problems, which were caused mainly by incorrect biasing and device implementation, and we have decided to proceed directly onto the development of integrated transceiver based on the lessons learned.

1.2.2 Third Transmitter and First Receiver Prototype

We finished the design of the RF circuit of the transceiver for both the Hub and the PEA and submitted it for fabrication at the end of March. The fabricated module will return by mid-April. The module contained RF circuits of the entire radio transceiver, which includes the voltage controlled oscillator and the frequency modulator of the transmitter as well as the phase locked loop, the demodulator, the IF amplifier and the frequency discriminator of the receiver.

By using a common frequency half-duplex channel for the two-way communication, we were able to combine parts of transmitter and receiver circuitry and simplify the design. The half-duplex design also allows us to use the module in both the Hub and the PEAs and thus reduce the development time.

After this RF module prototype, we plan to move directly onto the final implementation of the radio transceiver.

1.2.3 Hub Digital Circuit

We started the hardware design of the Hub PCMCIA card in mid-March. Since then, we have completed the architectural design of the card (including processor choice, memory map and interrupt structure) and produced a draft of the hardware specification.

We chose to use Motorola MC68356 (or MC68PC302 if available) as the embedded Hub microprocessor, and populate the card with a 512KB flash memory and a 512KB static RAM in addition to the digital interface to the radio transceiver. All the digital parts are connected by a 8-bit MC68K bus. The card will interact with the host PDA through a standard PCMCIA interface and an interrupt signal. Both MC68356 and MC68PC302 are low-power microprocessors specialized in communication applications; they are equipped with a MC68K core, a four-channel communication processor with DMA and a build-in PCMCIA interface. The availability of a multi-protocol communication processor and the PCMCIA interface has simplified our hardware design while the existence of the MC68K core greatly reduces our software development efforts.

1.2.4 Development Strategy

As a development strategy, we have been simplifying the hardware development in order to preserve the budget and meet our deliverables. This came as a result of reassessing the development effort required to implement all the originally intended functionalities. While we have produced design notes explaining the set of desirable functions, we will only implement those necessary to demonstrate the project goals. The actions taken are:

1. We simplified both the Hub and the PEA hardware by implementing only half-duplex communication. By using a single carrier frequency and removing the full-duplex capability from the Hub, we can combine several parts of transmitter and receiver circuitry, and use the same circuitry in both the Hub and the PEAs. This simplification will enable savings in both the design and fabrication processes.

2. We will reduce the number of prototypes fabricated within the development cycles. We will make one complete RF prototype – the one just submitted – and possibly one prototype of Hub digital logic before the final implementation.

1.3 Software Design

1.3.1 Link Protocol Specification

We produced the design notes on link protocols and device drivers at the end of February. Since then, we have revised the design notes in order to accommodate the hardware modifications.

We specified, in the design notes, a light-weight link protocol which supports a *memory-mapped* device abstraction of the attached PEAs and a *wireless bus* model of the radio link between the Hub and the PEAs. As the bus master, the Hub can initiate movement of data blocks of specific length or continuous data stream by using either the *block* or the *stream* transfer modes. The transfers are *not* error free, and the transactions are *not* acknowledged. An acknowledged version of the protocol has been designed and could be used as an extension of the existing protocol.

We are holding back the protocol implementation pending for the outcome of the receiver and hub hardware layout. This will make for more efficient software implementation at the expense of some development delay.

1.3.2 Hub Software Development

Along with the choice of a high-performance embedded processor, we decided to write the Hub controller code in a high level language (either C or C++) in order to reduce the programming effort. We also decided to develop a library of simple PEA communication and control functions instead of writing a full-scale device driver for the Hub applications.

1.3.3 Development Strategy

As in hardware development, we tried to simplify the software development task and have taken the following actions:

1. We have simplified the task of Hub programming by using the MC68356 processor and the programming language C or C++. The programming of the PEAs, which is simpler than the programming of the Hub, however will still be done in assembly language.

2. We will develop a library of PEA communication and control functions, instead of a full-scale device driver.

3. We have withheld the writing of formal software specifications and converted it into the documentation of actual implementation.

1.4 Analysis

We modified the spread spectrum signal to one that consists of three *four-symbol bursts* with inter-burst intervals obeying the (64,3,1) optical orthogonal coding scheme. This new signal design will enhance the radio transceiver efficiency by reducing the circuit on/off overhead and by simplifying the implementation of the spread spectrum signal. While this is expected to raise the bit error rate above the estimated value of 10^{-3} due to the increased probability of successive symbol corruptions, the amount of redundancy will restore the target bit error rate at the expense of bandwidth.

Once we are confident with this implementation, we plan to make tests on the OOC approach. In order to limit project spending, we decided *not* to conduct any simulation on the new signal scheme; instead, we will observe the transceiver performance during prototype testing, and take corrective adjustments if necessary.

1.5 Prototype Development

We received the first PCMCIA card prototype from Centennial Technologies Inc. at the end of March. The prototype contains a standard PCMCIA interface with resident static RAM and an interrupt signal. Its availability enables us to proceed in developing device drivers in parallel with hardware design.

1.6 Plan for Next Quarter

We will focus on the goal of constructing a pair of working Hub and PEA prototypes for the first point-to-point communication test. The breakdown of tasks includes the following:

- Fabrication and testing of the RF transceiver module (used in both the Hub and the PEA),
- Implementation and testing of the Hub PCMCIA digital logic,
- Implementation and testing of the PEA modem controller logic,
- Development and debugging of basic link protocol in the Hub and the PEA for command and data block transfers,
- Development and debugging of the Hub library for PEA communication and control,
- Writing of simple test application program for the Hub.

2. Program Development and Equipment Purchase

— NONE —

3. Personnel Changes

There has been *no change* in the key personnel of the project.

Junior software engineer, Trevor Mendez, and hardware engineer, Nuriel Lapidot, left the project after fulfilling their duties. Trevor has written a draft of the device driver specification and Nuriel has completed the layout and testing of the second transmitter prototype.

Senior hardware engineer, Ronald Pettyjohn, joined the project in February. He is responsible for the design, layout and testing of the Hub PCMCIA logic circuits.

4. Meetings and Visits

— NONE —

5. Problems and Concerns

The layout and implementation of the transmitter as well as the specification of wireless channel protocols both consumed more time and effort than anticipated. In contrast, the subsequent layout for the receiver circuit was achieved in approximately half the time of the transmitter. Similarly, the hub layout has proceeded at rapid pace and is essentially ready for fabrication.

Moreover, we have delayed the protocol implementation until the hub hardware has been tested, so that software development need not make any development assumptions about the hardware. While this causes a one to two month delay in this hardware task, it will make development more efficient. By applying parallel software development to the Hub micro-code and the application program, we expect to remain within the project schedule.

The actions taken to preserve the budget of Hub micro-code and application program are mentioned in Sections 1.2.4 and 1.3.3. A summary of these actions is listed below:

- Both the Hub and the PEA implement only a half-duplex radio link using the same carrier frequency 375MHz for both inbound and outbound communication.
- The BodyLAN network employs an unacknowledged link-layer protocol to support both stream and block data transfers. This is consistent with expected applications.
- The resident software on the Hub PCMCIA card will be written in C or C++ and running on a MC68356 or a MC68PC302 high-performance communication processor.
- A library of PEA communication and control functions will be developed to replace a full-scale device driver in supporting the application programs in both testing and final demonstration.
- Fewer transceiver prototypes will be made, combining all the lessons learned from previous prototypes.
- The final protocol specification will be produced together with the documentation of the actual software implementation.

We believe that the above changes will substantially reduce budget risks while preserving the goals of the project.

6. Fiscal Status

— SEE ATTACHMENT —

7. Accomplishments

In the past quarter, we have reached the following milestones:

- design, fabrication and testing of second RF transmitter prototype,
- design and fabrication of first integrated RF transceiver,
- preliminary and revised specifications of link protocol and Hub device driver,
- architectural design of Hub PCMCIA card.

Contract No. DABT63-94-C-0017
BodyLAN: A Wireless, Body Local Area Network
BBN Reference No.11592

Fiscal Status: January 1, 1995 - March 31,1995: Report #4

Cost Funds currently authorized	$685,081
Total Estimated Cost	$685,081
Expenditures & commitments as of March 31, 1995	$483,742
Estimated cost funds for Completion	$201,339
Estimated Date of Completion	10/31/95

August 10, 1995

Advanced Research Projects Agency, ESTO
3701 N. Fairfax, Drive
Arlington, VA 22203-1714

Attention: Dr. Kaigham Gabriel
(703) 696-2252

Subject: Quarterly R & D Status Report
Contract No. DABT63-94-C-0017
BBN Reference No. 11592 – BodyLan –

Dear Dr. Gabriel:

Enclosed is Quarterly R & D Status Report #5 covering the period April 1995 through June 1995 on the subject contract.

If you have any questions, or require any additional information, please do not hesitate to contact the undersigned at (617) 873-3786.

Sincerely,

Thomas Blackadar
Department Manager

cc: ARPA/PM/ESTO/CSTO/SSTO/ASTO
B. Bolling
M. DiBlasio
Julio Escobar

TB/md

BodyLAN: A Wireless, Body Local Area Network

Contract Number: DABT63-94-C-0017

Quarterly Status Report #5

April 1995 through June 1995

Contractor:

BBN Systems and Technologies
A Division of Bolt Beranek and Newman Inc.
10 Moulton Street
Cambridge, MA 02138

Principal Investigators:

Mr. Phil Carvey
Telephone (617) 873-3208
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Telephone (617) 873-4579
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Submitted to:

Advanced Research Projects Agency
3701 N. Fairfax Drive
Arlington, VA 02203
Attn: Dr. K. Gabriel

1. Project Progress

1.1 Overview

1.1.1 Progress Summary

The following list summarizes the main tasks accomplished in the areas of *hardware development, software design* and *signaling scheme* between the months of April and June 1995.

Hardware

- Design of PEA digital controller modules
- Circuit simulation of Hub and PEA digital controller modules

Software

- Specification of block and stream data transfer mechanisms

Signaling Scheme

- Specification of TDMA signaling micro-codes

1.1.2 Future Milestones

We had delayed software development milestones until the hardware design changes explained in the previous report were achieved. the milestones below reflect these changes.

- Hub/PEA link test
- PDA software test
- BodyLAN Prototype

---------- End of September ----------

- Performance benchmarking
- BodyLAN demonstration
- Final report

---------- End of December ----------

1.2 Hardware Design

The main accomplishments were made in the development of receiver prototype and Hub digital logic.

1.2.1 Second Transmitter Prototype

A simulated design has been completed for both the HUB modem (implemented on a PCMCIA card) and Personal Electronic Accessory (PEA) modem. These designs include digital control chips, Transmitter/Receiver RF sections, and all ancillary circuits such as VCXO, power supplies, and frequency measurement circuits. All non-digital modem sections have been implemented in a prototype card and have been partially tested.

Due to component count and board space considerations, both the Hub and PEA modems are implemented as two board sets. Each set consists of a mother board (unique for the Hub and PEA) and a common daughter board. The Hub modem will conform to the PCMCIA Type III mechanical specification.

The Transducer Controller Module (TCM), introduced in the last Technical Report as a mechanism for separating the evaluation testing and early application demos from the PEA modem development has been abandoned. The plan called for contracting the TCM development to an outside consultant. Only one bid was submitted. It was judged too costly compared with expected project benefits. Accordingly, the plan has been changed to integrate the testing functionality into the PEA microprocessor.

A programming reference manual was also produced during the reporting period for both the Hub and PEA modems.

Since only off-the-shelf components are employed in the prototype PEA modem, and we want to have some commonality with the Hub modem, we have partitioned the PEA modem design into a mother/daughter board pair. The daughter board design, containing all receiver components, is also used in the Hub modem. The mother board contains all other non-receiver components including the digital control chips. One of the primary design goals were to make the transition to final product straightforward. In our model, the final PEA modem design would include a single CMOS chip integrating all digital, analog and RF sections together with a handful of discrete components (e.g., crystal, inductors, bypass capacitors).

While in principle the processor of the PDA might control the Hub directly, it was decided to use an on-board processor because the interrupt latency of the PDA is unknown and encapsulating the functions will allow easier porting of the Hub to various PDAs. The Motorola MC68PM302 is utilized as the Hub processor. It implements the PCMCIA interface, its inexpensive, has a very small BGA footprint, and meets the design constraints of "thin & 3v"

A 512K byte flash memory is used for:

* the PCMCIA-required Card Information Structure, used for host-system configuration using template host drivers,
* on-board processor code

A 256K byte SRAM is used for:

* general purpose on-board processor read/write memory
* buffers for message/data transceived between the Hub and PEAs
* "instructions" for the hardware controller EPLD

An Actel 1280XL FPLD interfaces the processor to the analog and RF sections and implements all lower level digital functions. Its primary task is to execute instruction contained in the TDMA plan. Most instructions are associated with a triplet of RF bursts. The instruction indicates when each of the three bursts is to occur relative to the start of a 32 millisecond frame, the direction of transfer (i.e. Hub->PEA or PEA->Hub) and an associated SRAM location.

Transfers across the RF channel are in units of nibbles or bytes. Nibbles will be redundantly encoded by replicating the nibble three times. Bytes will be encoded with a four bit error correcting code. For byte errors with single-bit errors, the data will be corrected and an error is logged. For 2-bit errors, an error is logged.

The controller is implemented in an Actel A1280XL-TQC (8000 equivalent gates) in a 176-pin TQFP package. This device was chosen because of our experience using Actel arrays in other projects but primarily because it generates CMOS output levels, works at 3.3 volts, and comes in a "thin" package.

1.2.2 PEA Conroller Chip Design

While the power consumption of the analog and RF sections is much higher than could be achieved in a single chip implementation, measured power consumption is within a factor of four of our targets. Power consumption of the digital sections is off by a factor of 2000.

Since demonstrating feasibility of the BodyLAN concept hinges on an overall power budget consistent with small size battery operation, we have contracted with an MIT graduate student to design a low power version of the controller chip. Under the supervision of Prof. Anantha Chandrakasan, the student is changing the logic and architecture of the FPGA version of the controller chip and constructing a layout utilizing the MOSIS one micron CMOS foundry design rules.

1.3 Software

1.3.1 Physical Layer Device Abstraction

The RF and digital circuits in PEA and Hub were designed to provide *six* TDMA channels through the wireless link:

- *one* command and control channel
- *one* device state reporting channel
- *two* processor data channels
- *two* device data channels

With respect to PDA system software, the BodyLAN operates as a wireless bus which can accommodate a total of 56 PEA devices. The PEA devices are mapped onto PDA memory through the PCMCIA interface.

1.3.2 Device Register Block

Two techniques were employed to manage the image of PEA registers in the Hub: (1) the use of a hashed value to summarize the device state for comparison and (2) the use of a block transfer to communicate the entire state of a PEA device.

The device register block of each PEA consists of *three* kinds of registers:

- *control* and *status registers*, which; their contents constitute the *software observable state* of the device;
- *data pointers*, which specify the address of data to be transferred via different channels, and
- a *device state-summary register,* which contains a hashed value of the current *state* of the PEA, i.e. the content of control and status registers of the device. Currently, CRC-16 is chosen to be the hashing function.

1.3.3 Information Transfer

All digital communication through BodyLAN (including command and control communications) are performed in one of *three* transfer modes:

1. the *automatic or event-triggered transfer mode,*
2. the *block transfer mode,* and
3. the *stream transfer mode.*

The *automatic transfer* is used by the HUB to issue commands to the PEAs and to acquire their state summary. The *stream* and *block transfers* provide the two basic data link services of BodyLAN imitating the *connection-oriented circuits* and the *connectionless datagrams* supported by most data networks. The *block transfer* is also used to exchange control and status information such as the device parameters, the TDMA plan and the register contents over the wireless network.

All transfers except command dispatches are performed *without* explicit acknowledgment nor link-layer re-transmission. Command dispatches, however, can be conducted *with* or *without* acknowledgment by design, but the first prototype only implements the simple protocol without acknowledgment.

1.4 Prototype Development

We have tested the RF transnmitter board and have fabricated the receiver board. We have sent the Hub digital controller to fabrication and are about to lay out the PEA digital controller board.

1.5 Plan for Next Quarter

- Hub/PEA link test
- PDA software test
- BodyLAN Prototype

---------- End of September ----------

2. Program Development and Equipment Purchase

— NONE —

3. Personnel Changes

There has been *no change* in the key personnel of the project.

4. Meetings and Visits

— NONE —

5. Fiscal Status

— SEE ATTACHMENT —

6. Accomplishments

In the past quarter, we have reached the following milestones:

Hardware

- Design of PEA digital controller modules
- Circuit simulation of PEA digital controller modules
- Revision of PEA interface specification
- Production of PEA programming specification

Software

- Specification of block and stream data transfer mechanisms
- Revision of PEA device abstraction
- Revision of PEA modem interface

Signaling Scheme

- Revision of TDMA signal format
- Specification of TDMA signaling micro-codes

Contract No. DABT63-94-C-0017
BodyLAN: A Wireless, Body Local Area Network
BBN Reference No.11592

Fiscal Status: April 1, 1995 - June 30,1995: Report #5

Cost Funds currently authorized	$685,081
Total Estimated Cost	$685,081
Expenditures & commitments as of June 30, 1995	$635,711
Estimated cost funds for Completion	$49,370
Estimated Date of Completion	10/31/95

November 15, 1995

Advanced Research Projects Agency, ESTO
3701 N. Fairfax, Drive
Arlington, VA 22203-1714

Attention: Dr. Kaigham Gabriel
(703) 696-2252

Subject: Quarterly R & D Status Report-Revised
Contract No. DABT63-94-C-0017
BBN Reference No. 11592 – BodyLan –

Dear Dr. Gabriel:

Enclosed is a revised Quarterly R & D Status Report #6 covering the period July 1995 through September 1995 on the subject contract. This replaces the report which was sent to you under cover letter dated November 6, 1995.

If you have any questions, or require any additional information, please do not hesitate to contact the undersigned at (617) 873-3786.

Sincerely,

Thomas Blackadar
Department Manager

cc: ARPA/PM/ESTO/CSTO/SSTO/ASTO
B. Bolling
M. DiBlasio
P. Carvey

TB/md

1. Project Progress

1.1 Overview

1.1.1 Technology Insertion

We have actively explored inserting the BodyLAN technology in a number of application areas including non-invasive patient monitoring, personal inertial navigation, medical monitoring, and sports training. We have spoken with seven organizations including BBN. BBN management has expressed sufficient interest in pursuing BodyLAN applications that BodyLAN was highlighted in its premier Web page.

1.1.2 Progress Summary

The following list summarizes the main tasks accomplished in the areas of hardware development, software design and signaling scheme between the months of July through September 1995.

Hardware
- transmitter section tested and fully characterized.
- 4 MHz crystal osciliator fully characterized.
- full custom CMOS chip implementing PEA controller, VCXO, and SRAM completed.
- receiver partially characterized

Software
- development tools for Microchip processor purchased and integrated into BodyLAN PC system.

Signaling
- New Ordered Optically Orthogonal Codes developed
- New Linear Orthogonal Codes developed

1.1.3 Future Milestones

The only milestone remaining is the final report. We have requested a no-cost time extension. Milestones are as follows:

- Test of the receiver
- Hub/PEA link test
- Digital/RF integration demonstration
- final report

1.2 Hardware Design

Work during this period focused on evaluation of the 3" x 4" test board fabricated during the previous reporting period and the development of the custom CMOS PEA controller chip.

The evaluation board contains the power supplies, voltage controlled crystal oscillator, transmitter, receiver, duration controller, frequency measurement circuits, and control FPGA. Understanding the discrepancies between Spice simulations and the prototype was the primary goal. Of special interest was operation during the transition region between power-off and power-on.

Significant simulation discrepancies were discovered in the evaluation board. These differences were due in part to incorrect modeling of both board parasitic devices used and coupling between the digital and RF sections of the prototype.

A simulated layout of the custom CMOS PEA controller chip has been completed. While much of the chip is a direct conversion of the FPGA developed for the PEA prototype, both the 4 MHz crystal interface, matched filter, and clock distribution schemes are new. New approaches were required because the discrete implementations used in the prototype have very large power consumptions not sufficiently reducible by a direct conversion to silicon.

1.2.1 Prototype Evaluation

The 4 MHz VCXO has been fully characterized. With a control voltage variation from 0.5 to -6 volts, oscillation frequency changes by 154 Hz (i.e. +/- 19 ppm). This is factor of two smaller than expected and is caused by parasitic capacitance one the oscillator nodes. Extinction current of the oscillator was 1.35 uamps. At its nominal 2 uamp operating current, loaded output voltage was 260 millivolts peak-to-peak. Losses in the oscillator are an order of magnitude larger than expected. The tuned output amplifier, consisting of Q1, L1, and C1 with a bias current of 15 uamps was able to drive the Actel A1240A FPGA with a 3500 millivolt peak-to-peak clock sine wave clock. Parasitic loading on the clock line was estimated at 26 pfd.

The Duration Comparison (DC) circuit has been fully characterized. It is used to determine which of two pulses is of longer duration. Frequency lock is established when the two pulses are equal. The degree to which DC is able to determine equality determines the frequency accuracy. DC uses a single current source inserting about 700 uamps into node Ns. Measured sensitivity of the new circuits is better than 2 nsec.

The prototype transmitter section has been fully characterized. The design integrates the function of oscillator, amplifier, tuning, and modulator. The new design reflects minor changes introduced during this reporting period. This includes a Tx Antenna tuning capacitor, charge pump referenced to Vdd instead of ground, a resistor inserted on the prescaler input, and change of the output transistor to a BFP405.

With a 900 uamp bias current, the measured antenna voltage is 5700 millivolts peak-to-peak. This generated a -27.5 dBm signal using a 9 inch antenna into the spectrum analyzer at one meter. This signal about 18 dB larger than expected with perfect antenna matching. While we are not unhappy with such a large radiated signal, it suggests that components in addition to the Tx Antenna are radiating. We have not isolated the source of this excess radiation.

With all digital circuits inhibited, the -28 dB bandwidth is 9 KHz band. The -28 dB bandwidth increases to 220 KHz when the digital circuits are enabled. Studies have shown that better supply decoupling reduce this digital/RF coupling. It is clearly caused by power supply modulation. We believe a balanced transmitter circuit will have less power supply sensitivity.

The transmitter is modulated by switching in varactor diodes. Modulation causes less than one dB change in radiated power. Modulation between tones is limited by the rise and fall times of the Actel 12040A controller chip to under 15 nsec.

When frequency locking is enabled in a continuous mode of operation, the frequency is not stable. Rather, it drifts over a 350 KHz band offset from 320 MHz. Both the size of the drift and size of the spread are of unknown cause. The drift is about a factor of 3.5 larger than expected. While this spread is still small compared to the 3000 Khz between tones, it was suprisingly large. We have plans to test out a balanced version of the transmitter to examine whether its reduced power supply sensitivity improves the frequency stability.

Measured Transmitter turn on time was under 120 nsec. With the continuous mode frequency instability, we have not seen cause to explore stability under burst conditions.

The prescaler used was a Motorola MC12052A. When first powered on, the chip's output corresponded to a 1700 MHz input, regardless of input, i.e. the chip was internally oscillating. After many blind alleys, the insertion of a 50-70 ohm resistor in series with the prescaler input close to the chip provided sufficient dampening to prevent oscillation.

A simple mechanism for testing the I & Q baseband circuits has been developed. It consists of injecting one tone into the I channel and another tone into the Q channel. Since the discriminator is incentive to amplitude errors, the output waveform should be a limited version of a sine wave whose frequency is the difference of the two tones. Offset voltage sensitivity, frequency cutoff points, and saturation effects can easily be studies with two signal generators.

1.2.2 PEA_C Chip Design

We have subcontracted the design of a custom CMOS chip to a master's student of Anantha Chandrakasan at MIT. This chip replaces the functionality of the VCXO, program SRAM, and FPGA PEA controller chip. We have named this design the PEA_C chip. While demonstrating microwatt power consumption of the RF sections using low duty cycle transmit and receive appears to be successful, the FPGA prototype showed power consumptions in the 20-40 milliwatt range.

The basic BodyLAN concept traded off power consumption in the RF sections with increased complexity in the digital control sections. Since the digital section must be 'on' all the time, feasibility of a micropower system is crucially dependent on whether the power consumption of the digital section can reduced by more than three orders of magnitude.

It is important to put the 20 microwatt target power consumption in perspective. With a 3 volt supply voltage and 4 MHz clock, charging and discharging a 0.55 pF capacitor will dissipate 20 microwatts. Since a typical one micron CMOS process FF has about 10-15 fF of gate capacitance, this limits one to about 35-50 FFs toggling at 4 MHz. The question is, "is it possible to design a chip to execute the desired functionality with this low a power consumption". Simulation results suggest that it is possible.

While a full discussion of the techniques used and the simulated power consumption achieved will be included in the final report, the preliminary results suggest a 20-30 microwatt power consumption with a 2 K b/s channel data rate.

1.3 Software

A protocol functional specification of the PC residing software was completed in the last reporting period. Due to funding exhaustion, no software implementation work was done in this reporting period.

An abbreviated firmware functional specification for the HUB and PEA microprocessors has been completed. Firmware for the MC68356 HUB microprocessor, because it is based on a Motorola 68000 compatible code, can be developed on BBN's ubiquitous SUN workstation platforms. Since there are no SUN platform environments for firmware development of the Microchip PIC16C64 PEA microprocessor, BBN has purchased the appropriate PC based development system on BBN's captial funds. We now have development environments for both BodyLAN microprocessors.

1.4 Spread Spectrum Signals

We have described in previous technical reports, the design and performance of a TDMA signaling scheme based on Optical Orthogonal Codes (OOC). These codes are optimal for certain conditions. However, prior to this reporting period, our use of these codes in the BodyLAN application to avoid interference between multiple interacting BodyLANs did not conform to the optimum conditions. Recently, we have discovered a means for using OOCs and other similar codes which results in optimum performance in the BodyLAN application domain. We have called this scheme Ordered Optically Orthogonal Coding (OOOC).

We have also discovered a new class of codes which gives optimum performance in the BodyLAN application. Preliminary analysis suggest these codes to perform about as well as OOOC.

Funding exhaustion has caused all project work to be concentrated on the prototype hardware evaluation. BBN has accordingly sponsored all signal spectrum work off project.

1.5 Plans for Next Quarter

- Test of the receiver
- Hub/PEA link test
- Digital/RF integration demonstration
- final report

2. Program Development and Equipment Purchase

Current plans are to focus on showing a reduced functionality prototype.

During the quarter, BBN has purchased a Microchip development system with its capitol funding (off project funding) to allow microcode development of the PEA's microprocessor code.

3. Personnel Changes

At this time the only people working on the parogram will be mr. Carvey and his supoort staff. Due to a death in his family Dr. Escobar has taken a 9 month leave of absence. Mr. carvey will continue as PI.

4. Meetings and Visits

Mr. Carvey went to the joint ESTO/CSTO summer meeting in Fort Lauderdale. A BodyLAN poster was presented during the meeting. All meeting costs were born by BBN.

5. Fiscal Status

see attachment

6. Accomplishments

In the past quarter, we have reached the following milestones:

Hardware
- Transmitter, VCXO, and Duration Comparitor fully characterized
- Custom CMOS chip implementing PEA controller, SRAM, and VCXO completed

Software
- Development environment for Microchip processor integrated with BodyLAN PC.

Signaling Scheme
- New Ordered Optically Orthogonal Codes scheme invented
- New class of codes called Linear Orthogonal Codes invented

Contract No. DABT63-94-C-0017
BodyLAN: A Wireless, Body Local Area Network
BBN Reference No.11592

Fiscal Status: July 1, 1995 - Sept. 30, 1995: Report #6

	Cost	Fee	Total
Funds currently authorized	$634,557	$50,524	$685,081
Total Estimated Cost	$634,557		
Expenditures & commitments as of Sept. 30, 1995	$607,696	$45,985	$653,681
Estimated funds for Completion	$26,861	$4,539	$31,400
Estimated Date of Completion	10/31/95		

BBN SYSTEMS AND TECHNOLOGIES

January 18, 1995

Advanced Research Projects Agency, ESTO
3701 N. Fairfax, Drive
Arlington, VA 22203-1714

Attention: Dr. Kaigham Gabriel
(703) 696-2252

Subject: Quarterly R & D Status Report
Contract No. DABT63-94-C-0017
BBN Reference No. 11592 – BodyLan –

Dear Dr. Gabriel:

Enclosed is Quarterly R & D Status Report #3 covering the period October 1994 through December 1994 on the subject contract.

If you have any questions, or require any additional information, please do not hesitate to contact the undersigned at (617) 873-4579.

Sincerely,

Dr. Julio Escobar
Senior Scientist

cc: ARPA/ESTO/CSTO/SSTO/ASTO
B. Bolling
T. Blackadar
M. DiBlasio

JE/ro

BodyLAN: A Wireless, Body Local Area Network

Contract Number: DABT63-94-C-0017

Quarterly Status Report #3

October 1994 through December 1994

Contractor:

BBN Systems and Technologies
A Division of Bolt Beranek and Newman Inc.
10 Moulton Street
Cambridge, MA 02138

Principal Investigators:

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Submitted to:

Advanced Research Projects Agency
3701 N. Fairfax Drive
Arlington, VA 02203
Attn: Dr. K. Gabriel

Table of Contents

1. PROJECT PROGRESS

1.1 OVERVIEW

Status

We identified several possible demos and we are evaluating their impact to the project goals and resources. They include an "engineering" demo designed to illustrate BodyLAN operation and application demos based on the wired-BodyLAN of the ARPA Pathfinder project at BBN (e.g., pulse-oximeter, Twiddler keyboard.) We are also evaluating the potential for collaboration with Intermedix, a cardiac-monitor manufacturer that has expressed interest in BodyLAN.

We are planning the software architecture for BodyLAN. The software will be developed in a DOS environment and the main question remaining is the singletasking vs. multitasking version of the DOS environment (Multitasking can be achieved through COTS add-on software).

We have begun the hardware development process. We prototyped the radio section of the BodyLAN modem transmitter and verified center frequency operation. This also served to calibrate our hardware circuit simulator. We plan a process of five or six hardware subsystem prototypes before we generate the first complete BodyLAN Hub and Pea (Personal Electronic Accessory) prototype. The process is designed to simplify problem identification and solving.

We generated draft specifications that include modem hardware specifications, TDMA hierarchy, modem functional specifications, Hub device driver specifications, and bootstrap algorithms. They are undergoing revisions to insure they are properly integrated. This process will conclude with the interim research report.

Our plans call for parallelizing the development effort into three main sections: RF subsystems, microprocessor subsystem, device driver.

We have obtained the collaboration of a student at MIT, Tom Barker, under the supervision of Prof. Anantha, to do part of the hardware VLSI design. This has the strategic advantage of making available to our project the state-of-the-art VLSI tools and personnel at MIT. In return we plan to fund $11,000 of BodyLAN summer work for the student.

Plans for Next Quarter

In the coming quarter we plan to achieve the following milestones:

- Transmitter prototype including frequency control section
- Receiver prototype layout
- Software specifications and start of device driver development
- Demonstration development plan

1.2 HARDWARE PROGRESS

We generated specifications for the BodyLAN modem hardware. These are found in four draft documents:

1. Hub Interface Specifications
2. Pea Interface Specifications
3. Pea Hardware Specifications
4. Transducer Controller Module Specifications

The low level Pea hardware specification is common to the Hub. The Transducer controller will serve as a stand in for a BodyLAN sensor (Pea) in the experiments and benchmarks.

The specifications detail the signal acquisition and synchronization process, the initial Pea discovery process, synchronization tracking, and hardware data transfer process.

Signal acquisition is achieved through oversampling the channel at twice the chip rate of the spread spectrum signal and using a matched filter to scan for an "attachment beacon" signal from the Hub. The attachment beacon itself is used to transfer information at low rate to configure the Pea with the BodyLAN Hub identification parameters. This allows the Pea to scan for a synchronization beacon, by reprogramming the matched filter, and begin the process of frame and chip level synchronization. A cascade counter is used to monitor the interval between synchronization beacons and a voltage controlled crystal oscillator is used to readjust the timing until chip level synchronization is complete.

The hardware includes several modes of error control redundancy for the data transfer. These can be applied at the spread spectrum signal detection level and at the data bit level. The TDMA allocation is programmable and operates on 32 millisecond frames. Transmission and reception frames are transferred from and to ping pong buffers for parsing by the digital logic.

We planned and specified a Transducer Controller Module to serve as a (Pea) sensor emulator. This module will interface with the Pea modem and serve as a source and sink of data, as well as help monitor bit error rate and hardware state through a Liquid Crystal Display. The transducer also has several serial interfaces (e.g., RS232) so that we can monitor Pea modem operation by connecting the transducer to a PC or laptop.

We prototyped the RF stage of the transmitter section of the Pea specifications. The RF oscillation frequency of the prototype matched hardware simulations. We are laying out a second transmitter prototype that will be used to test hardware control of transmitter frequency to the appropriate initial range that the receiver expects.

1.3 ANALYSIS

We created a simulator of the spread spectrum pulse detection circuitry and coupled it into the bit error rate simulator. This gives the most realistic bit error rate simulations to date because it takes into account the effect of signal power levels on the detection circuitry, and not just the spread spectrum signal design. The results confirm a bit error rate slightly above 10^-3, which is our design target.

With these simulations we have concluded for the moment the simulation benchmark of a candidate for spread spectrum signal. It is an Optical Orthogonal Code of 64 chip positions (spreading factor), three pulses, and maximum cross-correlation or off-peak autocorrelation of 1.

We explored several other promising choices of spread spectrum signals, including a set of signals whose pulses are always placed in a block (i.e., adjacent to each other). This method makes the power consumption more efficient since it comes closer to continuous operation, but does so at the expense of some performance. We will revisit the issue of signal design later in the project if necessary.

1.4 PROTOTYPE DEVELOPMENT

Prototype development has progressed in three areas: specifications of the Hub device driver, description of potential BodyLAN demonstrations, and investigation of software architecture issues.

The device driver will provide an Applications Program Interface (API) that application software will use to operate BodyLAN. The primary services offered by the device driver are stream and block data transfer functions, dynamic TDMA plan computation, and the low-level interface with the BodyLAN Hub card (designed as a PCMCIA card).

We have specified the functions and interfaces for the device driver. A PCMCIA card with BodyLAN interrupt handling capability has been ordered from Centennial Technologies Inc. and will be used to enabled device driver development in parallel with BodyLAN Hub development.

We have been evaluating several BodyLAN demonstrations. An engineering demonstration will use the Transducer Controller Module to illustrate in real time how BodyLAN Pea devices attach themselves to a BodyLAN hub and establish communications. It will also serve to benchmark bit error rate and multi-user channel performance.

We also described a demonstration based on a "pulse-oximeter," a device that measures heart rate and blood oxygen content. This device is part of the suite of devices available for demonstration in the wired-BodyLAN vest for the ARPA Pathfinder project at BBN. Similarly we have acquired device specifications for the "Twiddler" one-hand keyboard. This could serve as a demonstration for kinematic sensors as well as virtual reality keyboard, since it contains accelerometers that provide mouse control from hand motions and keys that provide keyboard input. As far as possible we would like to reuse Pathfinder systems to minimize the expense in development resources.

In software architecture, the main issue we have been evaluating is that of multitasked applications. Ideally, we envision application software modules that are independently developed and coded based on the device driver API specifications. This would require a multitasking environment capable of switching control from one application module to another as needed. On the other hand, DOS appears to be the best supported environment for Personal Digital Assistants (PDAs) and PDAs are our current choice of host environment for a BodyLAN system. Our concern is that DOS provides a singletasking environment. However, it appears that several commercial utility programs exist to emulate a multitasking environment on DOS. We will be exploring this situation early in the coming quarter.

1.5 MILESTONES FOR NEXT QUARTER

In the coming quarter we plan to achieve the following milestones:

- Transmitter prototype including frequency control section
- Receiver prototype layout
- Software specifications and start of device driver development
- Demonstration development plan

2. SPECIAL PROGRAMS DEVELOPED OR MAJOR EQUIPMENT PURCHASED

A requisition is in process to provide subcontract work, from Centennial Technologies. The work will consist of Design and Prototype Build for a BodyLAN PCMCIA interface emulator to permit developmnet of the BodyLAN hub device driver in parallel with the hub PCMCIA hardware development. Cost not to exceed $3,800.

We cancelled the Gateway P5-60 Computer System, reported on Quarterly Status Report #2 due to late delivery. We replaced this order with a Micron Computer System P90PCI. Cost with handling is $3520.

3. CHANGES IN KEY PERSONNEL

There have been no changes in Key personnel.

Larry Dennison, hardware manager of the Hardware Development and Manufacturing Department has joined the project to help plan and monitor the hardware development process.

John Zao has joined the project and is in charge of the link protocol specifications and channel performance analysis. He joined BBN last fall and is nearing completion of his Ph.D. dissertation in Computer Science at Harvard University.

Trevor Mendez, a junior software engineer at BBN's Advanced Networking Department, joined the project for the fall quarter to produce the device driver specifications for BodyLAN.

4. MEETING AND VISIT HIGHLIGHTS

-- NONE --

5. PROBLEMS OR CONCERNS WHERE ASSISTANCE OR GUIDANCE REQUIRED

-- NONE --

6. FISCAL STATUS

Fiscal Status: October 1, 1994 - December 31, 1994: Report #3

Cost Funds currently authorized	$483,684
Total Estimated Cost	$685,081
Expenditures & commitments as of Dec. 31, 1994	$263,583
Estimated cost funds for Completion	$421,498
Estimated Date of Completion	10/31/95

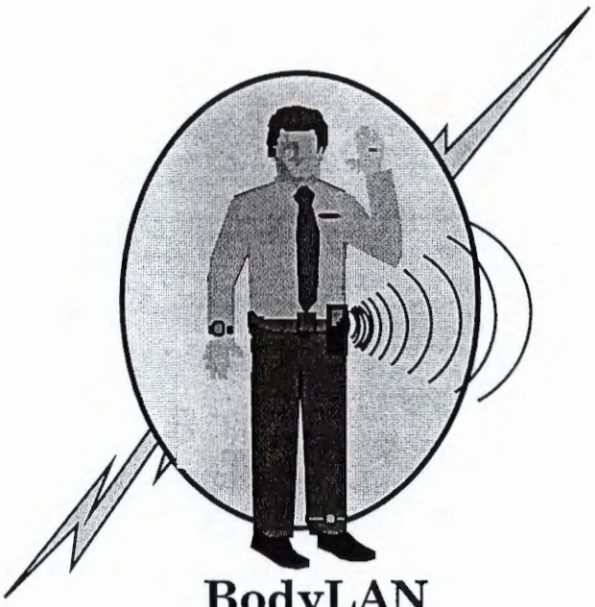
7. ACCOMPLISHMENTS

During this past quarter we achieved the following milestones

- Hardware and functional specifications for Hub and Pea
- Specifications of Transducer Controller Module
- RF transmitter prototype
- Device Driver and preliminary link protocol specifications
- Draft description of pulse oximeter demonstration
- Simulation benchmarking of bit error rate performance with detector model

BodyLAN

A Wireless, Body-Local Area Network



Principal Investigator:
Philip P. Carvey

Co-Principal Investigator:
Julio Escobar

Technical Report July 2 - January 31, 1995

Prepared For:

Advanced Research Projects Agency
Electronic Systems Technology Office
Contract No. DABT63-94-C-0017

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1. Introduction

1.1 Overview

BodyLAN is a wireless local area network whose range is the size of a human body. It connects miniature peripheral devices worn in the body like jewelry to a processing hub that can be worn on the belt or any other appropriate area. The peripheral devices, or Personal Electronic Accessories (PEAs), enhance human sensorial perception and body functions thanks to miniature electronics, e.g., magnetic and gravity sensors. The hub can be implemented with miniature computers, e.g., Personal Digital Assistants (PDAs).

The BodyLAN project is a proof of concept effort that includes hardware, software, and system design and development. We have prototyped and tested the transmitter RF stage and are in the process of prototyping the full transmitter unit. We have specified the transceiver hardware, PEA emulator, hub i/o control, device driver, and potential test applications. We have characterized bit detection through the hardware and simulated bit error rates.

The BodyLAN project is also identifying potential BodyLAN users and component manufacturers. BodyLAN has an open architecture and seeks to define standard interfaces so that multiple companies can find their niche within the BodyLAN architecture and yet interoperate with other components to create an effective BodyLAN.

BodyLAN communicate with the hub through a Time Division Multiple Access scheme to minimize stand-by power consumption of receivers, since they are only used when reception is expected. BodyLAN uses pulse-based spread spectrum transmissions to permit coexistence among nearby BodyLANs and minimize consumed and radiated average power. Devices in a The hub wireless interface is currently designed for a PCMCIA card. This card can be attached to a PDA which acts as the computer "host" running the BodyLAN applications.

This report includes a detailed overview of the development progress at all levels of the system. It discusses critical issues and design considerations that result from our work. The previous report (April 15 -July 1, 1994) described the project goals and considerations in detail.

1.2 System Architecture

The BodyLAN hub consists of a host and attached PCMCIA card. The host runs the applications and the BodyLAN device driver that controls the PCMCIA card interface. The PCMCIA cards implements the wireless i/o transfer. The hub can communicate with several PEAs at the same time and, depending on operating system, can run several BodyLAN applications at the same time.

BodyLAN has been design to minimize complexity of the PEAs, so that power saving and miniaturization can be pushed to the limits. The hub provides the brains of the system, thereby relieving the PEAs of many processing functions. BodyLAN can be thought of as a host (the PDA) with attached peripheral devices (the PEAs). This is a simple model for protocol and application development, yet does not preclude migration to peer-to-peer applications where a PEA may have as much intelligence as the hub and want to run a full network protocol through BodyLAN.

BodyLAN hardware is designed to minimize power consumption. Processing and transceiver functions are suspended until required. The timing mechanism is the only one that needs to remain on continuously. Since processing is minimized and transceiver use is based on scheduled requests, the power savings are significant. The hub hardware and PEA hardware

execute the attachment process by which PEAs join a hub. The PEA "modem" interfaces with the PEA data unit (e.g., sensor or actuator) in a serial fashion. The Hub "modem" interfaces with the device driver in the host through the PCMCIA card interface.

The Hub and PEA modems run link protocols that define the exchange of data and control information, as well as initialization procedures and management of the BodyLAN wireless channel. The device driver treats BodyLAN as a wireless bus with read and write operations to data and control registers of the PEAs. In fact, the device driver operates with local images that mirror the data contents of the actual PEAs across the wireless channel. The device driver and link protocols support a stream and a block transfer mode of operations. Streams are used for continuous transfer of data. Blocks are used for infrequent transfer of a small data set.

The device driver provides an Application Program Interface (API) to applications. In our preferred design, application programs are self-contained programs that can be developed independently based on the device driver API specifications. One company could develop a medical application that works with medical sensors while another could develop virtual reality applications that work with kinematic PEAs. Both could be running at the same time. For the BodyLAN prototype, we need to check if the development environments appropriate for PDAs are also appropriate for the application "multitasking" environment described above. It is clear that this is the direction in which operating systems are developing.

1.3 Description

Since the hub is the brain of BodyLAN, we can start by describing the hub hardware. The hub modem in the PCMCIA card consists of a microprocessor, RAM, an EPLD, and a transceiver unit. A sample block diagram is shown in Figure 1.

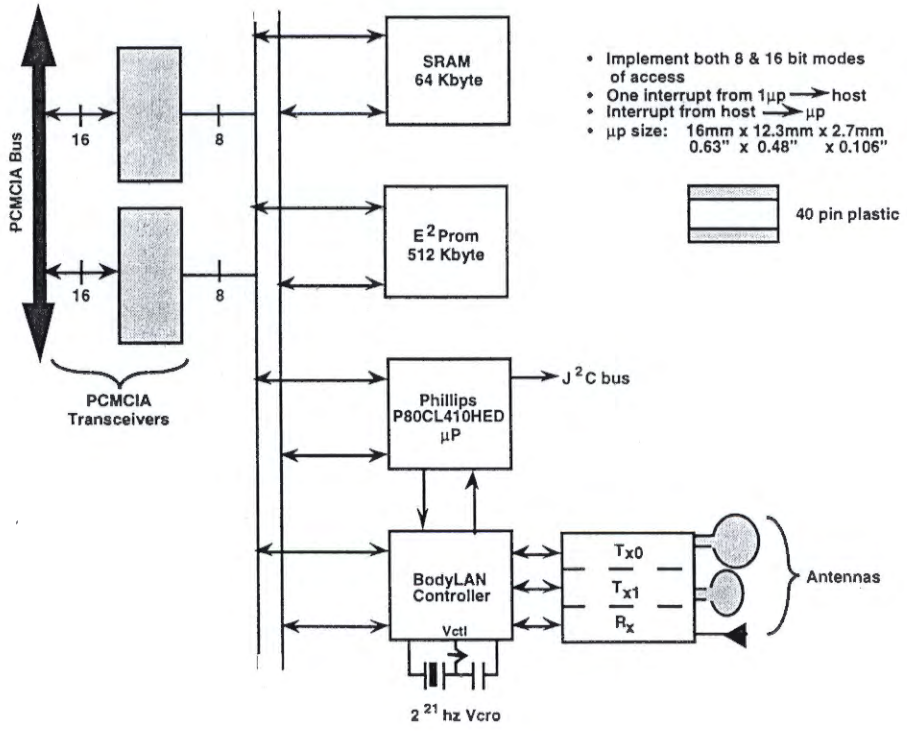


Figure 1:

The transceiver has a crystal oscillator that drives a cascade counter to keep track of the occurrence of events. The events include radio channel sampling instants, spread spectrum chip timing and TDMA framing. The transceiver has a transmitter circuit that is frequency stabilized from the oscillator. The receiver circuitry implements and FM quadrature demodulator operating as an FSK receiver.

Data transmission and reception takes place by loading ping pong buffers in RAM. Every 32 ms a TDMA frame is retrieved from this memory and the active part transmitted to the channel. Similarly, the active part of reception is loaded into ping pong buffers. The Programmable Logic implements this operation and alerts the microprocessor to the availability of data. It essentially re-enables microprocessor operation and points to the code that must be executed. The microprocessor implements fragmentation or reassembly of TDMA frame bits into data units and returns control to the Programmable Logic finite state machine. It also alerts the device driver when sufficient data is available in RAM for the host to take it.

As part of its transmissions, the hub modem inserts in every frame a "synchronization beacon" signal. This is a sparse pattern of pulses and the FSK tones of the pulses form a unique signature for each BodyLAN. A PEA will use a matched filter to detect the arrival of the synchronization beacon and use this event to maintain frequency and chip timing synchronization with the hub, using a phase locked loop mechanism. Similarly, when an "unattached" PEA is within range of the BodyLAN hub, the hub can send an "attachment beacon," which is ignored by already programmed PEAs but is used by the unattached PEA as a command to attached itself to the hub.

The attachment beacon is common to all BodyLANs and only used occasionally. A PEA will attached itself to the first BodyLAN to send it an attachment beacon. The beacon is detected by a matched filter fed by a detector circuit that is oversampling the channel at twice the spread spectrum chip rate. The attachment beacon FSK sequence and its complement sequence are used as a low rate bit serial HDLC channel to download to the PEA the parameters that identify the BodyLAN. These include synchronization beacon specification, spread spectrum sequence specification, and the assigned PEA identification number.

A PEA attaches itself and scans for its synchronization beacon, which also establishes TDMA frame synchronization. Then it looks in a fixed part of the frame for a command and control channel, receives the TDMA plan currently in use and its allocation within it, and is ready for data transfer.

Link protocol define the set of command primitives to achieve data transfer and manage the BodyLAN wireless interface. Two data transfer modes are possible: continuous stream and discrete block. These are possible from PEA to hub and hub to PEA, and mostly initiated by the hub. To preserve bandwidth, reduce interference and power consumption, transmissions are kept to a minimum.

On the PEA side, a PEA modem implements transfer through the wireless link and also has four serial interfaces to a PEA device (sensor or actuator). The PEA modem clocks data from or to the PEA device to implement the data transfer mode and direction. We have defined a Transducer Controller Module (TCM) that emulates a PEA device for the purpose of testing. This module has an LCD and can also interface serially with a host for flexibility of testing.

The commands on the wireless channel and the responses by hub and PEA are governed by the BodyLAN link protocol. It specifies initialization actions and messages, data transfer actions and commands, and BodyLAN management commands and actions. Its style is one of register addressing and it resides as a collection of finite state machine code segments in the hub modem and PEA modem. The device driver in the hub host treats the hub modem as

a computer bus, with register read and write commands. The application at the host uses the device driver through a "socket" interface.

The device driver acts as a dock between applications and PEAs. When PEAs attach themselves and become available, the device driver makes them visible to any present or future application that may request them. When an application becomes active, the device driver connects it to the appropriate PEAs requested, if available.

2.0 Progress Report

2.1 Summary

Since the July 94 Technical report we have made significant progress in all areas of BodyLAN development. We have specifications for the main components of the BodyLAN system, including hardware, interfaces, protocols and drivers. We completed spread spectrum code analysis and bit error performance simulations. We designed and simulated transceivers using SPICE. We fabricated one transmitter stage prototype and tested it in the lab. We are about to fabricate a second prototype with the which includes the digital section.

The issue of PEA synchronization to the hub was a significant risk area and we now have a full design of the synchronization acquisition and tracking hardware and process. Low power design needed verification and we did this through SPICE simulations as well as checking power consumption of the lab prototype.

2.2 Hardware

- Receiver circuit design, including synchronization system
- Simulation of transmitter and receiver stages, including demodulators and detectors
- Fabrication and testing of Transmitter RF stage
- Hub Interface Specification
- PEA Interface Specification
- PEA Hardware Specification
- Transducer Controller Module Specification

This work fulfills the hardware milestones targeted up to December 94 and includes a milestone targeted for the quarter ending in March 95 (start of prototype fabrication). We are about to produce a new transmitter prototype that includes the digital section.

We have also received subcontractor bids on implementing our designs. We are studying them to decide the most cost effective manner to proceed.

2.3 Spread Spectrum

- Optical Orthogonal Code (Spread Spectrum) design tools
- Selection of Optical Orthogonal Code and analysis of alternatives
- Selection of FSK sequence allocation
- Simulation of cross correlation properties
- Simulation of chip pulse detector
- Simulation of Bit Error Rate

This work fulfills the analysis milestones targeted up to December 94 with the exception of the Analysis and Design Report. To preserve project funds, we are using the specifications as the design reports and technical memoranda as the analysis report.

2.4 Protocols and Software

- Specification of data transfer and TDMA allocation
- Specification of wireless channel management
- Specification of PEA and BodyLAN initialization procedure.
- Specification of hub modem interface
- Specification of hub modem Device Driver
- Design of testing and engineering demonstration

- Draft description of "pulse oximeter" demonstration.

This fulfills the milestones targeted up to December 1994 with the exception of the start of software coding. We delayed that milestone because we are reviewing the specifications and the approach to application development in the development environment.

We have also begun exploring in detail possible demonstrations for the BodyLAN system.

3.0 Future Milestones

- Begin software writing
- Hub and Pea microcode
- Receiver prototype

End of MAR 95

- PCMCIA Device Driver
- BodyLAN test application
- PDA software test
- Hub and PEA prototype
- first performance tests

End of JUN 95

- BodyLAN prototype
- Performance benchmarking
- BodyLAN demonstration
- Final Report

End of SEP 95

4.0 Detailed Progress Report

4.1 Hardware Introduction

Three major BodyLAN components have been identified and specified. The HUB modem (implemented on a PCMCIA card), the Personal Electronic Accessory (PEA) modem, and the Transducer Controller Module (TCM). A BodyLAN prototype system employing these three components and their interconnection to the Personnel Digital Assistant (PDA) is shown in Figure 2.

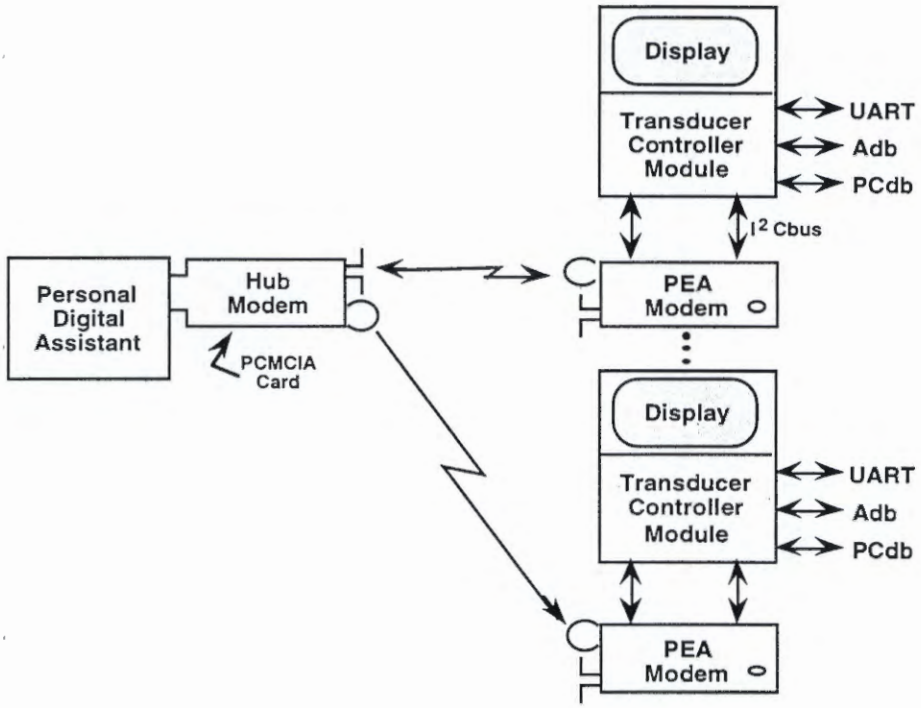


Figure 2: BodyLAN Hardware Architecture

The TCM (not discussed in the last Technical Report) has been introduced to allow separation of the engineering evaluation testing and early application demos from the PEA development. It will incorporate a small 2" x 3" dot matrix display and four serial communications channels in addition to the PEA modem interface. Its primary role is in testing and demonstrating the PEA/HUB communication channel operation. It will demonstrate all major BodyLAN modes or operation (i.e. Attachment, Discovery, Synchronization, Acquisition, and Communication) as well as source and sink both stream and packet data, measure error rates, and show bandwidth sharing.

Significant simplifying and unifying changes have taken place in the hardware architecture since the July 95 Technical Report. These changes have been motivated in part by the desire to reduce hardware complexity and to implement new link protocol concepts on bandwidth sharing. The new architecture is entirely table driven with much more emphasis on flexibility and the use of microprocessor control. Unlike the state of the BodyLAN in the last technical report, we now have an architecture coupling between all levels of the software and hardware with specifications for each major seam.

Significant implementation progress has been made in all areas of the HUB and PEA hardware design. Functional Definition documents have been created for the HUB, PEA, and

TCM. Detailed hardware specifications have been developed for the PEA including PEA microprocessor task definitions. Algorithms have been developed for all BodyLAN functionality which implement the BodyLAN link protocols.

We elected to concentrate development effort on the PEA Modem because it is the more challenging of the two major design tasks. It is more difficult than the HUB because of a much lower power consumption requirement, its synchronization requirement, and its smaller antennas. The implementation effort has been in three major areas, prototyping key RF sections, designing both the analog and digital PEA modem circuits, and partitioning the functional specifications between microprocessor and hardware implemented tasks.

Hardware prototypes of the transmitter and reference clock circuits have been constructed and tested. These prototypes show excellent agreement with the Spice simulations. Preliminary schematics of the Pea modem including both digital and analog section have been completed. About 60% of the schematics for the PEA's one major Field Programmable Logic Device (FPLD) have been completed including a complete implementation of the digital matched filter. A PEA control microprocessor has been chosen (MicroChip PIC16C64) and clocking, interrupt, and interface mechanisms defined for interfacing the microprocessor to the FPLD.

4.1.1 Transducer Controller Module

A functional specification has been developed for a new component to allow testing and early BodyLAN insertion into new applications. This component is called the Transducer Controller Module (TCM). Its major components are a relatively small dot matrix display and four serial interfaces. Its 2" x 3" size matches the size of the prototype PEA and thus will allow demonstration of a pocket pager size PEA/TCM plug together showing full functionality.

It will incorporate serial communication links for the Apple desktop bus, the IBM desktop bus, and UART in addition to a conventional I2C serial bus. These links will allow attachment of a wide assortment of existing transducer devices (e.g. Blood Oximeter, FluxGate monitor, Instromedix ECG monitor, Apple keyboard and mouse, Twiddler Keyboard) if funding is available to develop the controlling microcode.

The primary role of the TCM is not to serve as a means for BodyLAN application demos but rather to serve as a mechanism for the engineering evaluation of BodyLAN. The TCM specification calls for the ability to display the state of the PEA microprocessor via the receipt of I2C messages from the PEA microprocessor. This will allow us to demonstrate and monitor all major functionality. One of its main benefits is that it will provide a normal microprocessor environment. We expect, for example, that the TCM's processor clock to be constantly enabled. This is in contrast to the PEA microprocessor environment where the clock is inhibited for 98% of the time.

In addition to the display of PEA microprocessor state, the initial TCM functionality calls for the sourcing of a repeatable arbitrary block of data on one or more of the user data channels, the sinking of data from the HUB, and loopback of data received from the Hub back to the Hub. Data received from the Hub will be checked and simple error rate computations made. The number of errors in a given time interval will also be fed back to the HUB via I2C packets fed to the PEA microprocessor and delivered via the Command and Control Channel.

In the current plan, the TCM will be implemented by an outside company to BBN supplied specifications. A statement of work has been developed and bids are being solicited.

4.1.2 Architecture

The PEA modem has two fundamental modes of operation: non-table driven and table driven. In the non-table mode, PEA operations are activated by matched filter detection events. In this mode, the PEA Data Path (PDP) chip performs 128 million additions per second matching oversampled received data with 32-bit Attachment or Synchronization Beacons patterns. In table driven mode, all PEA operations and and their occurrence relative to a repetitive 32 Hz frame are controlled by entries in an SRAM. The frame period is frequency and phase locked to the HUB. Since this mode consumes several orders of magnitude less power, one goal of the architecture is to spent as little time as possible in the non-table mode of operation.

There are five primary PEA processes: Attachment, Discovery, Synchronization, Acquisition, and Run. Each process is implemented through close interaction of PEA microprocessor instruction execution and PDP chip hardware primitive activities. To reduce complexity, our design philosophy has been to migrate as much functionality as possible into the microprocessor. The role of the PDP chip is to implement those functions which cannot be practically implemented in the microprocessor such as the Matched Filter, charge pump, phase detector, etc. Through the course of the microprocessor code development, several of the microprocessor functions may be moved into the PDP chip when microprocessor implementation warrants a simplification.

The Attachment Process is initiated immediately following the release of Reset or after the microprocessor has received a Command and Control Channel (CCC) packet indicating PEA Reset. While in Attachment, the PEA has none of the parameters which are needed to Discover and Synchronize with its home HUB. A PEA would be in this state when purchased. While in this state the PEA periodically searches a particular spectrum band for a sequence of spread spectrum coded signals which we call Attachment Beacons. These Attachment Beacons have the same burst distributions as the Synchronization Beacons normally transmitted by the HUB and can be detected by the PEA matched filter preset to a predefined code. The sequence of Attachment Beacons forms a 256 bps asynchronous channel. Over this channel, a single packet is repetitively transmitted by the HUB with a conventional HDLC inter packet separation byte and bit stuffing protocol. This packet, called the Attachment Packet contains all the information needed by the PEA to Discover and Synchronize itself with the home HUB. While power consumption during Attachment is quite high (estimate 8-10 milliwatt), the power on/off duty cycle of 1/1300 results in acceptable power consumption.

In Discovery, the PEA periodically monitors the HUB->PEA frequency bands for Synchronization Beacons (SBs). SBs are similar to Attachment Beacons. Currently an SB is made up of 8 RF bursts each of which is composed of four FM modulated symbols above or below the carrier frequency. The 8 4-tuples which make up the SB are quasi unique to each HUB. These eight 2 microsecond RF bursts are spread out in time over a 260 microsecond interval to give about the same RF density as used in normal data transmissions. The first four 4-tuples are limited to 0011 or 1100 to simplify phase locking the PEA to the HUB. This provides a code diversity of only 20-bit. Since the matched filter matches with up to two errors, the probability of detecting an SB from a foreign HUB is only about 1/2500. To reduce the probability of locking onto a foreign HUB, eight SBs are transmitted per frame at locations within the frame unique to each HUB. This increases the diversity by about 16 orders of magnitude and makes the probability of locking onto a foreign HUB vanishingly small. At the end of the Discovery process the PEA has established that the SB being received are originating from its home HUB and an approximate idea of HUB framing.

After Discovery, the PEA begins the Synchronization process. In this state, the PEA varies its VCXO frequency to lock onto the arrival of the SBs. Since the PEA knows the approximate temporal locations of the SBs, a 15 to one power consumption reduction is

possible by enabling the detection of SBs for only short periods of time. After the frequency locking part of Synchronization has occurred a table is created by the PEA microprocessor and the table driven mode of operation is entered. The Pea then achieves phase synchronization by locking onto only the 0->1 and 1->0 frequency transitions in four of the SB bursts. Power consumption in this mode is dramatically reduced because here a much simpler matched filter is used and power on/off duty cycle has been reduced to 1/500. Note the phase synchronization continues throughout the entire Acquisition and Run states until SBs are no longer received by the PEA.

The Acquisition process is entered following Synchronization. In this process the PEA and HUB microprocessors exchange packets over a relatively low bandwidth channel (defined in the Attachment Packet) which we call the Command and Control Channel (CCC). After Acquisition, the PEA has a TDMA plan in its SRAM which corresponds to that of the HUB and the application code appropriate to service the particular Pea is ready for use by the Hub's host processor. The Pea then begins transferring user data. During this phase, which we call Run mode, the PEA continues to send periodic status nibbles to HUB and will respond to commands over the CCC. What operations and when they will be performed is controlled by a table contained in SRAM which we call the Event Table. Each entry in this table contains a 14-bit quantity which indicates when the event is to be initiated, a 6-bit Event Op code, and two 6-bit event parameters. While all table entries are accessed once per frame, some entries do not cause any activity because they were not enabled by received data earlier in the frame. Some events conditionally cause the PEA microprocessor to be awaken to participate in the operation. This simple event scheduling scheme unifies the implementation of all known BodyLAN functionality while still preserving low power consumption and flexibility.

4.1.4 Voltage Controlled Oscillator

Central to PEA functionality in both table and non-table modes of operation is the Voltage Controlled Crystal Oscillator (VCXO). The underlying assumption in the entire BodyLAN architecture is that a low power PEA oscillator can be constructed which can be phase locked to the HUB with only occasional voltage updates. It must have sufficient stability to have low drift rates between updates. The VCXO and a companion 25-bit counter are never powered down as they supply all circuitry with the capability of powering down. From a power consumption standpoint, it is desirable to have a low VCXO oscillator which must be phase locked to a lower frequency VCXO on demand adds considerable complexity and introduces a significant noise source for the RF oscillators.

The VCXO design to be used in the PEA prototypes is based on an ISCC journal article design for a CMOS chip implementation and has been modified to use bipolar transistors. The VCXO, varactor charge pump, and output amplifier is shown in Figure 3. A 3 volt peak to peak output drives one PDP chip input. Power consumption of the VCXO and charge pump is well under one microwatt while power consumption of the output amplifier is about 40 microwatts. In a CMOS implementation, the ISCC journal article showed power dissipation for the CXO and 3 stages of counters under 1 microwatt.

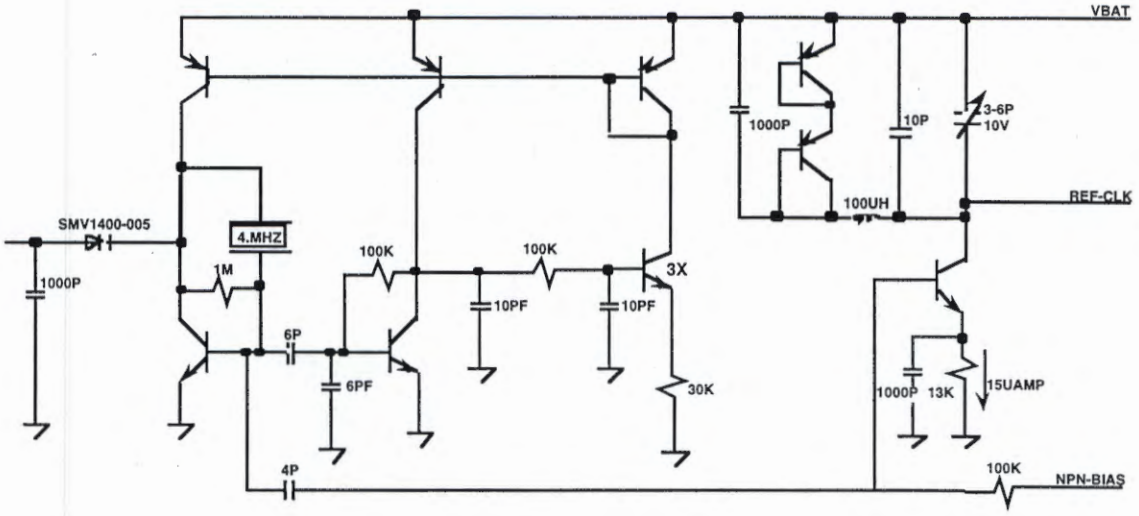


Figure 3: Voltage Controlled Oscillator

The VCXO frequency selected is 4 MHz with the ability to vary the frequency by +/- 50 parts per million. We have built and begun testing a breadboard of the VCXO part of the circuit to verify its power consumption, tuneability, and supply voltage sensitivity. The circuit has demonstrated correct operation and tuneability but has somewhat higher power consumption than estimated. We are currently in the process of incorporating higher Ft NPN transistors to see if the beta dependence on frequency is the reason for the higher power consumption. Note that a CMOS implementation would not have this problem.

4.1.5 Transmitter Breadboard

The PEA transmitter minus the frequency modulation and frequency locking subsection was breadboarded during the last period. This circuit was the first BodyLAN circuit to be fabricated and served to introduce the design engineers into the 'art' of RF design. The breadboard is a two layer, 1" x 2" PC board having 20 discrete components in addition to the Tx antenna. The antenna was a single loop, two centimeters in diameter.

While the breadboard began transmitting immediately upon battery insertion, the stories about the nasty surprises encountered by RF circuit designers in their breadboards are clearly true. While BodyLAN plans to utilize a relatively low RF frequency (300-400 MHz), substantial consideration must be paid to reducing parasitic capacitances, especially at the high impedance levels planned for BodyLAN circuits. In addition, while oscilloscopes have the bandwidths to view the RF waveforms at these low frequencies, we found that special care must be given to scope grounding (i.e. less than 0.2" wire is OK), and that the large probe capacitance (1.5p) has an effect on the circuits.

Measurements were taken using a one-quarter wavelength antenna into a spectrum analyzer. While we have not yet established a calibration of the antennas Db to field strength, it is clear that the transmitter's radiated signal is more that large enough to receive and is 25 Db greater than any other signal over the 100-1000 MHz range even at the maximum 1.5 meter antenna/transmitter separation distance.

Power consumption was disappointing with a five volt peak-to-peak antenna voltage occurring at 800 microamps. Spice simulations predicted only 200 microamps would be needed. The problem was the low antenna Q. Implementing an antenna using a 2.5 mm copper foil antenna instead of the PC board etch antenna reduced the current needed for maximum output to 450 microamps. The measured Q of both the PC board etch and copper

foil antenna are about a factor of three less than predicted by rough skin effect loss calculations. While this power consumption is higher that expected, it is not a major concern since transmit power is only a small fraction of receive power consumption.

4.1.6 Hardware Design

Our design philosophy in the BodyLAN hardware development has been to first put in place a preliminary design of every single section. We then iterate the design as new ideas are discovered and/or the breadboards uncover problems in the design. We have now made multiple passes over all the RF and analog sections and are nearing completion of a design of the digital sections. This has resulted in the creation of hardware Functional Specification document s for the HUB, PEA, and TCM together. Detailed descriptions of the PEA hardware and a PEA microprocessor programming manual have also been generated as a byproduct of creating the full set of PEA schematics. We have also generated schematics for the two versions of transmitter breadboard, the VCXO breadboard, and the first receiver breadboard. Approximately 60% of the PDP chip schematics have been generated to examine whether all the functionality can be incorporated into a single FPLD or a second chip will be required. No activity in the HUB design has been started other than to acquire a full set of PCMCIA specifications.

We have elected to defer the slow frequency hopping feature of BodyLAN until the end of the project. This reduces the complexity of the LNA since with a fixed Rx frequency, no dynamic tuning of the antenna matching nor cascade load circuits need be implemented. We can simply use trimmer capacitors and manually trim to the 384 MHz HUB->PEA carrier. This also means that the Rx and Tx oscillators need only sufficient dynamic tuning to compensate for voltage, temperature, and component variations.

4.1.7 Low Noise Amplifier

A more conventional low noise amplifier has been adopted rather than the transconductance amplifier previously suggested. Simulations show excellent noise numbers with a much higher probability of a successful LNA breadboard when PC board parasitic capacitances are taken into account. The high Q dipole antenna will be matched to the low noise BJT using a resonant circuit manually trimmed to 384 MHz. A simple cascode circuit is employed in the first stage having a simple tank load. This allows us to easily compensate for the PC board trace capacitance and still achieve good front end gains.

Circuit simulations show more than 30 Db of gain at better noise figures than were achievable with the transconductance amplifier. Interestingly, the antenna matching inductance equivalent resistance was a major noise contributor at 200 micro amp transistor currents.

4.1.8 Discriminator

The receiver detects that the incoming signal is above or below the carrier frequency by limiting the signal formed by the product of the I and derivative of Q minus the product of Q and the derivative of I. This little used discrimination is popular in direct conversion demodulators but suffers from several problems.

The first problem is that it is difficult to develop dI(t)/dt and dQ(t)/dt without amplifying noise. Limiting the bandwidth of the differentiators introduces phase errors at IF. We have solved this problem by noting that the frequency discrimination function works just as well if instead of X we use X phase shifted by N degrees and instead of using dX(t)/dt we use X phase shifted by N-90 degrees. Simulations have shown this to give identical waveforms as using X and dX(t)/dt. Standard 90 degree phase shifter networks can now be used with this

observation. This not only remove the active dX()/dt stage but removes any phase shift anomally.

The second problem is dynamic range. If the I and Q signal are to have a 200 to one dynamic range as PEAs are brought in from their maximum range, the product terms of the discriminator output (e.g. I(t)*dQ(t)/dt) have a 40,000 to one range and therefore become very sensitive to DC offset voltages. We have discovered that by employing dX(t)/dt on one side of the multiplication and Lim[X(t)] on the other side of the multiplication that the discriminator works almost as well. The negative is that the locations of the actual versus the discriminator zero crossings now suffers an ambiguity of about +/- 40 nanoseconds. This ambiguity goes to near zero for low level inputs and is maximum for the largest input. This of course is just what is desired as at high input levels, noise is not a problem.

The benefits of this limiter scheme is that now the dynamic range has been reduced from 40,000 to one to about 300 to one. If the system has a maximum final limiter input of 1000 mv peak-to-peak, the 300 to one range now reduces the minimum limiter input to 3.3 mv. Thus the minimum limiter input is much greater than the offset voltage of final limiter.

4.1.9 Frequency Control

The PEA contains three subsystems needing frequency control: the receiver local oscillator, the transmitter oscillator/modulator, and the VCXO. Since measuring the frequency of these oscillators necessitates significant power consumption, BodyLAN employs a non-conventional sampling approach. Here a frequency is measured quasi periodically and then for only a very short period of time. One of the ancillary benefits of this approach is that it allows us to time share much of the logic.

Oscillator frequency stability over multiple power up/down cycles is central to the success of this scheme. In normal operation, for example, the RXLO may be powered up for 2 microsecond periods f50 times over an interval of four milliseconds before a frequency adjustment cycle is initiated. Fortunately, the +/- 150ppm frequency stability requirements of BodyLAN are about two orders of magnitude less severe than in conventional narrow band wireless modems.

BodyLAN unifies all frequency control by mapping the measurement into the comparison of two intervals each of which has the start or stop referenced to the reference and the stop or start referenced to the frequency under test. For example, in measurement of the RXLO frequency, start time of the two intervals is referenced to the VCXO while the stop time of the two intervals is referenced to the RXLO prescaler output. A Duration Interval Comparitor circuit (shown below) provides an indication of which interval is longer and when the intervals are approximately equal. Approximate equality is detected when the comparitor inputs are sufficiently close to one another that the output is neither a logic one nor a logic zero. This equality measurement capability has been found to improve frequency lock stability and reduce the maximum deviation.

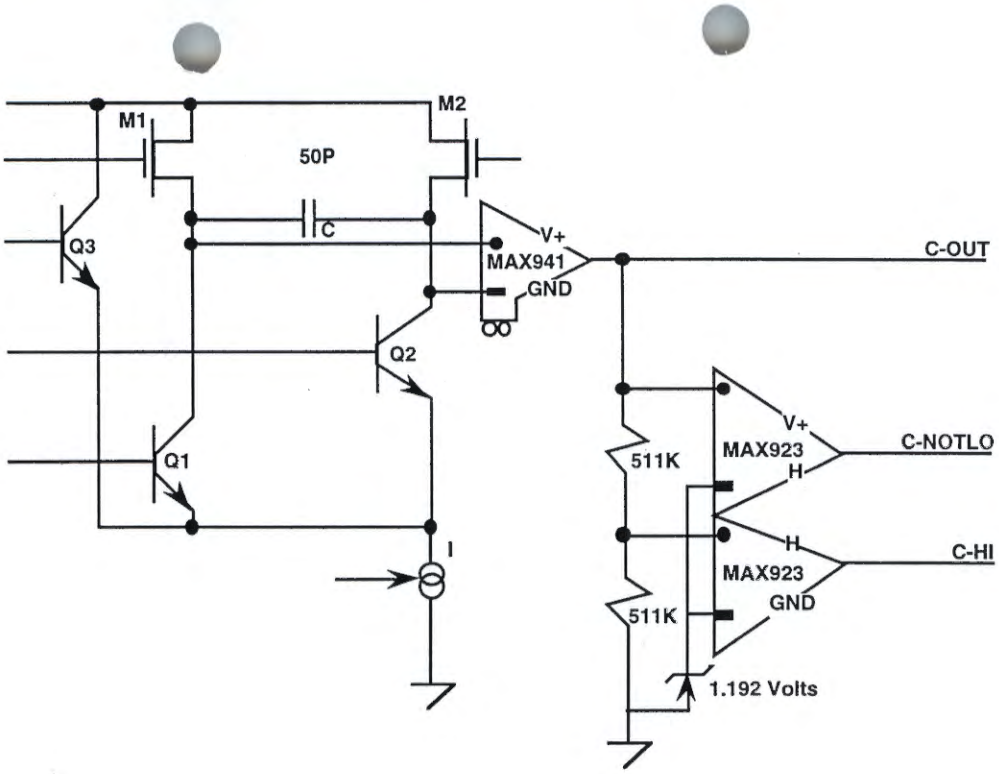


Figure 4: Duration Comparitor Circuits Here

Between frequency measurements, matched JFETs M1 & M2 are biased on thereby shorting capacitance C. Shortly before the first interval comparison, programmable current source I is enabled with transistor Q3 biased on. This diverts the current to the supply rail. During the first interval, current source is routed to the positive side of the capacitor and the current source turned off. The process is repeated for the second interval this time routing the current to the negative side of the capacitor. Since the programmable current source can be different between the two measurements, we can compare non-equal durations.

4.2 Protocols

The basic BodyLAN protocols were designed to be lightweight as well as bandwidth and power efficient so that they can be implemented on simple PEA devices without requiring too much power or circuit complexity.

As shown in Fig. 5, the protocols provide a logical connection between the low-level communication interfaces on the Hub and individual PEA. On the Hub, the interface assumes the form of device abstraction. To the system software of PDA, every PEA appears as an I/O mapped device. The Device Driver may read/write the data buffers, access the control and status registers, and receive interrupts from these I/O mapped devices. At the PEA, the interface appears as four unidirectional modem channels, to which the User Devices are attached. Data flow through these channels according to programmed modes. The protocols support timely update of PEA device abstraction and evocation of communication action. Nonetheless, it is rudimentary in its data communication functions. Currently, we decide not to support error detection and packet retransmission for data transfer.

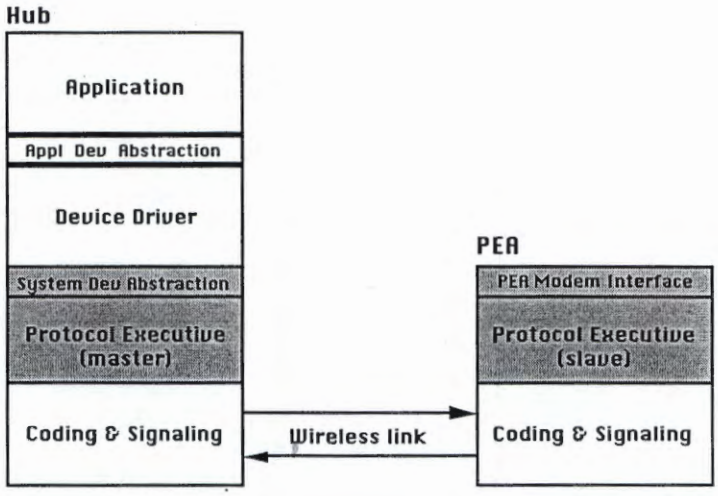


Fig. 5: BodyLAN Protocol Stack

In the remaining of this section, we will describe briefly the device abstraction, the TDMA assignment, and the packet formats used by the protocols. This description reflects the current design of link protocols. They are undergoing review from and system perspective.

4.2.1 Device Abstraction

The BodyLAN is designed to be a wireless bus which can accommodate a total of 56 PEA devices. Each PEA occupies an image block in the PDA's I/O map [Fig: 6]. The block is addressed by a six bit PEA ID assigned to the PEA during its attachment to the BodyLAN. Each PEA image block consists of a data buffer, which contains the incoming or outgoing data, and 16 registers, which are further divided into five register files: one for the device and one for each of its four Data Channels. The contents and the use of the registers are described below.

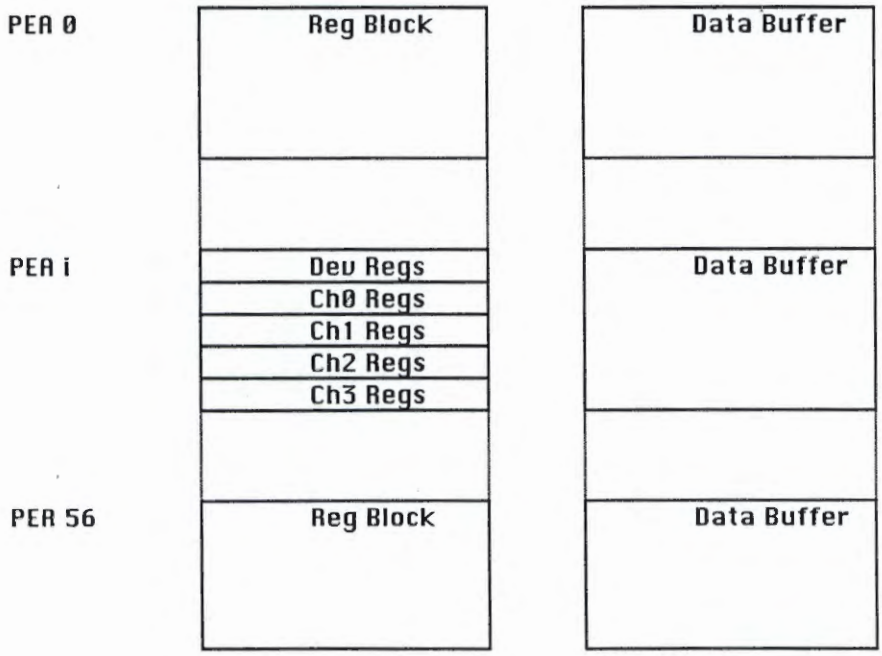


Fig. 6: Hub Device Abstraction

Device Registers

Each PEA has four device registers: the Control Register, the Status Register, the TDMA Plan Storage, and the PEA Parameter Storage.

The Control Register specifies the operational parameters of the radio transceiver. Parameters under consideration are:

Inbound Frequency	frequency band used for PEA to Hub communication in a slow hopping system
Outbound Frequency	frequency band used for Hub to PEA communication in a slow hopping system
Transmitter Power Level	preset levels of transmitter power to compensate the diminishing signal power due to Hub-PEA distance
Receiver Power Gain	preset levels of receiver gain to compensate the diminishing signal power due to Hub-PEA distance

and the Status Register contains the fields that reflects the current state of the PEA device:

Device State	Inactive or Active Low Battery Flag High Error Flag
Battery Level	threshold indicator of PEA battery level
Bit Error Count	scaled count of bit encoding errors; a high error count indicates the existence of high interference
Overrun / Underrun Error Count	scaled count of overrun/underrun data blocks; a non-zero value implies insufficient throughput

The TDMA Plan Storage maintains a specification of blocks in a TDMA frame that are assigned to the PEA for command and control and data exchange. The PEA Parameter Storage will be programmed by the PEA manufacturers to specify the type and the communication requirements of the device. Hence, the PDA software can program and monitor the operation of a PEA by accessing its Control and Status Registers, learn its configuration by reading the PEA Parameters, and assign TDMA blocks by writing the TDMA Storage.

Channel Registers

The operation of each Data Channel of a PEA is controlled and monitored through a pair of Control and Status Registers.

The Control Registers consist of fields that specify the following communication parameters for each channel:

Channel Direction	Inbound: from PEA to Hub Outbound: from Hub to PEA
Stream / Block Transfer	This specifies whether the data will be transferred as a continuous stream or in distinct blocks.
Poll / Automatic Trigger	This specifies whether the data transfers will be initiated by the Hub through explicit pollings or by the PEA when data are available.

Bit Coding Scheme	This selects an encoding scheme for carrying the data bits over the modulating symbols.
Error Checking Scheme	This selects a checksum-based error detection scheme for the data packets.
Packet Byte Count	This specifies the size of data packets used in the block transfer

Similar to the status registers of microprocessor-based I/O devices, the PEA Status Registers contain fields that show if the transceiver buffers are ready for data and if errors have occurred in the previous data transfer.

4.2.2 TDMA Architecture

Three kinds of communication channels run between the Hub and an attached PEA. First, there are two command and control (CC) channels, known as the Basic and the Extended CC Channels; one BCC Channel and a maximum of eight pairs (inbound and outbound) of ECC Channels exist within each BodyLAN. In addition to the CC channels, there are four Data Channels for every PEA. Each supports a unidirectional communication between the PEA and the Hub.

The basic concept underlying the TDMA architecture is bandwidth sharing -- several channels of different PEAs may use the same blocks in the TDMA frame as long as no contention will occur. The BCC is shared by all attached PEAs; each pair of ECC can be shared by a group of seven PEAs; finally, the Data Channels of any number of PEAs may share a TDMA block if they use Block Communication Mode and are in the same direction. Data Channels in Stream Communication Modes, however, must use dedicated TDMA blocks in order to avoid indefinite wait. The reason to support bandwidth sharing is to enable more efficient use of the bandwidth. By sharing the TDMA blocks among a number of channels with statistically low data throughput, we can assign the TDMA blocks according to the peak bandwidth of the data channels (and thus achieve low communication latency) while maintain a high utilization of the blocks.

The use of the two types of Command and Control Channels may require further comment. The single BCC Channel is shared by all 56 PEAs to report their status and to listen to broadcasting commands. The channel is also used to evoke special actions such as reset of individual PEA. The eight pairs of ECC Channels, on the other hand, are used for downloading TDMA assignment to individual PEA, accessing device registers on the PEAs, and initiating data transfers. The outbound channels are used to send commands and the inbound channels to receive corresponding replies. The ECC Channels are assigned to individual PEAs based on a grouping of the devices according to the six-bit PEA ID. The 56 PEAs are divided into eight groups with either the upper or the lower three bits of the PEA ID as their Group Numbers and the other three bits as their IDs in the group (Group IDs). Each group of seven PEAs are assigned with a dedicated pair of ECC Channels. Individual PEAs are identified when using the ECCs by their three-bit Group ID, which will be the first field in the command packets.

Currently, eight bits per frame is assigned to each inbound and outbound ECC channel. The bandwidth is sufficient to send a read register command (16 bits) in two frames, a write register command (28 bits) in four frames and receive a reply to either (9 or 13 bits) in two frames. The band-width is also sufficient to download a UDIB-level TDMA block assignment (40 bits) to a PEA in five frames or a symbol-level TDMA block assignment (48 bits) in six frames. These communication rates allow a Hub-PEA exchange in 1/8 second and the download of one TDMA entry in 1/5 second.

4.2.3 Packet Formats

Among the three kinds of channels travel two types of packets: (1) *command and reply packets,* and (2) *data packets.* The command and reply packets travel only in BCC or ECC Channels while the data packets always go in the Data Channels. Consequently, they are completely separated in their paths and have different formats. The command packets can be further categorized into Network Management and Device Control Commands.

4.2.3.1 Network Management Commands

These commands, traveling only in the BCC Channel, are used to monitor the status of the PEAs attached to the BodyLAN and initiate network-wide actions. The command set consists of the following *five* commands and their continuation: (1) *Status Polling from all PEAs,* (2) *ACK Polling from all PEAs,* (3) *Command Broadcasting to all PEAs,* (4) *Command Sending to Individual PEA,* and (5) *Reply Receiving from Individual PEA.*

The continuation op-codes are needed to allow the commands or their replies to be extended beyond the frame boundaries. For example, in order to poll the status of all 56 PEAs, the Hub must issue a status polling start command in the first frame and a status polling continue command in each of the next seven frames in order to read in the device status in groups of seven. The acknowledgment from all PEAs can also be polled in a similar fashion. The continuation of commands however simply allow the commands to extend across the frame boundary. The acknowledgment from individual PEA does not need a continuation as it is short enough to be contained in a single frame.

Since the first block of a frame in the BCC Channel is always filled with one of the op-codes, the channel is always busy. The default activity is status polling, which has the lowest priority. The broadcasting command has the highest priority and the command to individual PEA follows. Acknowledge must takes place following a command to the PEAs; hence, they assume the highest priority after the issuing of a command.

4.2.3.2 Device Control Commands

The Device Control Commands are used for two major functions: (1) to monitor and control the operation of individual PEAs and their data channels, and (2) to initiate data transfers. Since the PEAs are modeled as blocks of registers, their monitoring and control can all be done by accessing the registers. Hence, the command set is further divided into Register Access and Data Transfer Commands.

Register Access

Every Register Access Command demands a reply. The command and reply packets have different formats, but are both delimited by the synch marks appearing after the frame boundaries.

In a command, immediately following the synch mark is the PEA's Group ID, which is the ID of the PEA in its assigned group. By examining the Group ID, a PEA can determine whether it should further listen to the command. If not, the PEA turns off its receiver. After receiving the command, the addressed PEA examines the checksum. If the command is received without error, the PEA obeys the command and returns a reply to the Hub with an ACK and possible data. Both replies contain checksums for error detection. When the Hub receives a NAK or an invalid reply, it will issue the command again and the PEA will respond accordingly.

Data Transfers

The Data Transfer Commands are used to initiate block or stream communication between the Hub and the selected PEA. Unlike the Register Access Commands, Data Transfer Commands do not require replies through the ECC Channels. Instead, they trigger data transfers through the specified data channel. The reception of an End Command before a Start Command will cause an Overrun/Underrun Error. The reception of an End Command after a Start Command but before the actual data movement will cancel the data movement and also cause an Overrun/Underrun Error.

All data movements through the data channels begin after a frame boundary and are marked by a frame synch mark. Opposite synch marks are sent in all other frame boundaries. It is decided that retransmission will not be supported in either data transfer modes; however, it is still undecided if the stream transfers should be packetized and if checksum should be included in the block transfers.

4.3 Device Driver and I/O Control

BodyLAN's system architecture is based on a model which represents PEAs as simple, bus-attached devices. BodyLAN's communications sub-system is regarded as a distributed, wireless transaction bus (called WBus). WBus is implemented by embedded hub software. In addition to managing the hub hardware, the BodyLAN device driver uses the WBus communications sub-system to manage PEA devices. The structure of this software was strongly influenced by two design goals: to minimize the software complexity; and to minimize power consumption, particularly in PEAs. We will present an overview of each of the main software components.

4.3.1 BodyLAN I/O Control

The embedded hub software runs on the hub's microprocessor and implements the BodyLAN WBus, the communications sub-system that allows a personal computer or PDA to access PEAs. Its primary functions include interfacing with the RF modem's controller hardware to execute frame I/O, implementing the WBus engine, and providing a convenient management interface for use by the device driver. The organization of the embedded hub software is further illustrated in Figure 7 below.

The "WBus SAR" performs "Segmentation And Reassembly" of bus messages, a function that is required because communication channels do not typically have sufficient assigned bandwidth to allow transmission of an entire message within a single frame. The WBus SAR interfaces with the modem controller, accessing its Data Buffer -- a ping/pong dual port frame buffer -- 32 times each second to perform frame I/O operations. The allocation of data bits in incoming and outgoing frames is specified by the RxPlan and TxPlan respectively, allowing the WBus SAR to perform input or output for each communications channel using a virtual synchronous bit-stream.

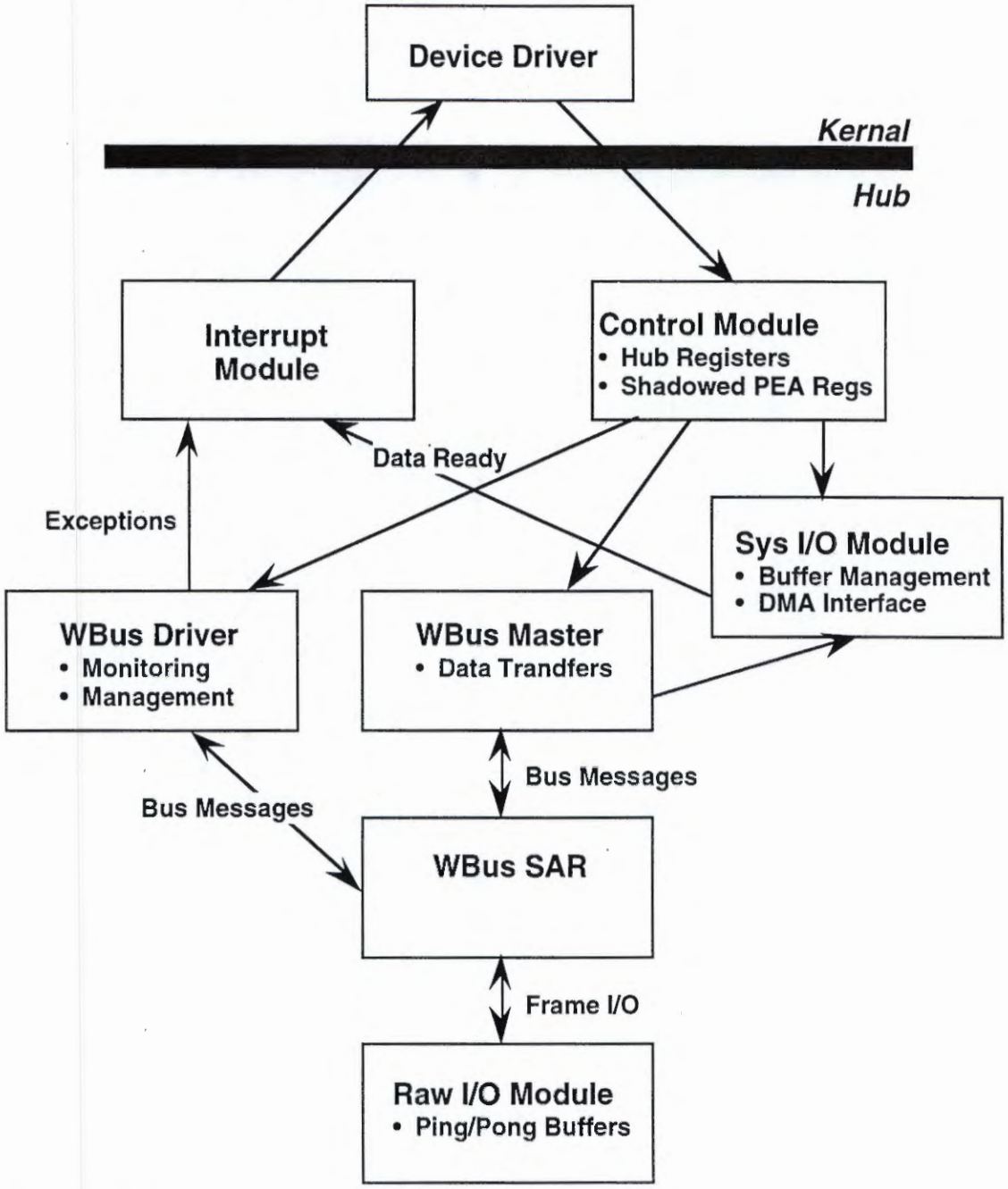


Figure 7: Hub Software

The WBus SAR uses the following input processing procedure. There is a reassembly buffer for each possible data or control input channel. Each reassembly buffer is tagged with state information describing the input process for the associated virtual channel -- whether the channel is active, the type of information being received, the amount of bits already reassembled, etc. The WBus SAR must be able to detect the beginning of message on any channel with incoming bandwidth. The modem controller may provide auxiliary signaling information along with incoming frames in order to simplify that task. The expected length of a control message is determined from the message type. For data messages, the expected length is determined by interrogating the appropriate PEA control registers. Reassembled messages are delivered to either the bus driver or bus master modules for processing, along with tags identifying the input channels from which they were received.

The WBus SAR uses the following output processing procedure. Outgoing messages accepted from the bus master or bus driver are tagged and stored in an array which has an element for each possible outgoing channel. The WBus SAR must be able to queue outgoing multiple messages for individual channels. Exception handling procedures must be defined for handling "channel congestion". The message segmentation procedure that is used to generate output frames is described by the following pseudo code:

The "WBus Master" performs data transfer transactions. Write requests effect data transfers from the hub to PEAs; and read requests effect data transfers from PEAs to the hub. The bus master writes/reads control data directly to/from hub memory, but interacts with the "System I/O Module" for exchanging user data. The WBus supports the following data transfer transactions:

* Block read from/write to an addressable register area or a data area.
* Stream read from/write to a data area.
* Auto block read from a data area -- PEA forwards the next data block once accumulated.
* Isochronously auto block read from a data area -- PEA isochronously forwards data blocks as they accumulate.

The details of the data transfer (and all other bus) transactions have been defined in the specification of the communications protocol for the bus (Section 4.2). which is also referred to as the BodyLAN Link Layer Protocol.

The "WBus Driver" performs bus monitoring and management functions. It is responsible for all bus operations and events that are not associated with data transfer transactions. These include initiating device probe/attachment procedures, periodic status polling of attached devices, and managing bandwidth allocations for example.

The hub software's device driver interface is defined collectively by the "Control Module", the "Interrupt Module" and the "System I/O Module". The Control Module has a group of hub control registers that provide the primary method by which the device driver can control the operation of BodyLAN. The register group includes a command register, a command argument register, and a command status register. The Control Module also includes "shadows" of the control registers on each of the PEAs participating in the BodyLAN. The PEA registers have been defined but will not be discussed in detail. Writing to the PEA register shadow area will cause the Control Module to send an update to the appropriate PEA. The Interrupt Module generates maskable hub interrupts when the hub needs to deliver data to the kernel, and when an exception has occurred. The System I/O Module manages ring buffers for each possible communications channel, and carries out DMA transfers between system memory and hub memory.

4.3.2 BodyLAN Device Driver

The device driver interfaces the kernel with the BodyLAN hub. It will map the hub memory into the kernel's address space so that hub memory is addressable by the kernel. It will interact with the hub's Control Module to carry out configuration and/or initialization procedures that are required to activate a BodyLAN, and will handle interrupts generated by the hub's Interrupt Module.

The device driver's application interface will allow applications to perform PEA I/O operations using existing facilities for file manipulation. Applications will be permitted to directly access the PEA control registers stored in hub memory in order discover the nature and state of PEAs that are participating in a BodyLAN. Applications will be able to "connect" to PEAs' data sub-channels, and to perform I/O and bandwidth management operations for such connections. The device driver will not perform data replication if multiple applications attempt to access a single PEA sub-channel.

4.4 Spread Spectrum

The data protocol for BodyLAN uses Optically Orthogonal Codes (OOCs) as one of several methods to withstand the interference of multiple, adjacent BodyLANs. We tested that design idea through computer simulations. The simulations attempted to reveal the circumstances that would favor signal integrity and the expected bit error rates under various forms and power levels of interference.

Each OOC code is characterized by one or more sets of code words consisting of a sparse pattern of pulses. Only one such set must be selected for use. Pulse signaling is done by an FSK method within each pulse. When received, each code word ultimately is interpreted as one bit.

The OOCs that were explored for use with the BodyLAN were {63,3,1}, {64,3,1}, {64,4,2}, {128,3,1} and {256,3,1}. The intent of the simulation was to explore all possible interference possibilities with their expected chip error rates and, from those rates, using a simple "majority voting" scheme, the expected bit error rates. The simulation included the following realistic factors:

1. Asynchronous behavior of the interfering signal with the desired signal, so that partial overlaps of the chips were possible
2. Various power ratios of signal to interferer
3. All possible combinations of interfering code word pairs
4. All possible signal code words

Since the problem is combinatorially explosive, a simplifying stratagem was used: interferences were categorized by type and were logged as such. Then, having essentially created a histogram showing the absolute number of interferences of each type, a detector model was introduced to reveal the chip error rates, and from that, the bit error rates.

The simulation was done computationally, allowing each code to be the "desired" code. For each such case, all code pairs would take turns as the "interferer." A chip was said to be correct when there was more energy at the expected frequency than at the interfering frequency. In cases of a tie, a random choice decided. A bit was said to be correct when a majority of its chips were correct. For 4-chip codes, ties were resolved by a random choice.

General results:

- Code words with adjacent active chips had strikingly poor performance. The cause for this peculiar behavior was found to be generic and uncorrectable. As a result, such code words were excluded from further consideration in transmitting data. (They still could be used for transmitting the less frequent beacons.)

- Frequency alternation of successive chips is a major advantage.

- Code diversity (i.e., more codes) reduces bit error rates.

- Theoretically poor codes (e.g., {64,4,2}) might be desirable, since the gains from frequency alternation and code diversity are greater than the loses from the autocorrelation of 2.

- Even with the power of the interferer being, unrealistically, 10x the power of the desired signal, and with a {64,4,2} code, bit-error rates were only of the order of 1 in 200.

Work on simulation of interference between the OOCs of two BodyLANs was greatly advanced by arrival of the project's 90MHz Pentium PC. The complete interference analysis is combinatorially explosive, since all codes can be interfered with by all other asynchronous overlays of all code combinations, and at various power levels. For such complete analyses, we speeded up the computation by breaking it into two parts:

1. Creating a histogram for the kinds of possible interference events

2. Simulating the detector circuit's response to each kind of interference event only once and then multiplying by that event's frequency of occurrence

For part 1, the first complete calculation covered an OOC with ten codes (n=10), each 64 chips wide (w=64). It is easily shown that the calculation time varies as (n^3)(w^3) or 2.6x10^8, and each such calculation requires a 64*64 dot product. The compute time was 66 hours. Based on insights from this simulation, a second major calculation was done with 8 of the 10 code words from a different code set derived from the same OOC, {64,3,1}.

For part 2, discussed elsewhere in this report, the calculation is not at all tedious.

The results of these partial and complete simulations can be summarized as follows:

1. The goal of a bit error rate of 0.001 is achievable unless the power level of the interferer greatly exceeds that of the desired signal.

2. The OOC {64,4,2} has the advantage of more code words in each code set (than {64,3,1}). This code word diversity (typically 100+ code words in each code set) is inherently advantageous, since it dilutes the greater interference made possible by the greater cross-correlation (2 rather than 1). However, the dilution was not sufficient, with a worse final bit-error rate.

3. Without doing a simulation, we could not make a convincing theoretical case that code words longer than 64 chips were a net gain. (There is a bandwidth penalty.) Since the complete simulation was infeasible (without further simplifying insights), we saw no point in pursuing this line of investigation, however interesting.

4. We found two rules for weeding out interference-prone code words:

   a. Code words using adjacent chips were strikingly vulnerable.

b. Code words using the greatest fraction of the total width of 64 were the most vulnerable to interference.

Neither of these rules was foreseen. Both were validated from theory after they were discovered.

The net results of the interference simulations was that it was possible to choose an OOC of {64,3,1}, a most favorable code set of 10 code words from this OOC, and a most favorable subset of 8 of the 10. The final bit error rate calculations, including the power ratio of interfering signal to desired signal, can be seen from the following graph:

4.5 Engineering Demonstrations

We have been exploring several possible demonstrations for BodyLAN. One demonstration which will make use of our test software and systems is an Engineering Demo designed to show the basic operation and performance of BodyLAN. A medical demonstration that we have been exploring, if funds permit, is a wireless Pulse Oximeter. This section summarizes them. We have also been exploring other demos and applications.

4.5.1 Engineering Demo

The goal is to demonstrate BodyLAN operation and benchmark performance. It will demonstrate attachment/detachment process, reassignment of TDMA allocation, single channel bit error rate, multi-user bit error rate, read and write operations, command and control.

The engineering demo system will be planned as an extension of benchmarking and diagnostic tools produced in the project.

The measurement consists of two test BodyLAN hubs, two test PEAs, and two interfering PEA transmitters. Test PEAs have display capability. Test hubs and test PEA will show successful attachment, detachment by displaying their state. For TDMA plan we will give full bandwidth to one test PEA, then bring other test PEA nearby and observe resharing of bandwidth, as displayed by test Hub. Single channel error rate will be computed and displayed for both directions. For multi-user bit error rate interfering PEA transmitters will be used to provide background interference. Test Hub and PEA will display bit error rates or any problems in the channel.

While the hub has a PC or PDA at its disposal to run diagnostic software, the PEA does not. We will use the transducer controller module for this demo. This will serve to run diagnostics microcode in a simple fashion. The transducer will also have outputs, so it could be attached to a PDA or PC. To the extent that diagnostic code for PEA and Hub are similar, loading Hub diagnostic code on a PDA attached to the PEA is a possible extension of the PEA diagnostic system.

4.5.2 Pulse Oximeter Demo

The goal is to demonstrate medical sensor. Will demonstrate stream read operation from hand held medical PEA (Pulse Oximeter). This is one of the possible medical demos we are considering. We will eventually choose the most cost effective demo. This demo is included here to illustrate a possible BodyLAN application.

The demo would consist of connecting a Pulse Oximeter to a person and displaying the measurements being taken. The sensor monitors pulse rate and oxygen content. We will pass the data stream to a computer or to a printer for display. This demo can run for a few minutes.

The Pulse Oximeter is a two part device that monitors pulse rate and blood oxygen level. A small device (in finger or ear) periodically reads pulse rate or oxygen level and sends through a wire to an Oximeter unit. The unit can display rate and oxygen content on its LED displays. It also accumulates several bytes of information from the sensor, appends a header and timestamp and can print this block out to a printer. The sensor is very lightweight and the Oximeter is a hand held, 10 oz device that can be connected to a printer.

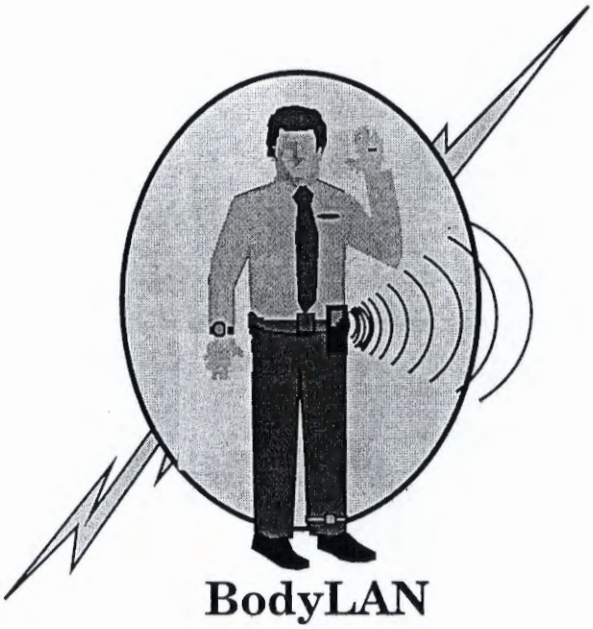
We plan to send the Oximeter output to a PDA for display. The output is ASCII 9600 baud data of known format. The PDA (or PC) will print the data on its screen. The approach proposed is essentially that of Pathfinder and hence we expect code and design reuse.

The Oximeter unit has all the buttons necessary to turn it on, off, print out or any other function. The application software developed must enable the stream read mode from the PEA (Oximeter) and be able to parse the Oximeter data. The PDA itself does no sensor data processing. All sensor data processing is contained within the Oximeter unit.

Using BodyLAN to send data from the sensor to the Oximeter is more in keeping with the spirit of BodyLAN. However, this approach for the prototype is unappealing because we would need to attach the hub to the Oximeter, which is not a generic computing device, and because (at this moment) we do not know the nature of the Sensor to Oximeter signals. Such issues would increase risk and development time.

BodyLAN

A Wireless, Body-Local Area Network



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Technical Report Feb 1 - July 31, 1995

Prepared For:

Advanced Research Projects Agency
Electronic Systems Technology Office
Contract No. DABT63-94-C-0017

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1. PROJECT OVERVIEW

In the past six months, the BodyLAN project team has made considerable progress in both hardware prototype development and link-layer protocol design. We have also simplified the hardware and the signaling architecture of the network to make it more power efficient and easy to implement.

1.1 Technical Progress

1.1.1 Hardware Prototypes

- The most important hardware decision was to use a set of *three* mini-circuit boards to implement both the Hub and individual PEAs. Due to high component count, limited board space and short development time, we implemented both the Hub and each PEA as *two-board* modules using a common radio transceiver board and a distinct digital controller board.
- We also used MC68356, a low-power / high-MIP / PCMCIA-compatible microprocessor, as the Hub controller. This choice greatly simplifies software development efforts on the Hub and enhances its performance. The built-in PCMCIA interface and versatile communication processor reduced the need of on-board logic.
- A Microchip PIC16C64 micro-controller was used on the PEA controller board to give us lowest energy consumption per instruction.
- Following our original plan, we started a collaboration with MIT to develop a low-power VLSI implementation of PEA circuitry, especially the receiver and the associated logic. A power consumption level of 10 - 12 micro-watt was extrapolated based on the conceived design.

1.1.2 Link-Layer Protocol

In software development, we have focused our efforts on the design of the link-layer protocol. We continue to support memory-mapped PEA abstraction on the Hub, and both block and stream data transfers without re-transmission over the wireless network. Furthermore, in order to ensure the protocol to be implementable on PEAs with limited computing power and brief active periods, we built the Hub-PEA communication upon *three* simple mechanisms: a two-way block transfer mechanism, a PEA state reporting method and a Hub command dispatching scheme.

- *Block data transfer mechanism.* A block transfer of preset length is the basic data transfer over the BodyLAN. It can be used in both the user and the processor channels to move application data, device memory / register contents and control information. Both the PEA abstraction and the application data datagram service are supported using this mechanism. A stream transfer mechanism is also implemented in the user channels to provide virtual circuit service.

- *Hashed state reporting.* In order to maintain close match between the PEA abstraction on the Hub and the actual device state, we send periodically to the Hub a hashed value of all software accessible registers of each PEA. This "state summary" will then be compared with a similar hashed value of the PEA abstraction. Any mismatch between the two state summaries indicates that one copy of device state is out of date, and thus a state update must be initiated.

- *Hub initiated command dispatch.* All commands of BodyLAN are issued by the Hub, which functions as the network master. The commands are sent with address first over a special command and control channel similar to the commands on a serial bus such as I^2C. The command dispatch can be acknowledged or unacknowledged. In the unacknowledged case, the network relies on the PEA state reporting method to maintain state consistency, and regards the data channels as lossy.

unacknowledged case, the network relies on the PEA state reporting method to maintain state consistency, and regards the data channels as lossy.

1.1.3 Network Architecture

In order to simplify hardware design and network operation, we have made the following changes to the basic design of BodyLAN:

- *Common up/down frequency and half duplex channels.* In order to use the same radio transceiver circuit on both Hub and PEAs, we decided to use the same carrier frequency for both up and down links and symmetric half-duplex communication between the Hub and the PEAs. This, however, will cut the data throughout of the Hub by half comparing with the original design.
- *Multi-symbol TDMA pulse.* In order to reduce the power overhead in switching the transceiver on and off between TDMA pulses, we decided to use *four-symbol pulses* on the TDMA channel. This new signaling format however may slightly increase average bit error rate under peer network interference.
- *Nibble-based data format.* Along with the use of four-symbol TDMA signals, we decided to use four-bit nibbles as the basic data transfer unit. This will decrease the data clock rate by four and further reduce power consumption.
- *User and processor data channels.* In order to build both network control and communication service upon the same data transfer mechanism, we incorporated a pair of processor data channels and a pair of user data channels in each PEA. The user data channels supports communication between user application and PEA modem ports while the processor data channels allows data movements between any part of PEA processor memory and the Hub device abstraction. Hence, the processor data channels provide the communication medium for device monitoring and control.

1.2 Progress Summary

The following lists summarize the tasks accomplished in the areas of *hardware development, software design* and *signaling scheme* between the months of January and June 1995.

Hardware

- Fabrication of integrated radio transceiver module
- Test of transmitter circuit
- Design of Hub and PEA digital controller modules
- Circuit simulation of Hub and PEA digital controller modules
- Revision of PEA interface specification
- Production of PEA programming specification

Software

- Specification of block and stream data transfer mechanisms
- Revision of PEA device abstraction
- Revision of PEA modem interface

Spread Spectrum Signal

- Revision of TDMA signal format
- Specification of TDMA signaling micro-codes

1.3 Future Milestones

We have delayed software development until the simplification design changes described are implemented. The proposal revised Milestone schedule reflects this approach.

- PDA software test
- Hub/PEA link test
- BodyLAN Prototype

----------End of September----------

- Performance benchmarking
- BodyLAN demonstration
- Final report

----------End of December----------

2. HARDWARE

A simulated design has been completed for both the HUB modem (implemented on a PCMCIA card) and Personal Electronic Accessory (PEA) modem. These designs include digital control chips, Transmitter/Receiver RF sections, and all ancillary circuits such as VCXO, power supplies, and frequency measurement circuits. All non-digital modem sections have been implemented in a prototype card and have been partially tested. The planned Transducer Controller Module development has been dropped.

Due to component count and board space considerations, both the Hub and PEA modems are implemented as two board sets. Each set consists of a mother board (unique for the Hub and PEA) and a common daughter board. All three boards will be described in detail in the following sections. The Hub modem will conform to the PCMCIA Type III mechanical specification.

The Transducer Controller Module (TCM), introduced in the last Technical Report as a mechanism for separating the evaluation testing and early application demos from the PEA modem development has been abandoned. The plan called for contracting the TCM development to an outside consultant. Only one bid was submitted. It was judged too eostly compared with projected project benefits. Accordingly, the plan has been changed to integrate the testing functionality into the PEA microprocessor.

A 3" x 4" board, containing all non-digital modem sections, was fabricated and tested during the reporting period. This board contains the power supplies, voltage controller crystal oscillator, varector, capacitor charge pumps, transmitter and receiver section, duration controller, and frequency measurement circuits. A single control EPLD was also incorporated to activate and test the various RF and analog sections. Understanding the discrepancies between simulations and prototypes was the primary goal. Of special interest was operation during the transition region between power-off and power on. There were significant discrepancies between measured and simulated operation. These discrepancies are discussed in subsequent sections. To summarize, parasitic board capacitance was much larger than expected, power losses were about a factor of two higher than anticipated, and behavior of several new low power off-the-shelf components was different than expected.

While the measured power consumption of the analog and RF circuits was higher than expected, it does demonstrate nano-joule per bit operation. Power consumption of the digital sections, however, was a factor of 2000 larger than acceptable using the Field Programmable Logic Devices (FPLD). To determine the feasibility of designing the digital sections at power consumption 2000 times less than state-of-the-art FPLD, we have contracted a CMOS chip development study at MIT. The chip replaces the FPLD and SRAM chips in the PEA modem. This development is being supervised by Anantha Chandrakasan, a leading expert on low-power IC design. Several novel techniques had to be developed to reduce power consumption in very low duty cycle synchronous FSMs employing high frequency clocks.

A programming reference manual was also produced during the reporting period for both the Hub and PEA modems. These documents, together with the detailed functional specifications completed in the last reporting period, will form the detailed information structure needed to program the microprocessors on each modem.

2.1 PEA Device

A block diagram of the PEA Modem is shown in figure 2.1a The PEA modem has the following components:

* a Microchip PIC16C64 8-bit microprocessor
* 64KB SRAM memory of which only 2KB are used
* a PEA controller implemented with an Actel 1280XL EPLD
* transmitter and receiver
* voltage controlled crystal oscillator
* duration controller
* power supplies

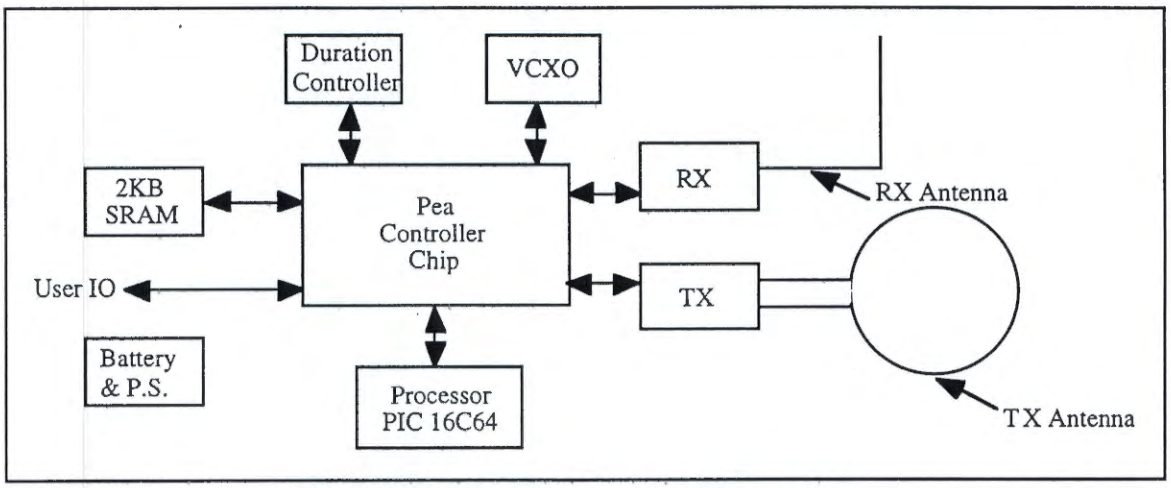


Figure 2.1a Block diagram of PEA modem

Since only off-the-shelf components are employed in the prototype PEA modem, and we want to have some commonality with the Hub modem, we have partitioned the PEA modem design into a mother/daughter board pair. The daughter board design, containing all receiver components, is also used in the Hub modem. The mother board contains all other non-receiver components including the digital control chips. One of the primary design goals were to make the transition to final product straightforward. In our model, the final PEA modem design would include a single CMOS chip integrating all digital, analog and RF sections together with a handful of discrete components (e.g., crystal, inductors, bypass capacitors).

2.1.1 Digital Section

Except for the power supply, all PEA modem sections are controlled by the micro-processor/controller chip combination in two major modes of operation. In the pre-synchronized mode of operation, the PEA periodically (i.e. once every eight seconds) enables its receiver and searches for a particular sequence of FM modulated RF bursts called Beacons. These beacon have inter-burst intervals common to all BodyLANs but an FM modulation sequence quasi-unique to each BodyLAN. A sequence of eight Beacons, having inter-beacon intervals unique to each BodyLAN, is repeated once each 32 msec frame. If the correct sequence of beacons is found, the PEA adjusts its VCXO to frequency lock to the synchronization beacons. After synchronization, the PEA then enters the synchronized mode of operation whereby it executes a sequence of instructions corresponding to a TDMA plan unique to the particular BodyLAN.

In the pre-synchronized mode, the micro-processor is the master. That is, it issues commands to the controller chip to execute low level functions (e.g., activate a Rx local oscillator varector charge pump cycle). After a process is completed, the micro-processor shuts down its clock to conserve power and selects a group of events to cause a later wake-up. In the synchronized mode, the controller is the master. It executes instructions (stored in the SRAM) at specified times within the TDMA frame. For most instructions, the controller wakes up the processor and causes it to execute some function. For example, after

assembling a nibble of Command and Control Channel data, the controller wakes up the micro-processor and indicates that it is to process the data.

A block diagram of the FPLD controller chip is shown in figure 2.1.1a. Major sections include:

* clock distribution
* frame counter
* micro-processor interface
* digital matched filter to detect beacons
* SRAM interface
* RF interface
* charge pump controller
* micro-processor wake-up FSM
* TDMA instruction execution FSM

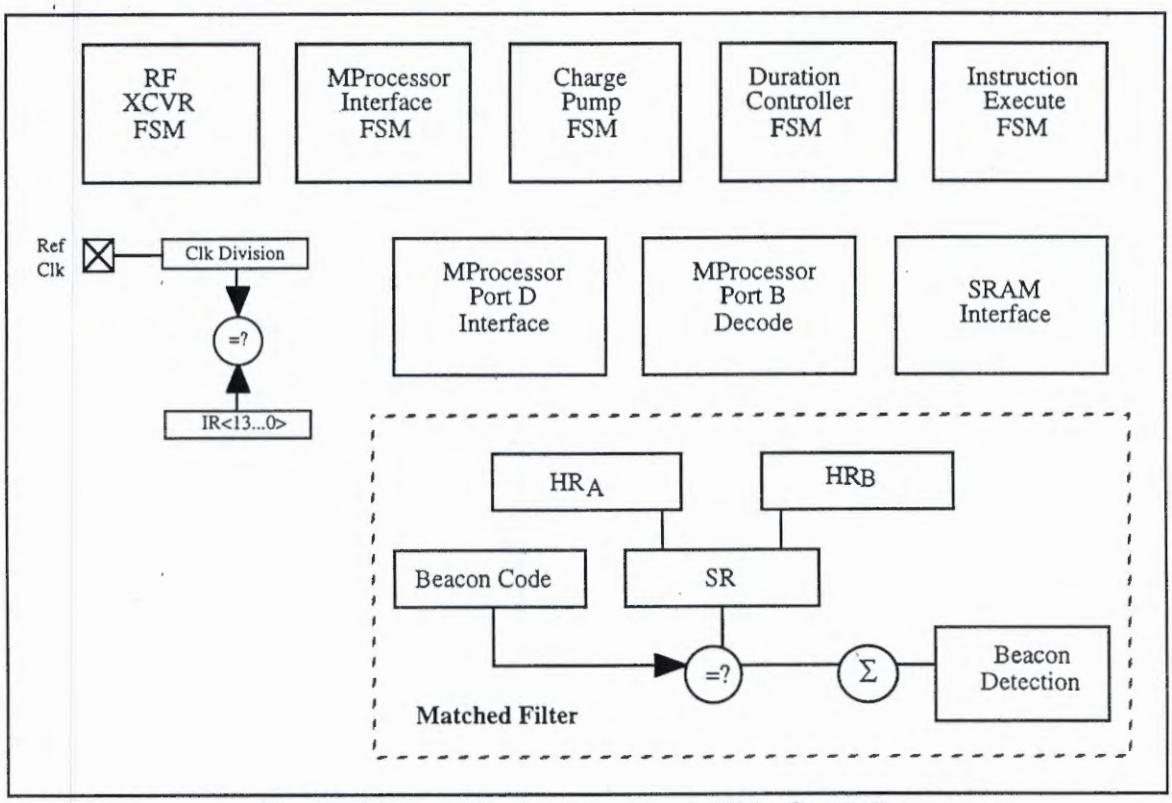


Figure 2.1.1a : Block diagram of PEA Controller

A 4.0000 MHz 800mv sine wave, sourced from the VCXO, drives 16 finite state machines plus several ripple counters. There are 48 equivalent un-gated clock loads and over 200 gated clock loads. Power consumption in the clock distribution network and just the un-gated clock is 15 milli-watts. Total power consumption of the controller chip is estimated at 20 milli-watts.

In the digital matched filter, received data is over-sampled and stored in the SRAM. Matched filter processing occurs a nibble at a time by transferring eight sets of 7 samples into 56-bit holding registers. There are two holding registers one for each of the over-sampled sets. Matching occurs by selecting successive 32-bit subsets of the holding register and counting the number of comparisons with the beacon code word. The output is a number ranging from 0-31. We currently allow three bit errors in a beacon match. Thus 0-3 is decoded as a beacon match "zero" while 28-31 is decoded as a beacon match "one".

2.1.2 **Voltage Controlled Oscillator**

PEA functionality is center around the Voltage Controlled Crystal Oscillator (VCXO). The entire BodyLAN architecture hinges on the feasibility of constructing a low power oscillator which can be phase and frequency locked to the Hub with only occasional voltage updates. The VCXO design consists of a varector adjusted crystal oscillator, output amplifier, and varector capacitor charge pump shown below.

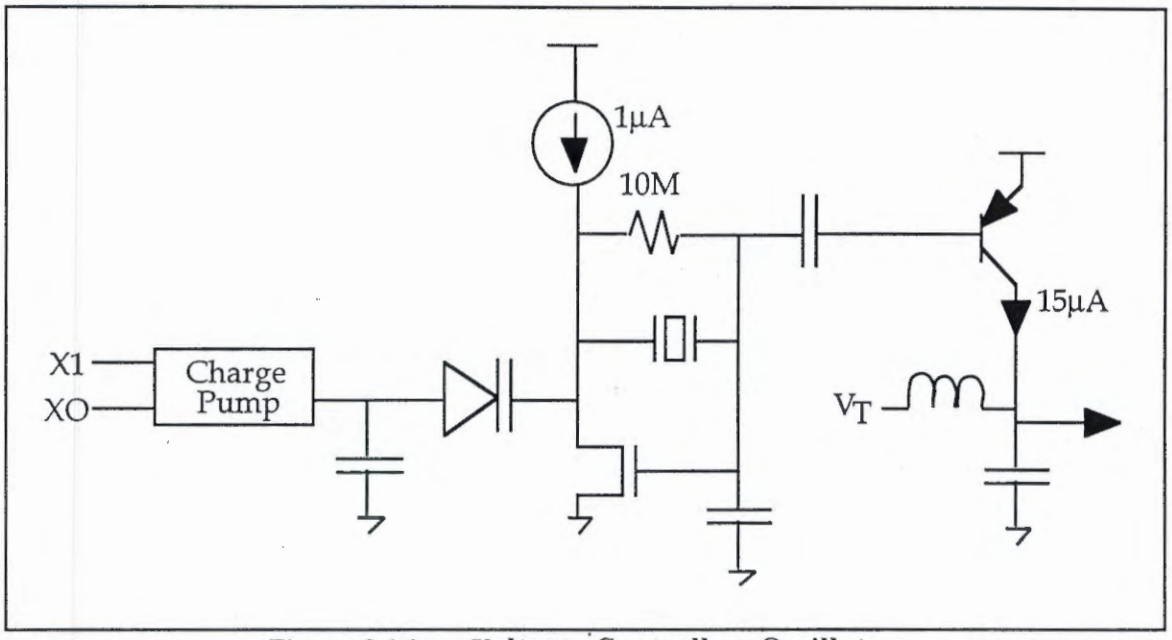


Figure 2.1.2a : Voltage Controller Oscillator

Charge is pumped onto the control capacitor by pulsing xc1 and then xc0. With a three volt supply voltage, the charge pump can vary the control voltage over an eight volt range. This corresponds to a 50 ppm frequency difference. The advantage of the charge pump scheme over conventional linear amplifier approach is power consumption. Once the target voltage is reached, only an occasional pumping cycle is needed to replace the charge lost due to leakage current.

A tuned amplifier is used to both amplify the 250 milli-volt crystal oscillator output up to 1500 milli-volts and to provide a DC signal value of 1.4 volts (i.e. the TTL threshold). The tuned circuits provides a low power mechanism to drive the 16 pfd reference clock load.

2.1.3 Transmitter Section

A single transistor transmitter design integrates the function of oscillator, amplifier, tuning, and modulator as shown below.

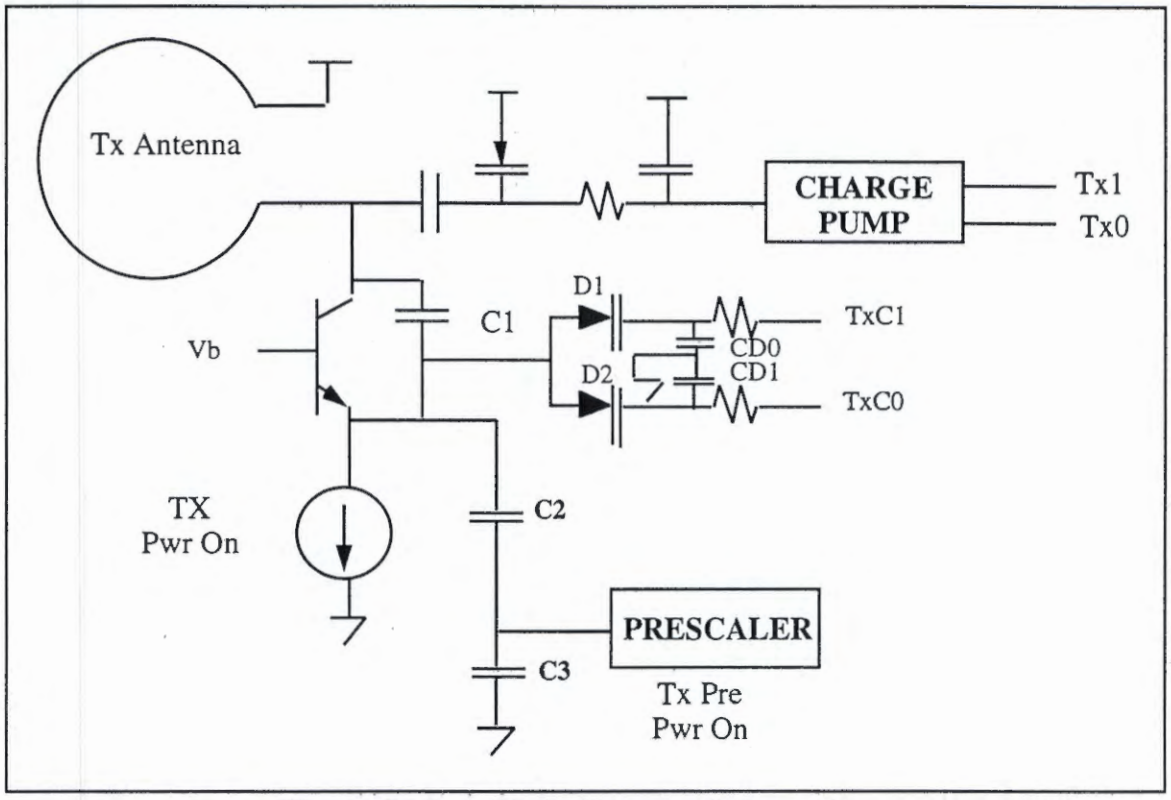


Figure 2.1.3a : Block diagram of Transmitter

The antenna is a 22 millimeter diameter loop constructed out a 0.127 x 6 x 62 millimeter piece of Brazaid strap. This material is a Ag alloy (50% Ag, 15.5% Cu, 15.5% Zn, 16% Cd, & 3% Ni), exhibits good stiffness and has reasonable RF losses. Achieving a high Q at 320 MHz is important for two reasons. First, since the majority of power dissipation in the transmitter occurs as skin effect losses in the antenna, increasing Q reduces overall power consumption. Second, a high Q reduces unwanted radiated harmonics. Measurement of the antenna gives an inductance of 38.5 nano-henry with a Q=26.5. While this Q is sufficient to achieve low power operation, we would like to see another factor to two to reduce unwanted radiated harmonics.

Varector D1 is used to adjust the transmitter's center frequency. A charge pump circuit identical to that used in the VCXO is used to adjust the varector control voltage. A 0-8 volt control capacitor swing yields a 45 MHz frequency change. This is sufficient to compensate for manufacturing tolerances but not enough to allow using the entire military aircraft band as originally planned.

Frequency modulation is implemented via varector diodes D0 & D1 and capacitors CD0 & CD1. When control voltages Tx0 & Tx1 are both low, diodes D0 and D1 are forward biased. This adds CD0 and CD1 to shunt capacitance C2 during the positive swings of the emitter voltage. When control voltages Tx0 & Tx1 are both high, diodes D0 and D1 are reverse biased thereby increasing C2 by a small amount. This circuit has demonstrated the smallest power consumption of any of the modulators explored.

During the tuning procedure, Tx0!=Tx1. A capacitor divider feeds a small fraction of the emitter voltage to pre-scaler P1. A Motorola MC12052A pre-scaler is used to both amplify and reduce the RF signal to a frequency which can be handled by the FPGA. A compariter converts the pre-scaler's ECL output swing signals to TTL signal levels. Both the pre-scaler and compariter are completely switched off except during the 16 microsecond frequency adjustment period. Measured turn-on times are less than 500 nanoseconds.

With a Peak power consumption of 2.4 milli-watts (i.e. 800 micro-amps at 3 volts), the transmitter develops a 65 milli-amp Peak-to-Peak antenna current. Antenna power consumption is estimated at 40% of power consumption. The transmitter has a conversion efficiency of 1.5 nano-joules per bit transmitted.

2.2 Receiver Board

A direct conversion receiver is implemented on a separate 1.8" x 2.4" board. This receiver board is used in both the Hub and PEA modems. In direct conversion, the RF is converted directly down to baseband without any IF. This demodulation technique reduces the number of processing stages, results in filters having the lowest pole frequencies and pole Qs, and reduces the post mixer processing stages cutoff frequency to the lowest possible, thereby reducing power consumption. The receiver block diagram is shown in figure 2.3. Major sections are:

* Local 320 MHz RF oscillator with +/- 45 degree phase shifters
* low noise amplifier
* I & Q mixers
* linear phase low pass filters
* Baseband amplifier and +/-45 degree phase shifters
* frequency discriminator and compariter

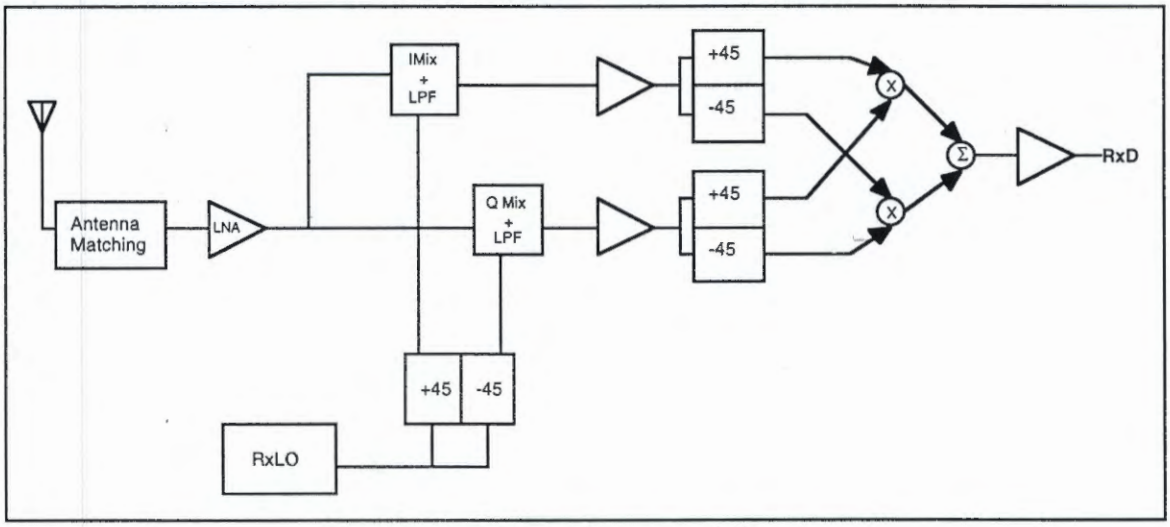


Figure 4.3 : Block diagram of Receiver

The receiver was designed to make the conversion to a CMOS chip implementation straightforward. We expect that all receiver sections except the antenna, input matching network, varector control capacitance, low noise input transistor, and local oscillator transformer will be integrated. Since we expect the receiver to have a lower conversion efficiency than the transmitter and it is typically turned on for longer periods of time, power consumption reduction is an important goal.

2.2.1 Receiver Local Oscillator

A local oscillator has been designed to source two balanced quadrature signal pairs at -2 dBm with 2.4 milli-watts power consumption and a power-up time less than 500 nanoseconds. A half circuit of the oscillator is shown in figure 4.3.1a. Low power consumption is achieved by utilizing a high Q transformer, removing the need for precise amplitude equality and 90 degree phase separation between the I & Q outputs, and employing a capacitive transformer

to directly driving the mixer inputs. The balanced I & Q LO outputs are derived from conventional +/- 45 degree all-pass RC phase shifters.

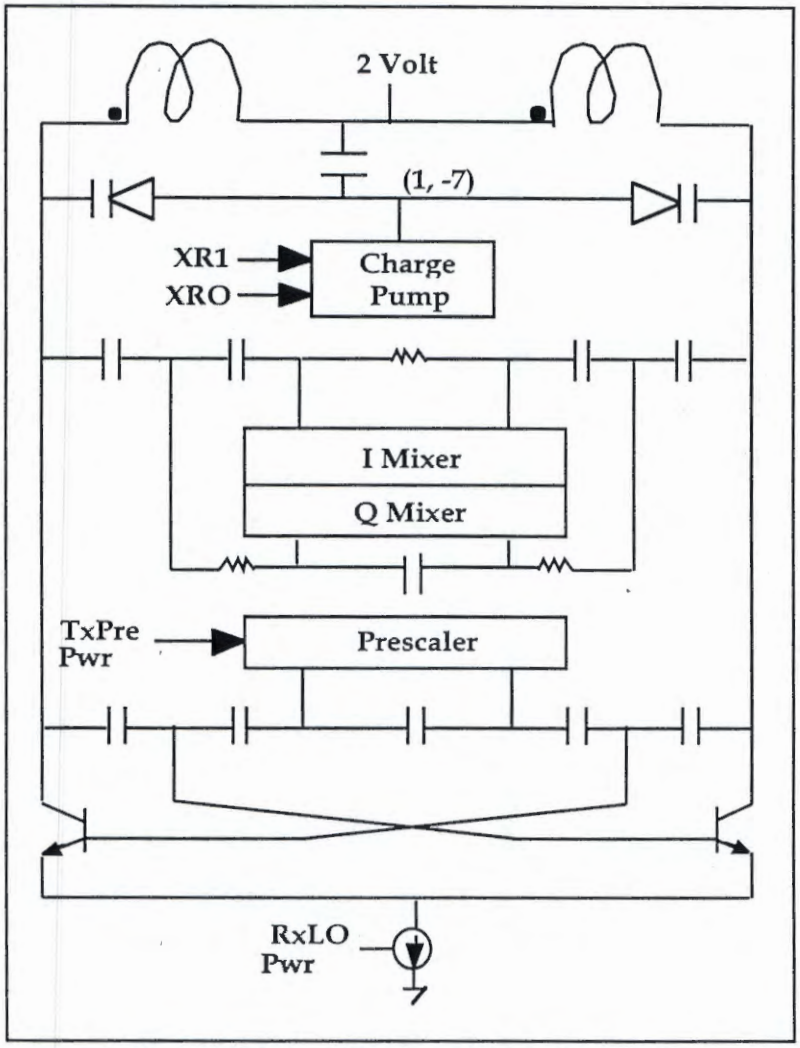


Figure 4.3.1a : Receiver Local Oscillator

The four turn transformer is realized as four 1.6 millimeter octagonal loops of 0.5 millimeter etch on the four layer PC board. Measured inductance is 40 nano-henrys with a Q of 32.

2.2.2 Frequency Discriminator

The overall purpose of the receiver is to detect if received RF power in the carrier frequency +/-1.6 MHz band is above the carrier or below the carrier. A detection scheme based on limiting I*dQ-Q*dI has excellent properties. For example, the discrimination is invariant to both amplitude and phase errors in the I & Q local oscillator signals. Simulations show invariant output with 20 to one amplitude ratios between I & Q LO mixer inputs and phase errors up to +/-85 degrees. While practical circuits will not exhibit this wide a tolerance, the contrast with conventional approaches needing +/-5% amplitude tolerances and +/-3 degrees of phase errors is apparent.

While it is easy to form I*dQ-Q*dI with ideal components, in practice, forming the derivative of I & Q is not straightforward unless a wide bandwidth differentiator is employed. A wide bandwidth differentiator consumes a comparatively large amount of power and has a small

output signal. Moreover, practical circuits delay the differentiated output causing errors in the I*dQ-Q*dI computation. To solve these problems, the proposed discriminator limits (I shifted by M degrees times Q shifted by M-90 degrees minus Q shifted by M degrees times I shifted by M-90 degrees). All pass RC circuits allow
generation of the components.

A block diagram of the discriminator is shown below. The balanced I & Q mixer outputs are first passed through an 16 dB buffered output gain block. This block also blocks out any DC. 3 dB frequencies are at 90 Khz and 1.6 Mhz. The gain block then drives an all-pass RC network generating the I & Q components shifted by 90 degrees. The shifted I & Q outputs then feed a pair of balanced Gilbert multipliers whose output currents are summed appropriately. The multipliers then feed a current mode compariter to limit the result and convert it to a single ended TTL compatible.

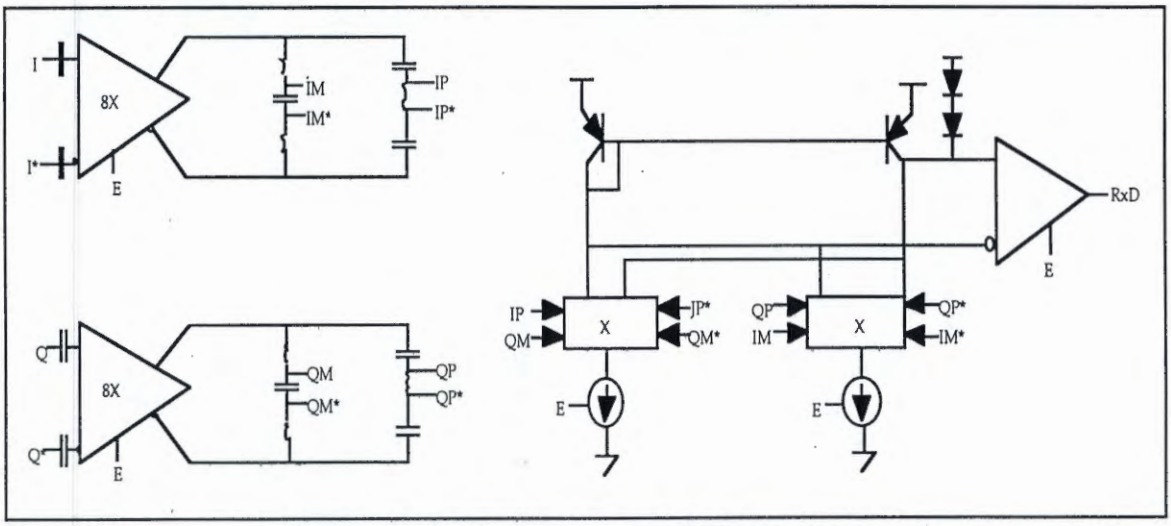


Figure 4.3.2 Block diagram of Discriminator

2.3 Hub Modem

A block diagram of the Hub Modem is shown in figure 4.4a. The modem is a PCMCIA card which plugs into a host (e.g. a personal digital assistant). It has the following components:

* a Motorola MC68PM302 processor with built-in PCMCIA interface
* 512KB flash and 256KB SRAM memory
* a Hub controller implemented with an Actel 1280XL EPLD
* transmitter and receiver
* Crystal oscillator
* Duration controller
* power supplies

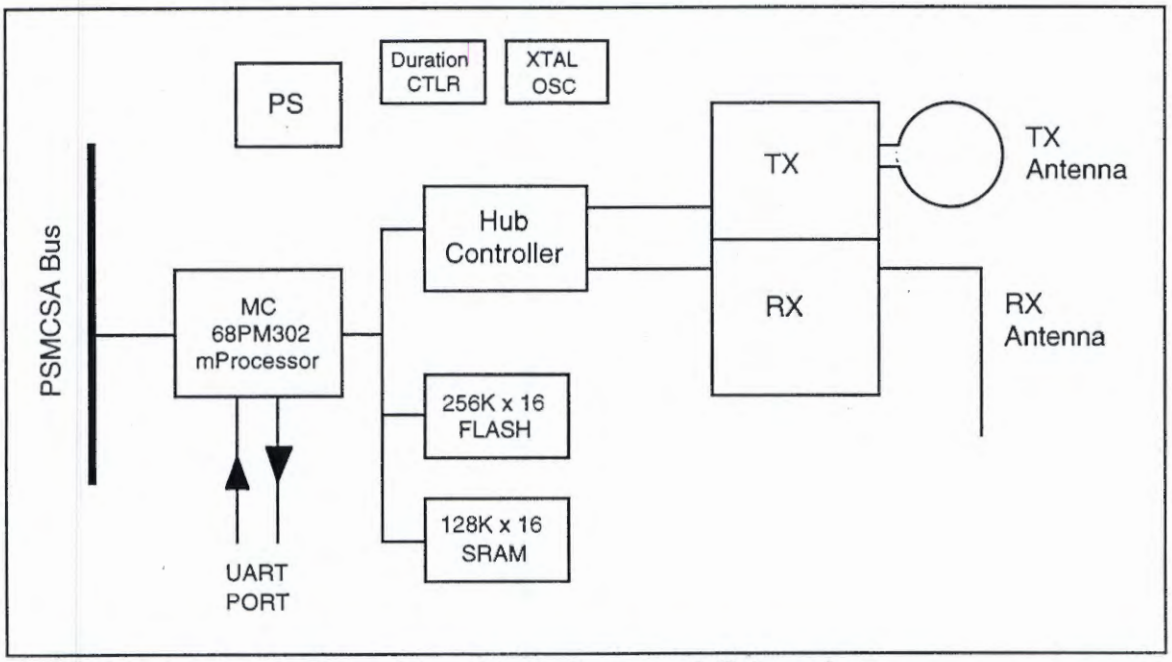


Figure 4.4a : Block diagram of Hub modem

The analog and RF sections of the Hub modem are identical to that of the PEA modem except for two differences. First, the Crystal oscillator varector, varector capacitor and charge pump have been replaced with a fixed capacitor. Secondly, to conserve board real estate, the discrete pre-scaler compariter has been replaced with two Maxim 941 compariters at a power penalty of 700 micro-watts.

Since only off-the-shelf components are employed in the prototype, component area precluded a single board implementation fitting in the PCMCIA form factor card. We have thus partitioned the design into a mother/daughter board pair with the daughter board containing all receiver components. A 10-pin connector interconnects the two boards. The Tx antenna loop is implemented in etch on the mother board while the Rx dipole in implemented in etch on the daughter card. A mechanical blowup of the ensemble is shown in figure 4.4B. It has been designed to fit within the Type III PCMCIA form factor specification. A 25 millimeter extension of the board beyond the rear edge of the PCMCIA package allows the Tx and Rx antennas to be outside the host package the PCMCIA assembly is inserted.

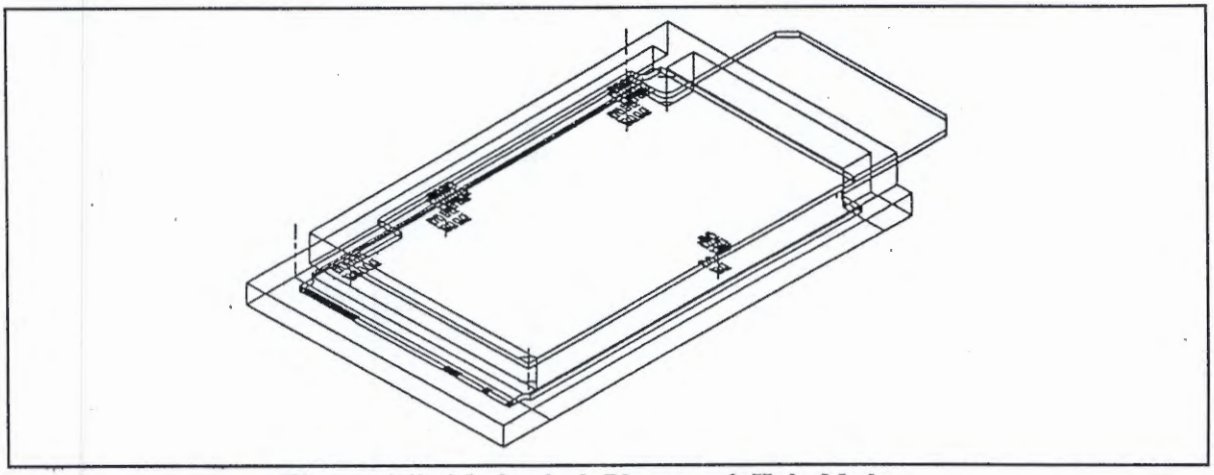


Figure 4.4b Mechanical Blowup of Hub Modem

The Hub Digital Section design was made under the following constraints:

* Components must be less than 2m thick in order to be able to design a type II package in the future with no change to the processor and controller parts

* Components should work at 3.3 volts in order to minimize power consumption. Not all parts in the prototype are actually 3-volt parts but all parts do have a manufacturer's commitment to supply such parts in the near future.

While in principle the processor of the PDA might control the Hub directly, it was decided to use an on-board processor because the interrupt latency of the PDA is unknown and encapsulating the functions will allow easier porting of the Hub to various PDAs. The Motorola MC68PM302 is utilized as the Hub processor. It implements the PCMCIA interface, it inexpensive, has a very small BGA footprint, and meets the design constraints of "thin & 3v"

The 512K byte flash memory is used for:

* the PCMCIA-required Card Information Structure, used for host-system configuration using template host drivers,
* on-board processor code
* possibly "execute-in-place" code for the host driver
* possibly non-volatile data logging
* board revision information, serial numbers, BodyLAN codes

The 256K byte SRAM (clearly much larger than needed) is used for:

* general purpose on-board processor read/write memory
* buffers for message/data transceived between the Hub and PEAs
* "instructions" for the hardware controller EPLD

An Actel 1280XL FPLD interfaces the processor to the analog and RF sections and implements all lower level digital functions. Its primary task is to execute instruction contained in the TDMA plan. Most instructions are associated with a triplet of RF bursts. The instruction indicates when each of the three bursts is to occur relative to the start of a 32 millisecond frame, the direction of transfer (i.e. Hub->PEA or PEA->Hub) and an associated SRAM location.

Transfers across the RF channel are in units of nibbles or bytes. Nibbles are redundantly encoded by replicating the nibble three times. Bytes are encoded with a four bit error correcting code. For byte errors with single-bit errors, the data is corrected and an error is logged. For 2-bit errors, an error is logged.

The controller is implemented in an Actel A1280XL-TQC (8000 equivalent gates) in a 176-pin TQFP package. This device was chosen because of our experience using Actel arrays in other projects but primarily because it generates CMOS output levels, works at 3.3 volts, and comes in a "thin" package. Using a synthesis tool, three FPLD families that were eligible under the design guidelines were considered. The design was specified in Verilog and simulated both prior to place-and-route and after (with post-annotated time delays). Some consideration to a low-power goal was given in the design. For example, clocks are gated to a section of the design only when that section is active and ripple counters are used.

2.4 PEA Controller Chip Design

While the power consumption of the analog and RF sections is much higher than could be achieved in a single chip implementation, measured power consumption is within a factor of four of our targets. Power consumption of the digital sections is off by a factor of 2000.

Since demonstrating feasibility of the BodyLAN concept hinges on an overall power budget consistent with small size battery operation, we have contracted with an MIT graduate student to design a low power version of the controller chip. Under the supervision of Anantha Chandrakasan, the student is changing the logic and architecture of the FPGA version of the controller chip and constructing a layout utilizing the MOSIS one micron CMOS foundry design rules. It is thus possible to estimate power consumption from the duty cycle, layout extracted node capacitance and clock rates. We expect to operate the 44 I/O pins at full supply voltage swings while the logic in the core circuits will run at 1.2 volts via a down converter. A preliminary layout of the 3.2 x 3.2 millimeter chip is shown in figure 2.4a. The two large components are the matched filter and SRAM.

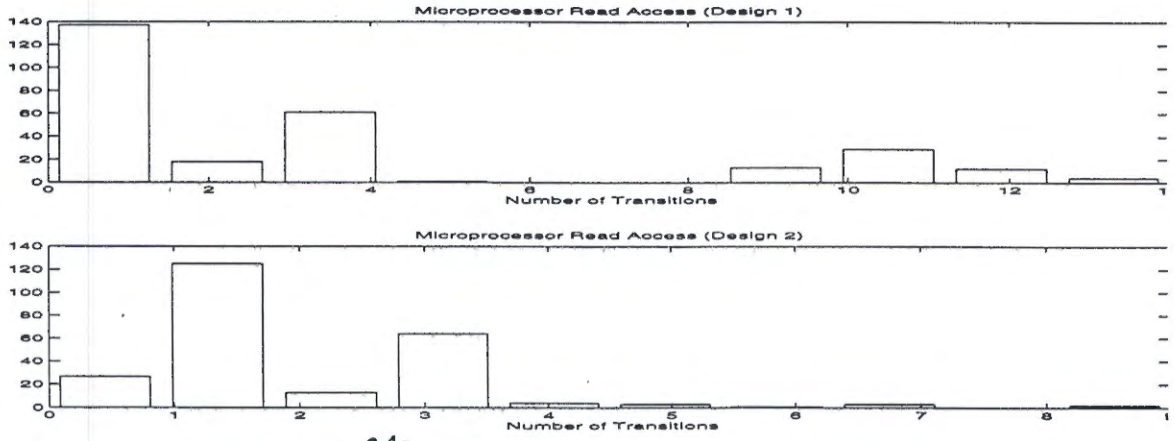


Figure 2.4a : Comparison of Number of Transitions

Table 2.4a : Comparison of Switched Capacitance

Operation	Design1	Design2	Power Reduction
up read	6.77 pF	5.28 pF	22%
up write	14.49 pF	10.38 pF	28%
TDMA	12.02 pF	I1.29 pF	6%

3. SOFTWARE

The basic BodyLAN protocols were designed to be lightweight as well as bandwidth and power efficient so that it can be implemented on simple PEA devices without requiring too much power or circuit complexity.

As shown in **Figure 3a**, the protocols provides a logical connection between the low-level communication interfaces on the Hub and individual PEA. On the Hub, the interface assumes the form of device abstraction. To the system software of PDA, every PEA appears as an I/O mapped device. The Device Driver may read/write the data buffers, access the control and status registers, and receive interrupts from these I/O mapped devices. At the PEA, the interface appears as four unidirectional modem channels, to which the User Devices are attached. Data flow through these channels according to programmed modes. The protocols support timely update of PEA device abstraction and evocation of communication action. Nonetheless, it is rudimentary in its data communication functions. Currently, we decide not to support error detection and packet re-transmission within the protocols.

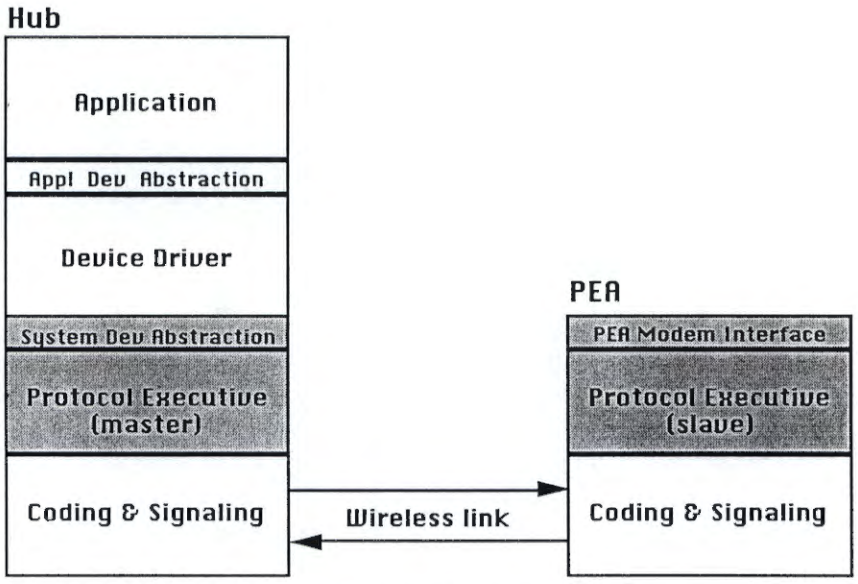


Figure 3a. BodyLAN Protocol Stack

To supplement the last report, we will focus this section on the device abstraction and the different transfer modes supported by the link layer protocol.

3.1 Device Abstraction

3.1.1 Physical Layer Device Abstraction

The RF and digital circuits in PEA and Hub were designed to provide *six* TDMA channels through the wireless link:

- *one* command and control channel — for the Hub to dispatch commands to individual PEAs and receive corresponding acknowledgments,

- *one* device state reporting channel — for the PEAs to send a summary of device state to the Hub for the detection of state change,
- *two* processor data channels — for the Hub to transfer blocks of data to or from the micro-controller memory of individual PEA,
- *two* device data channels — for the Hub to transfer discrete blocks or continuous streams of data to and from the I/O ports on individual PEA.

The communication through the channels are restricted by the hardware into the following modes:

Channel Types	*Directions*	*Transfer Modes*	*Dedicated / Shared*
Command & Control	dual	block	shared
State Report	inbound	block	shared
Processor Data	fixed single	block	dedicated
User Data	fixed single	block	shared
		stream	dedicated

Each channel consists of multiple UDIBs in every TDMA frame, and the number of UDIBs in the *four* data channels are programmable. Each UDIB carries *four* bits of data, and is specified by one of thirteen TDMA opcodes. The interpretation of UDIB contents—including the decoding of PEA ID — are performed by software.

The communication hardware of each channel contains double four-bit buffers. They will send data bits through the UDIBs once the buffers are filled and the corresponding channel is enabled. Among the six channels, the device state reporting channel and the processor data channels are always enabled once the PEA is attached to a BodyLAN.

3.1.2 Link Layer Device Abstraction

With respect to PDA system software, the BodyLAN operates as a wireless bus which can accommodate a total of 56 PEA devices. The PEA devices are mapped onto PDA memory through the PCMCIA interface.

As shown in **Figure 3.2a** each PEA occupies a *device register block* and a *device storage block*; it further consumes a number of *data buffer blocks* with each of the user and processor data channels. The blocks are indexed by a six bit PEA ID, which is assigned to the PEA during its attachment to the BodyLAN.

3.1.2.1 Device Storage Block

The device storage block contains the *operation parameters* and the *TDMA plan* of each attached PEA. The operation parameters are uploaded to the Hub during the device attachment process while the TDMA plan is prepared by the *network manager* in the Hub and then downloaded to the PEA shortly after its attachment and whenever a new plan for the device is prepared. Both transfers are conducted through the processor data channels.

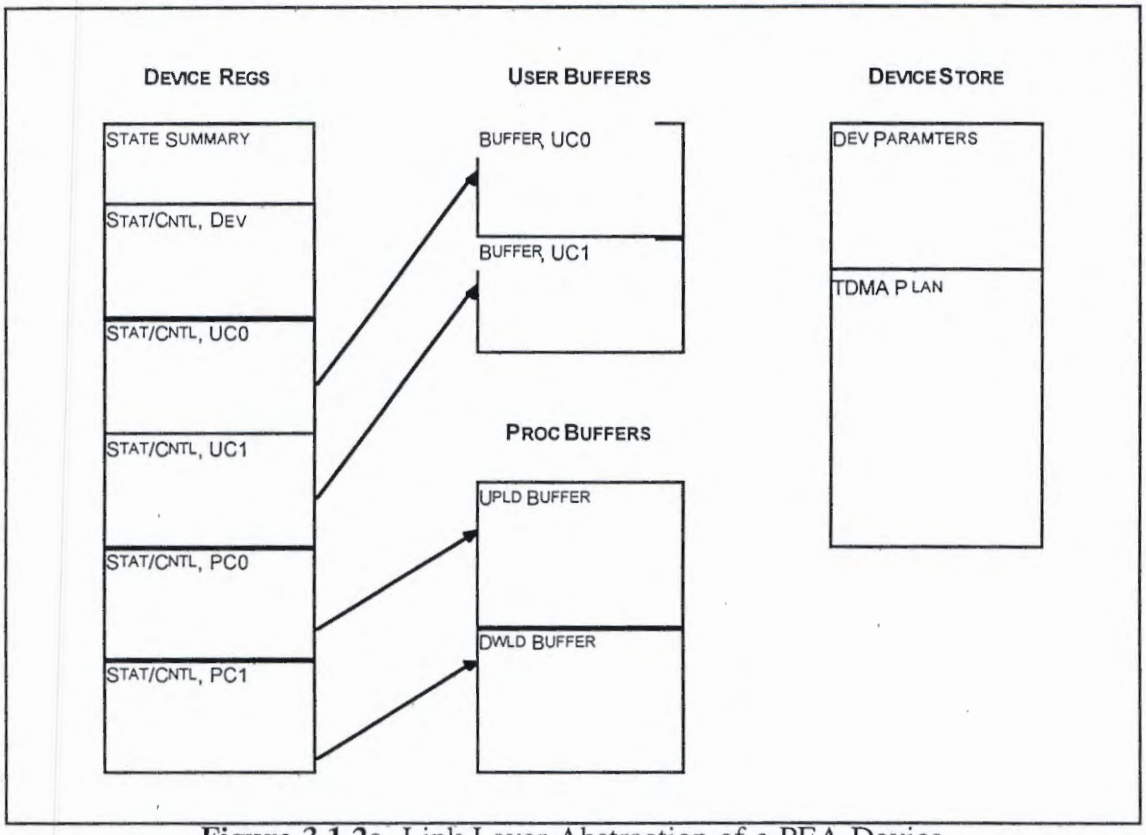


Figure 3.1.2a. Link Layer Abstraction of a PEA Device

3.1.2.2 Device Register Block

Two techniques were employed to manage the image of PEA registers in the Hub: (1) the use of a hashed value to summarize the device state for comparison and (2) the use of a block transfer to communicate the entire state of a PEA device.

The device register block of each PEA consists of *three* kinds of registers:

- *control* and *status registers*, which controls and monitors the operation of *four* data channels (*two* user and *two* processor) and the PEA device; their contents constitute the *software observable state* of the device;
- *data pointers*, which specify the address of data to be transferred via different channels, and
- a *device state-summary register,* which contains a hashed value of the current *state* of the PEA, i.e. the content of control and status registers of the device. Currently, CRC-16 is chosen to be the hashing function.

The control and status registers are also known as the *image registers* for they mirror the content of actual PEA registers. The data pointers and their associated status flags are called the *interface registers* as they are used to manage the device interface at the Hub and do not have counterparts in the PEA.

In order to provide a correct device abstraction of individual PEA at the Hub, it is important to maintain a consistency between the contents of PEA registers and their images within the Hub. The presence of device state summary provides a succinct way to detect any difference between these two pieces of information. In the order of their device IDs, every

PEA computes the hashed value of its current state and uploads it via the status reporting channel. Upon receiving the PEA's state summary, the Hub then computes the corresponding hashed value from the memory image of the PEA and compares it with the received value. Any mismatch between the two values indicates a difference between the states of the actual PEA and its image. Hence, an update of the device image is scheduled.

An update of the PEA image registers in the Hub is done by *a single block transfer* via the command and control channel. If the old and the new contents are different then an interrupt is generated and a record of the differences will be passed to the PDA.

3.1.3 Communication Buffers

Every processor and user data channel is associated with one or more *data buffers*; the user data channels are linked with *user buffers* while the processor data channels are linked with *processor buffers*. The processor data channels are also linked with the device storage and registers so that the channels can be used to transfer their contents. The organization of buffers is dictated by the modes of data transfer.

The data buffer for block transfer consists of a *single* data block, referred to directly by a pointer and a length register. In addition, there are channel REQ and RDY flags for conducting the necessary handshake to access the data buffer: PDA software shall set the REQ flag to initiate a block transfer, and may access the data buffer when the RDY flag is set.

The data buffer for stream transfer consists of a *cyclic queue* of *eight* data buffers. The first buffer is pointed by a pointer register while the insertion and removal points of the queue are indexed by queue counters. The state of the queue is further indicated by FULL and EMPTY flags.

3.2 Information Transfer

All digital communication through BodyLAN (including command and control communications) are performed in one of *three* transfer modes:

1. the *automatic or event-triggered transfer mode,*
2. the *block transfer mode,* and
3. the *stream transfer mode.*

The *automatic transfer* is used by the HUB to issue commands to the PEAs and to acquire their state summary. The *stream* and *block transfers* provide the two basic data link services of BodyLAN imitating the *connection-oriented circuits* and the *connectionless datagrams* supported by most data networks. The *block transfer* is also used to exchange control and status information such as the device parameters, the TDMA plan and the register contents over the wireless network.

All transfers except command dispatches are performed *without* explicit acknowledgment nor link-layer re-transmission. Command dispatches, however, can be conducted *with* or *without* acknowledgment by design. A simple acknowledgment and re-transmission protocol has been devised to enhance the robustness and responsiveness of the network although the first prototype only implements the simple protocol without acknowledgment.

3.2.1 Automatic Transfers

The *automatic or event-triggered transfers* move fixed-length packets through the command and state-return channels to perform the following two functions:

- to upload current state summary of every attached PEA to the Hub in regular intervals,
- to dispatch commands to individual PEA as needs arise.

3.2.1.1 PEA State Summary Upload

A PEA attached to a BodyLAN with the identifier PEAID must transmit its PEAID and the CRC-16 checksum of its control and status register content — i.e. its state summary — through the state-reporting UDIBs when the frame number (FRAMENUM) of current frame matches with PEAID according to the following formula:

PEAID == FRAMENUM *mod* 56.

The simple communication sequence is shown in **Figure 3.2.1.1a**.

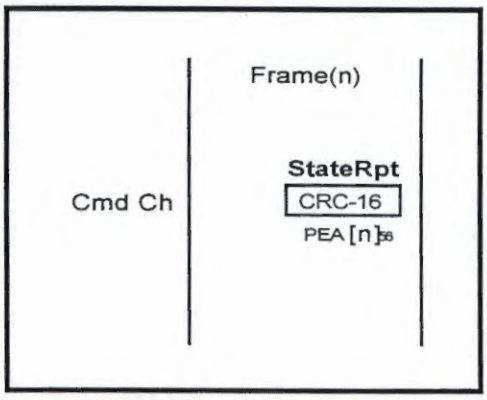


Figure 3.2.1.1a. Communication sequence for uploading the state summary of PEA(n).

The transfer serves two purposes: (1) detecting recent changes of the PEA state and (2) signaling the presence of the PEA devices. When received the PEA's state summary, the Hub will compute the CRC-16 checksum of the PEA's image registers in the Hub and compares it with the received value. Any mismatch between the two values indicates a difference between the states of the actual PEA and its image, and hence, a reloading of the device image will be scheduled. The reception of the state-summary packets also provides the necessary "keep-alive" signals for the HUB to know that the PEA still remains within the radio range of the BodyLAN. The Hub will stop all data communication with the PEA and relieve the TDMA bandwidth of the PEA if it fails to receive the packets consecutively over a preset period of time.

3.2.1.2 Hub Command Dispatch

All commands issued by the HUB are dispatched through the command and control channel (CMDCH). Only *one* command can be sent in a frame, and the dispatch can be conducted with or without acknowledgment.

3.2.1.2.1 Acknowledged Dispatch

An acknowledged command dispatch begins with the transmission of a command (CMD) packet (by the HUB) starting at the *first* UDIB of the CMDCH, and ends with the reception of an acknowledgment (ACK) packet (from the addressed PEA) before the end of the frame. The CMD and the ACK packets are separated by a preset *acknowledgment delay*, and the TDMA bandwidth of CMDCH lies within the delay is unused. This scheme requires both the HUB and the PEAs to change their communication directions between UDIBS.

Both the CMD packet format and the operation sequence are designed to *save power* during command reception at the PEAs. The acknowledgment (ACK) packet, on the other hand, is designed to conserve TDMA bandwidth and be robust against communication errors. No NAK packet is used in the communication: A PEA returns an ACK when it has received and decoded a CMD packet correctly; and simply refrains from replying in an erroneous case.

The HUB regards only the reception of an ACK as the confirmation of a successful dispatch. Reception of any other code is treated as an indication of an unsuccessful attempt. The dispatching operation also does not permit outstanding commands. Any command which is unsuccessfully dispatched will be re-transmitted in the subsequent frame. The HUB will repeat the re-transmission process if necessary up to *three* times. After that, the HUB will dispatch an ABORT command to the addressed PEA in the next frame and cancel the dispatch.

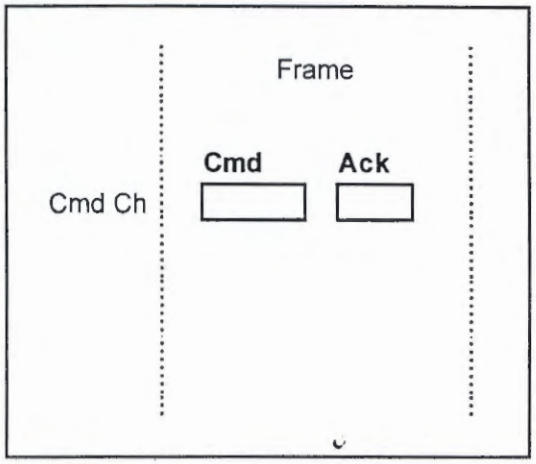


Figure 3.2.1.2.1a. Communication sequence of an acknowledged dispatch of a Hub command

The ABORT command is used to ensure that the addressed PEA is properly informed of HUB's action. After receiving a valid command packet and acknowledged the reception, a PEA will regard the dispatch of any command (valid or not) to it in subsequent frames as an instruction to abort the command previously received. The successful reception of a valid command during the operation of a previous command also aborts the operation and further initiates a new operation.

3.2.1.2.2 Unacknowledged Dispatch

An unacknowledged command dispatch is conducted in a way similar to an acknowledged dispatch. The main difference is that an unacknowledged dispatch stops after the transmission of the command packet; no reception of acknowledgment nor transmission of ABORT command will ever take place. The HUB assumes that the dispatched commands are always received successfully. The PEAs, however, ignore all the command packets that fail to pass the checksum test. Consequently, the HUB and the PEAs may *disagree* on command reception, and undertake different actions.

The correction of action is only partial and comes indirectly. The HUB, as the network master, may discover the effect of wrong device control commands by examining the state of PEA devices. On the other hand, the block transfers missed and the stream transfer data loss due to unsuccessful reception of data transfer commands can be counted as packet loss. Hence, the erroneous commands result in degradation of network throughput.

3.2.2 Block Transfer

The block transfer mode enables the HUB to send and receive a binary packet to and from an addressed PEA through *processor* or *user data channels*. The transfer is used to provide a connectionless datagram service and to exchange control and status information (including device parameters, TDMA plan and register contents) between the HUB and the PEAs. As such, it is the basic transfer mode of BodyLAN.

The transfer moves a packet of *preset length*, which may span across *multiple frames*. The transfer can only proceed in the fixed directions restricted by the hardware configuration of data channels. Duplex communication, however, can be carried out through pairwise use of the data channels.

Although the command dispatch may be acknowledged, the data transfer is always *unacknowledged* and hence, no link-layer re-transmission is performed. However, *error*

detection is implemented by including checksum fields in the data packets so that data corruption can nonetheless be detected and dealt with at a higher level.

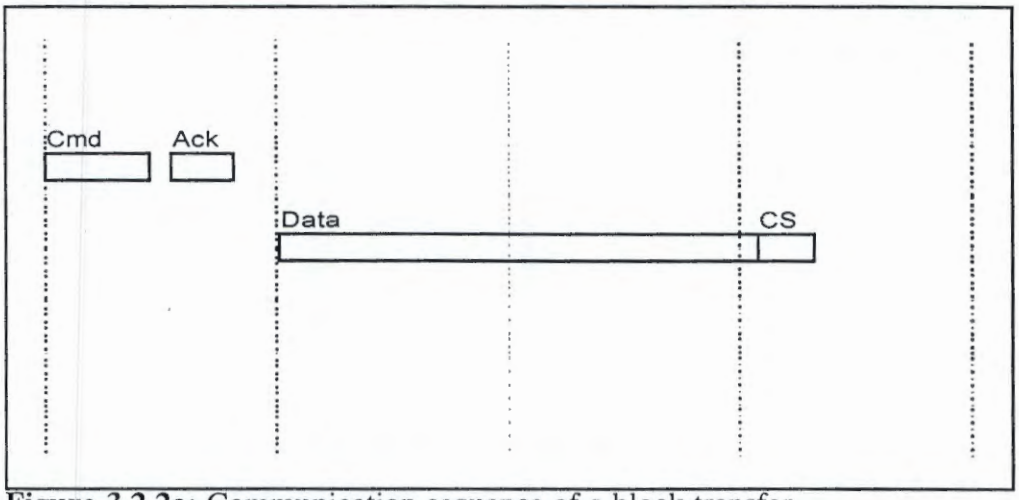


Figure 3.2.2a: Communication sequence of a block transfer

The communication sequence of a block transfer is depicted in Figure 3.2.2a. A block transfer can be considered to be made up of *two* transfers: a command dispatch and the actual data transfer. The data transfer proceed only after a successful command dispatch (while the dispatch is always successful in the unacknowledged case). Depending on the command and the data channel chosen, the data may be transferred from the HUB to the PEA(s) or from a PEA to the HUB emulating the *block read* and *write* operations. Furthermore, in order to allow complete freedom to TDMA bandwidth allocation, the transfer of data is required to occur in a separate frame *after* the command dispatch. The number of frames between the two transfers is currently set to be 1 frame.

3.2.3 Stream Transfer

The stream transfer mode enables the HUB to send and receive a continuous bit stream to and from a PEA, and is only supported by the two user data channels. The transfer establishes a data circuit between the Hub and an addressed PEA. The bit stream is not packetized; hence, the transfer does *not* support re-transmission. No error detection is incorporated, but certain stream error correction scheme may be implemented as an option. Furthermore, in order to maintain steady throughput, the transfer is conducted through dedicated TDMA bandwidth not shared by other channels.

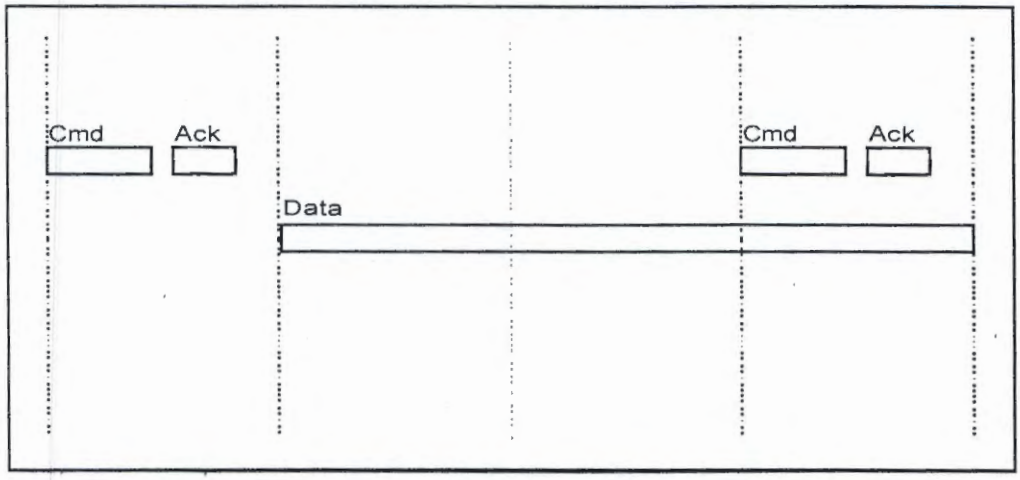


Figure 3.2.3a. Communication sequence of a stream transfer

The communication sequence of the transfer is depicted in Figure 3.2.3a. The transfer is delimited by a pair of START and STOP commands issued by the HUB: it begins in the frame after the successful reception of the START command, and ends in the frame with the successful reception of the END command. The transfer always begins and ends at frame boundaries and consumes all the TDMA blocks assigned to the channel within these frames. Due to possible faulty reception of commands, the timing of actual transfer may jitters. This may cause the fluctuation of transfer latency and more severely data loss at the two ends of the transfer.

4. SPREAD SPECTRUM SIGNALS

We have described in our last technical report [blan-tech-rprt-2], the design and performance of a TDMA signaling scheme based on Optical Orthogonal Codes (OOC). In this section, we will only supply the final conclusion of our analysis aided with graphs, and discuss the differences between the original design and the actual implementation.

4.1 Simulation Results

From the simulation of single source interference, we found three rules that summarize the effects of OOC design on the received bit error rate (BER).

1. The bit error rate increases with the rise of interfering signal power as expected; however, under moderate level of interference (with interference/signal power ratio < 3), the average BER can be maintained below .

2. The code words with adjacent active chips have notably higher BER especially under strong interference. Since the cause is generic and incorrectable, such code words should be excluded from use in the radio transmission.

3. The use of code words with shorter chip-span - i.e. spacing between first and last active chips - further lower the average BER of the signal. Hence, we also suggest to exclude the code with longest chip-span from the selected code set.

The following graphs of simulation results show the manifestation of the three rules. Fig. 1a clearly shows the increase of BER with the interference power while both Fig. 1a and Fig.

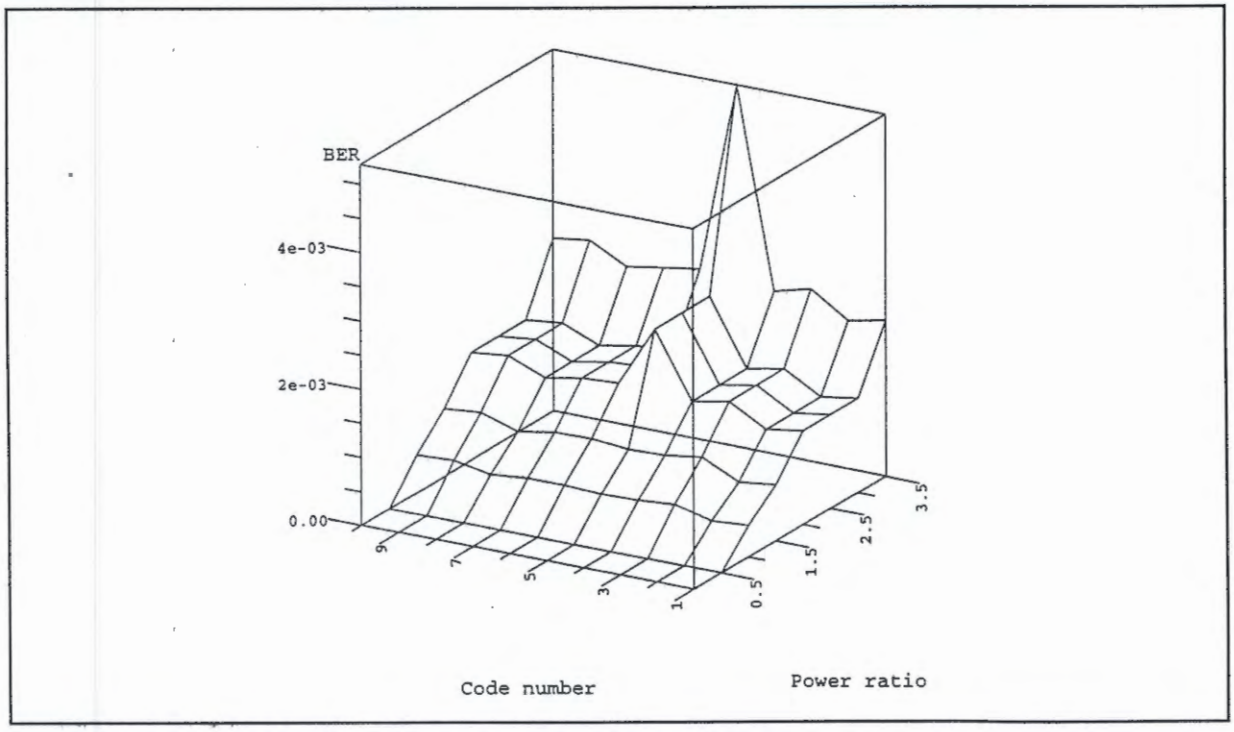


Figure 4.1-a : BER vs interferring signal power

1b show the poor performance of the code word with adjacent active chips. Fig.1b also shows the slow increase of code word BERs due to lengthening of their chip-spans.

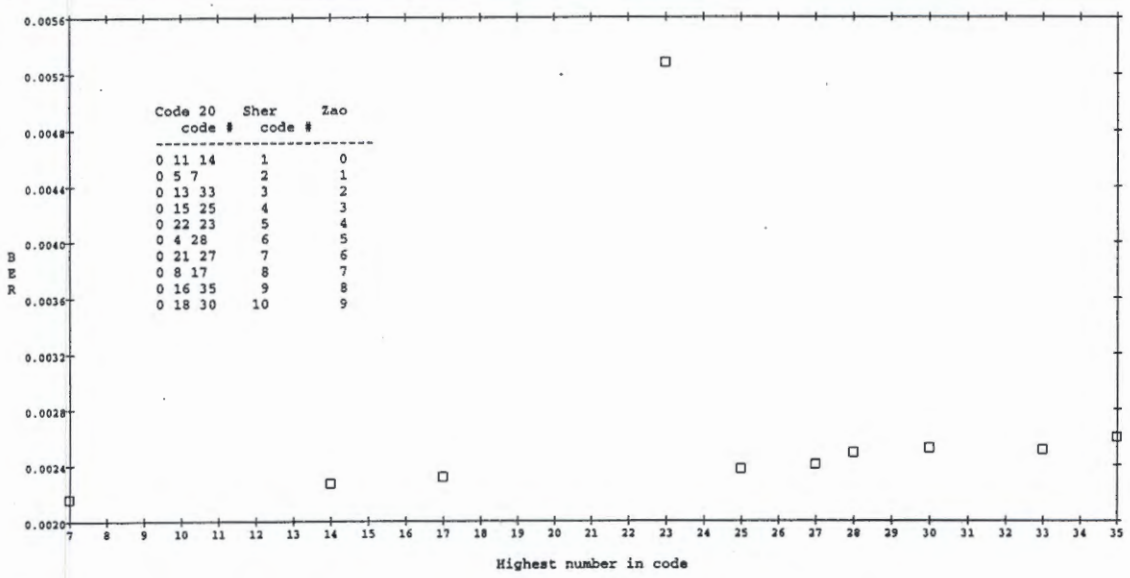


Figure 4.1-b : BER vs OOC chip spans

With knowledge of the three rules, we initiated a search for the best codes among the *five* ten-member (64,3,1) OOC sets we obtained from the first 100 runs of the greedy code generation algorithm. Code set 56 (as compared below with the original code set 20) contains the codes with shortest code-spans after removing the ones with adjacent active chips and longest code-span. Those eight codes are most suitable for data encoding while the code with adjacent chips can be used in synchronization beacons to provide timing of the chip boundary. The average BER of the eight selected codes from set 56 was plotted against that of the *ten* codes from set 20. The slower increase of BER of set 56 shows its superiority.

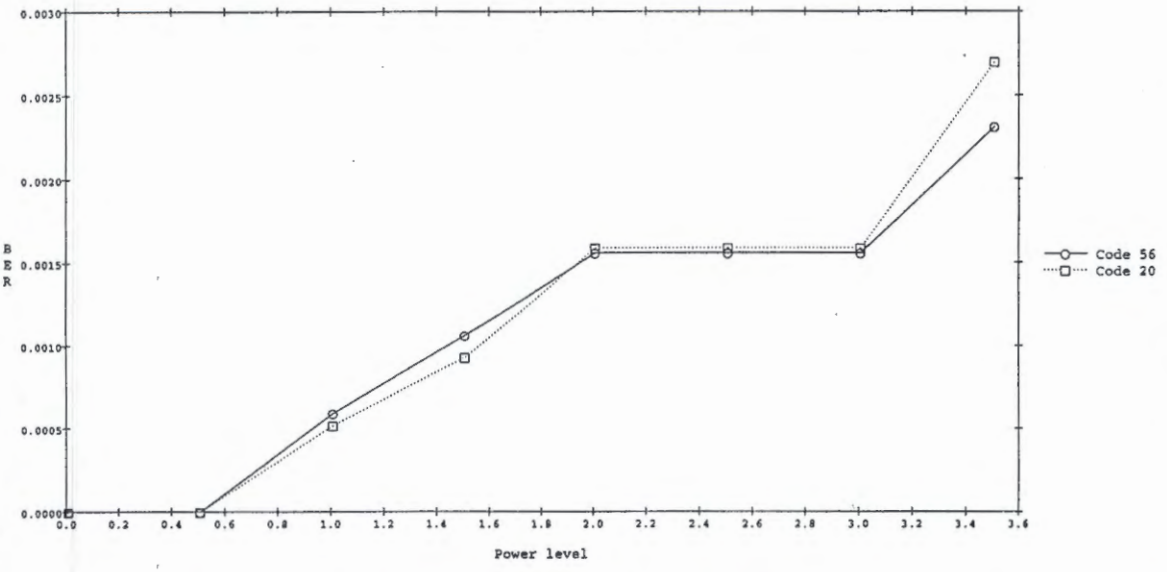


Figure 4.1-c : BER of OOC-20 and OOC-56 nnder different interference

Code Set 20	Code Set 56
0 11 14	0 10 27
0 5 7	0 19 28
0 13 33	0 2 13
0 15 25	0 4 20
0 22 23	0 5 26
0 4 28	0 24 25
0 21 27	0 30 33
0 8 17	0 8 23
0 16 35	0 12 18
0 18 30	0 7 29

TABLE 4.1a. Members of two contending OOC code sets

4.2 Implementation Decisions

We adopted a somewhat different signal design in the actual implementation of PEA and Hub hardware. Instead of sending individual data bits using the eight selected (64,3,1) OOC codes, we decided to transmit four data bits as a nipple in an multi-symbol (64,3,1) OOC format. In a multi-symbol OOC code, each chip (or symbol burst) contains four symbols corresponding to the four data bits to be sent. The chips of the code are identical, and the duplication of the symbols among the chips form a simple majority encoding of the data bits. The hardware design also allows both the starting position of the code, as well as the intervals between adjacent chips, to be programmable.

Besides the flexibility in programming the inter-chip intervals and the position of each code in a TDMA frame, this new design has two more advantages in term of hardware implementation and operation.

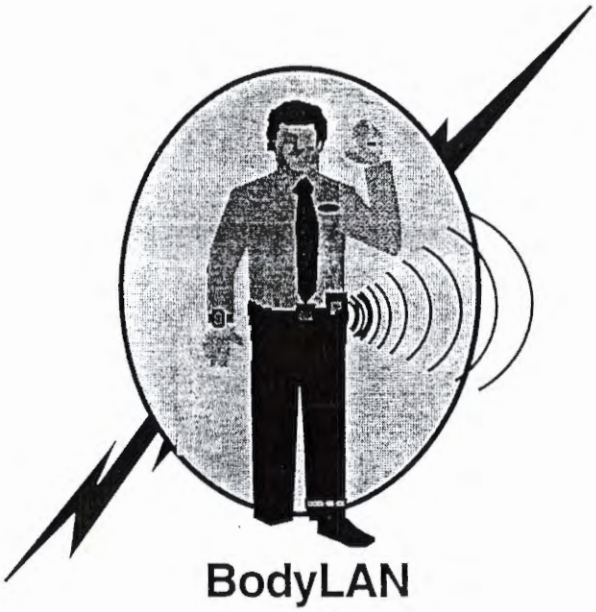
1. Data communication using multi-symbol codes are more energy efficient for the transceiver on/off time is then shared among four data symbols, and the data are transferred in nipples in a rate four times slower than the bit rate.

2. In the new design, the position, the inter-chip intervals, and the FSK symbol used to transmit the data nibbles are completely programmed by TDMA micro-codes. This greatly simplified the data encoding hardware; in particular, it eliminated the need of a random sequence generator. The compensating cost is a bigger TDMA code memory and a more sophisticated TDMA management software. Both are less costly than the design of dedicated hardware.

Nevertheless, this new signal design may cause an increase in bit error rates mainly because the interference between consecutive symbols may cause multi-symbol errors which is significant deducing from the lower performance of OOC codes with adjacent chips [Fig. *4a*][Fig. *4b*]. Furthermore, the repetition of chips or symbol bursts also reduces the randomness of the symbol stream and thus increases the chance of interference of successive symbols. We will perform performance analysis on the actual transceiver in order to determine the effect of the new signal design. If the performance degradation is significant, we can revert back to the original OOC signaling scheme by forcing the data bits within each nipple to be the same and thus effectively communicating at a quarter of the normal data rate.

BodyLAN

A Wireless, Body-Local Area Network



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Technical Report August 1 - September 30, 1995

Prepared For:

Advanced Research Projects Agency
Electronic Systems Technology Office
Contract No. DABT63-94-C-0017

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1.0 Project Overview

In the past three months, the BodyLAN project team has progressed in technology insertion, hardware prototype development, and coding protocols. We have contacted business, university, and government users who have indicated that the BodyLAN technology may allow lower risk and standardization to wireless transducer/processor interconnection. All sections of the hardware prototype have been examined except the a section of the receiver with excellent correlation with the simulations. Although uncompleted, this prototype clearly demonstrates the feasibility of low power consumption via low-duty cycle power enabling. Error performance improvements in the multi BodyLAN shared space situation were also developed.

1.1 Technology Insertion

We have actively explored inserting the BodyLAN technology in a number of application areas including non-invasive patient monitoring, personal inertial navigation, medical monitoring, sports training, baggage matching, proximity detection, and item tracking. We have spoken with: Organization Application ORNL coupling medical monitoring sensors such as a blood oximeter to a soldier's wearable computer USARIEM Real-time soldier effort sensors; Analog- devices Integrating a low power three axis accelerometer magnetomer for personal intertial navigation; Kent Display Integrating a wireless linkage to ultra low power displays, MIT Medical monitoring applications, Analogic Medical monitoring applications, BBN Personal inertial navigation and sports training. BBN management has expressed sufficient interest in persuing BodyLAN applications that BodyLAN was highlighted in its premier Web page (Appendix A). BBN is currently engaged in developing a business plan for inserting BodyLAN technology in government programs and soliciting third party relationships for product exploitation.

1.2 Hardware Prototypes

The BodyLAN hardware component has exclusively focused on testing the prototype design developed during earlier periods. No attempt has been made to improve the design. Redesigns have occurred only in those area which did not match the simulations. Hardware achievements during this period include:

- The transmitter section of the prototype has been fully tested. This includes frequency locking, FM modulation, and power enabling. Significant effort was applied in redesigning the power supplies to reduce digital/RF coupling.
- Numerous antenna materials and geometric designs were examined.
- The 4 MHz oscillator was redesigned and tested as a VCXO with a charge pump control. Frequency adjustment was 30 PPM, only 60% of the expected range. Power consumption of the prototype was 30 microwatts driving the 26 pFd of parasitic clock load.
- A new duration comparitor circuit was designed and tested giving a 4 nsec sensitivity.
- The MIT collaboration has been completed. A full custom CMOS chip layout was completed and is ready for fabrication. The 20 square mm chip was designed with one micron design rules for the MOSIS fab line. This semester, the student performing the work is completing the write-up for his MS thesis. An invited paper covering this thesis work will appear in the IEEE Circuits and Devices magazine.

1.3 Network Architecture

Network architecture activities have been limited during this reporting period due in part funding exhaustion. None of the network architecture work was project funded. Network architecture and software achievements include:
- A MicroChip PC based development system was purchased by BBN capitol funds for firmware development of the PEA microprocessor chip. Familiarization of the included tools has progressed. Some code has been generated.
- A new code sequence scheme was developed which reduces systematic errors induced by multiple BodyLANs sharing the same physical volume and frequency band.
- A new set of orthogonal codes have been developed which are more optimal. Performance of the optimal codes and the Optically Orthogonal Codes (with the new code sequencing scheme) appear similar.

1.4 Progress Summary

The following lists summarize the tasks accomplished in the areas of hardware development, and signaling scheme between the months of July and October 1995.

Hardware
- power supply redesign
- 4 MHz oscillator PLL completion
- PEA Transmitter section completion
- PEA Receiver partial completion
- Development of a receiver test board design
- Simulation and layout of a custom CMOS PEA controller chip

Software
- Purchase and setup of MicroChip development system

Spread Spectrum Signaling
- Modified encoding scheme to reduce error rate
- Development of a new class of low interference codes

1.5 Future Milestones

Since this is the last quarterly report in the original contract, the only milestone remaining is the final report. We have asked for a no-cost extension, so work can continue on remaining funds. Assuming an extension, milestones are as follows:

- Test of the receiver
- Hub/PEA link test
- Digital/RF integration demonstration
- final report

2.0 Hardware

Work during this period focused on evaluation of the 3" x 4" test board fabricated during the previous reporting period and the development of the custom CMOS PEA controller chip.

The evaluation board contains the power supplies, voltage controlled crystal oscillator, transmitter, receiver, duration controller, frequency measurement circuits, and control FPGA. Understanding the discrepancies between Spice simulations and the prototype was the primary goal. Of special interest was operation during the transition region between power-off and power-on.

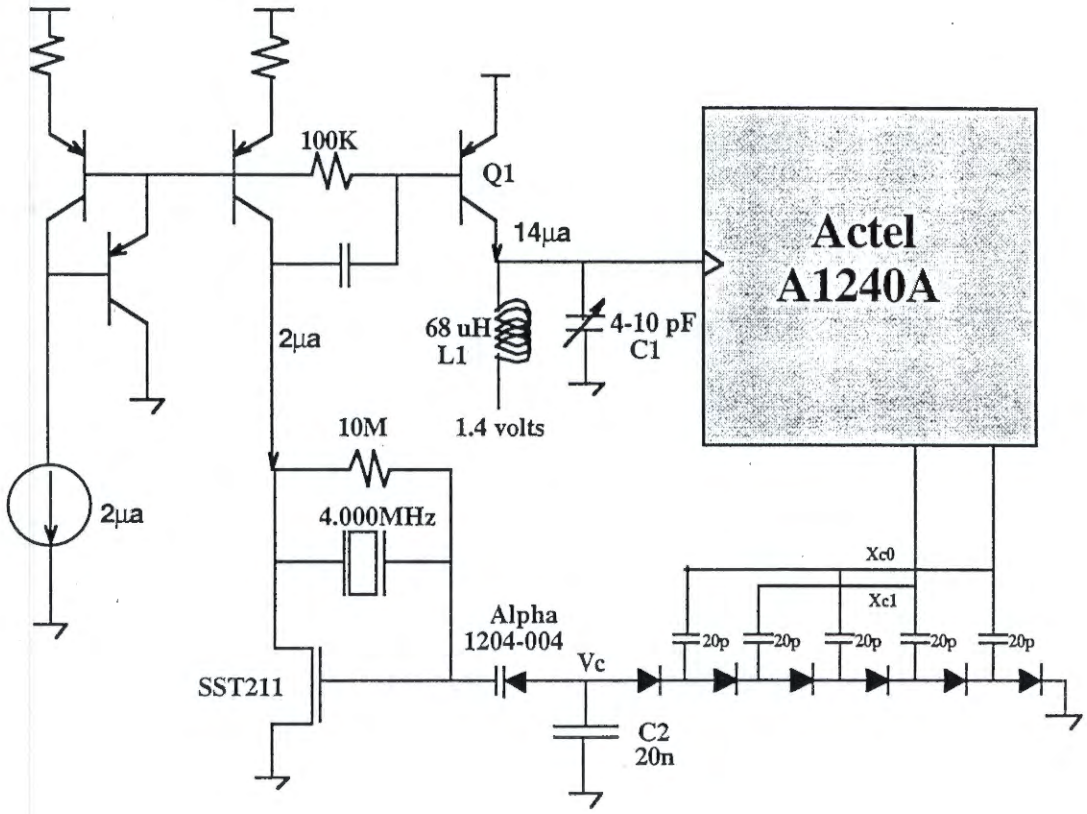
Significant simulation discrepancies were discovered in the evaluation board. These differences were due in part to incorrect modeling of both board parasitic devices used and coupling between the digital and RF sections of the prototype.

A simulated layout of the custom CMOS PEA controller chip has been completed. While much of the chip is a direct conversion of the FPGA developed for the PEA prototype, both the 4 MHz crystal interface, matched filter, and clock distribution schemes are new. New approaches were required because the discrete implementations used in the prototype have very large power consumptions not sufficiently reducible by a direct conversion to silicon.

2.1 Voltage Controlled Oscillator

The 4 MHz VCXO (shown in figure 2.1) has been fully characterized. With a control voltage variation from 0.5 to -6 volts, oscillation frequency changes by 154 Hz (i.e. +/- 19 ppm). This is factor of two smaller than expected and is caused by parasitic capacitance on the oscillator nodes. Extinction current of the oscillator was 1.35 uamps. At its nominal 2 uamp operating current, loaded output voltage was 260 millivolts peak-to-peak. Losses in the oscillator are an order of magnitude larger than expected. The tuned output amplifier, consisting of Q1, L1, and C1 with a bias current of 15 uamps was able to drive the Actel A1240A FPGA with a 3500 millivolt peak-to-peak clock sine wave clock. Parasitic loading on the clock line was estimated at 26 pfd.

Figure 2.1 Voltage Controlled Crystal Oscillator.



Varactor control voltage Vc had a measured leakage current of 9 namps. This leakage is the sum of the leakages of D0, D1, C2 and the board. Solder flux on the initial assembly was shown to have a leakage of about 135 namps. With a control capacitance C2=20nf, over a four millisecond period, voltage drift is 2 millivolts. This corresponds to a typical frequency drift of 4 psec per millisecond. Oscillator stability at constant varactor control voltage was better than 0.1 Hz over a 100 second measurement period.

Varactor voltage control is affected by repetitively pulsing Xc1 & Xc0. When only a single pulse pair is issued, there is sufficient leakage in the diode chain to discharge intermediate nodes. This results in no charge being pumped to C2. Three Xc1/Xc0 pulse sequences over 32 msec was found sufficient to drive the varactor control voltage to its most negative voltage of -6 volts.

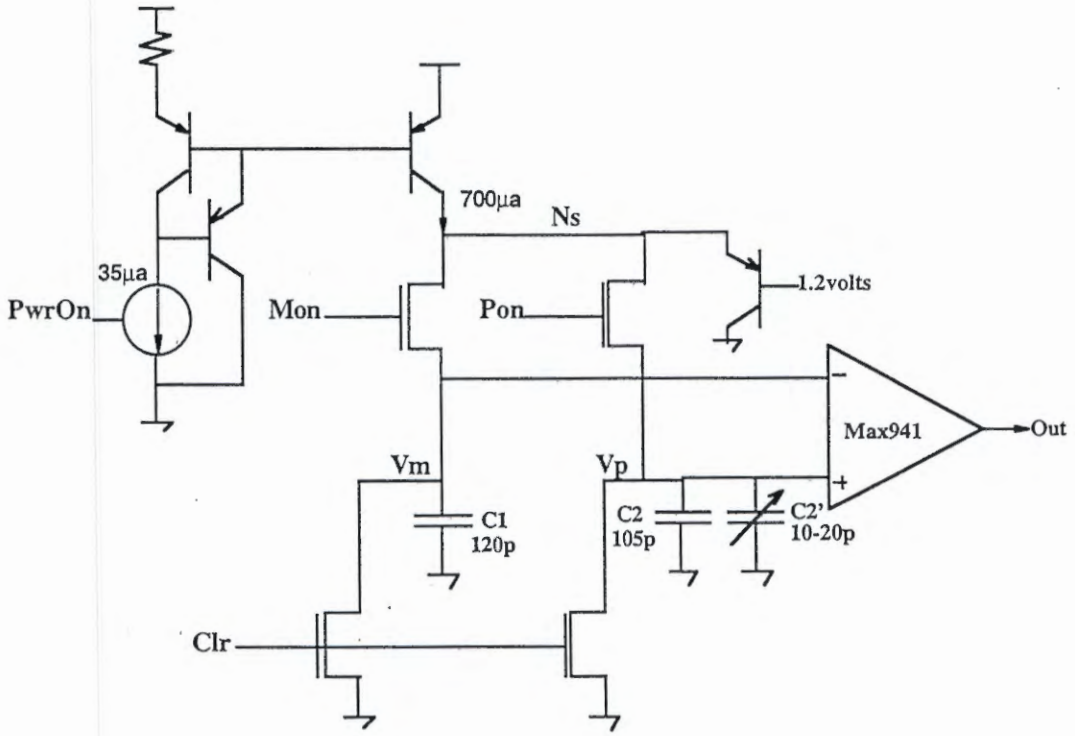
Many of the problems encountered in the protoype unit are expected to disappear in a chip implementation because of a reduction in parasitic capacitances and leakage capacitance. For example, extracted models of diodes used in a typical foundary worst case leakages of 0.5 namps.

2.2 Duration Comparison

The Duration Comparison (DC) circuit is used to determine which of two pulses, Pon and Mon is of longer duration. These pulses vary in duration from 83 nsec to 250 nsec. Frequency lock is established when the two pulses are equal. The degree to which DC is able to determine equality determines the frequency accuracy. For example, if DC is sensitive to duration differences of 1% (i.e. 2.5 nsec worst case), then the frequency can be established to one part in 6400. This would result in a worst case frequency uncertainty of +/-25 KHz. DC is enabled twice per frame, once to measure the transmitter oscillation frequency and once to measure the receiver's local oscillator frequency.

Numerous attmepts to make the prototype board circuit work were unsuccessful. Circuit failure was attributed to parasitic diodes in the quad FET pack used. A new DC Circuit was created (shown in figure 2.2).

Figure 2.2 Duration Comparitor



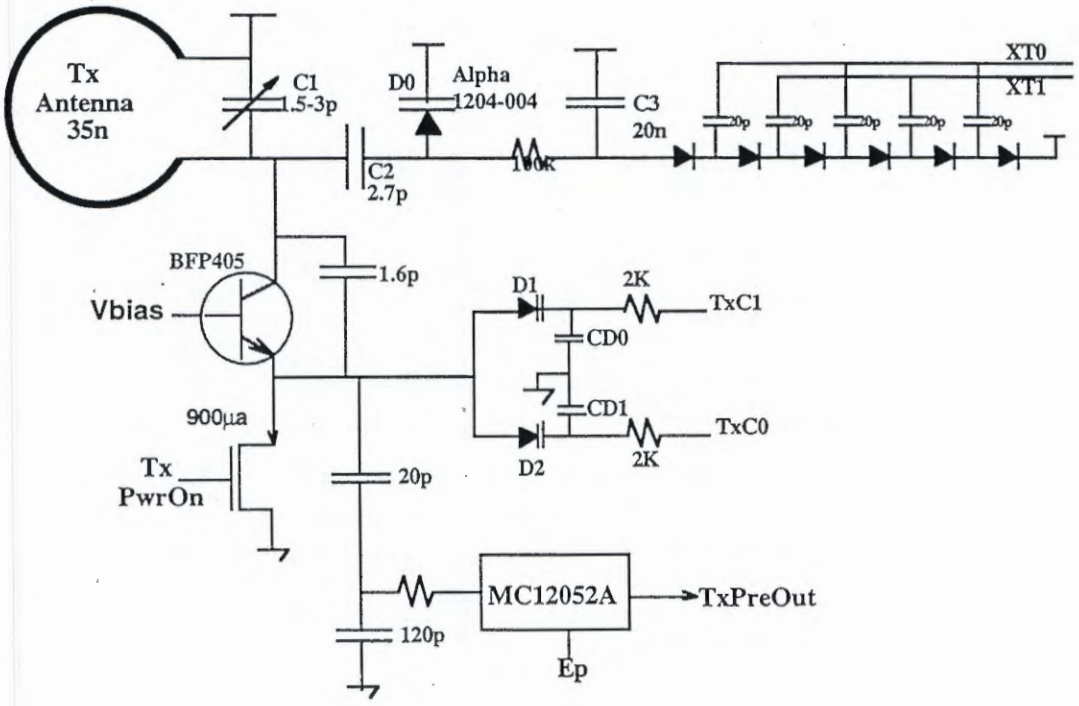
When the frequency measurement cycle is not active, CLR is asserted with both Pon and Mon negated. Nodes Vm and Vp are thus shorted to ground. In a measurement cycle, two pulses are generated. One is created from an integer number of 4 MHz clock cycles while the second is created from an integer number of Rx or Tx oscillator cycles. The second pulse is delayed from the first by an interval which varies between 83 and 250 nsec. Pon is asserted while the first pulse is asserted and the second is not. Mon is asserted while the first pulse is negated and the second pulse is asserted. When the durations of Pon and Mon are equal, the two pulses are equal. This implies that the two frequecies are interrelated as the duration count ratio times 4 MHz.

DC uses a single current source inserting about 700 uamps into node Ns. This current is steared either into ground, into node Vm or into node Vp. If capacitors C1 & C2 are equal and Pon & Mon are of equal duration, voltages Vm and Vp will be equal. With C1=C2, the MAX941's one millivolt offset voltage limits resolution to +/- 170 psec. Thus the main error contributer is the differences in between capacitors C1 & C2. To offset any differences, we adjusted variable capacitro C2' until equal Pon & Mon pulses produced a metastable comparitor output. Sensitivity of the circuit after trim is estimated at better than 2 nsec.

2.3 Transmitter

The prototype transmitter section has been fully charactrized. The design integrates the funciton of oscillator, amplifier, tuning, and modulator as shown below.

Figure 2.3 Transmitter Section



The new design reflects minor changes introduced during this reporting period. This includes a Tx Antenna tuning capacitor, charge pump referenced to Vdd instead of ground, a resistor inserted on the prescaler input, and change of the output transistor to a BFP405.

To reduce second and third order transmitted harmonics caused by the varactor, the tuning range has been reduced to 5%. With the frequency locking circut inhibited, trimmer capacitor C1 is used to trim the oscillation frequency to 312 MHz. The frequency locking process will then pump charge from node Vc (making it more negative) to tune the oscillation frequency to 320 MHz +/- 100 KHz. With this change, the transmitted second and third order harmonics are down 38 dB and 26 dB respectively.

With a 900 uamp bias current, the measured antenna voltage is 5700 millivolts peak-to-peak. This generated a -27.5 dBm signal using a 9 inch antenna into the spectrum analyzer at one meter. This signal about 18 dB larger than expected. with perfect antenna matching. While we are not unhapply with such a large radiated signal, it suggests that components in addition to the Tx Antenna are radiating. We have not isolated the source of this excess radiation.

Other shapes for antennas have been explored. Aside from adding a dipole to the loop, no shape changes of the loop at constant crossection appear to change coupled power by more than a few dB. Thus the 3 mm wide, 22 mm diameter loop will continue to be our 'standard' antenna. Adding a 22 mm dipole appears to add a few dB to the coupled signal.

Leakage at node Vc was measured at 8.5 namp. With a varactor control capacitoro C2=20 nf, Vc decays at 1.25 Khz per msec. With an average interval between charge pumping of 4 msec, we would expect Vc decay to contribute no more than 5-7 KHz of frequency spread.

With all digital circuity inhibited, the -28 dB bandwidth is 9 KHz band. The -28 dB bandwidth increases to 220 KHz when the digital circuts are enabled. Studies have shown that better supply decoupling reduce this digital/RF coupling. It is clearly caused by power supply modulation. We believe a balanced transmitter circuit will have less power supply sensitivity.

The transmitter is modulated by switching in varactor diodes D1 and D2. To transmit a low tone, TxC[1..0]=00. to transmit a high tone, TxC[1..0]=11. Capacitors Cd0 and Cd1 were selected to achieve a +/- 1.5 MHz modulation. Modulation causes less less than one dB change in radiated power. Modulation between tones is limited by the rise and fall times of the Actel 12040A controller chip to under 15 nsec.

When frequency locking was enabled in a continuous mode of operation, the frequency is not stable. Rather, it drifts over a 350 KHz band offset from 320 MHz. Both the size of the drift and size of the spread are of unknown cause. The drift is about a factor of 3.5 larger than expected. While this spread is still small compared to the 3000 Khz between tones, it was suprisingly large. We have plans to test out a balanced version of the transmitter to examine whether its reduced power supply sensitivity improves the frequency stability.

Measured Transmitter turn on time was under 120 nsec. With the continuous mode frequency instability, we have not seen cause to explore stabity under burst conditions.

The prescaler used was a Motorola MC12052A. When first powered on, the chip's output corresponded to a 1700 MHz input, reguardless of input, i.e. the chip was internally oscillating. After many blind alleys, the insertion of a 50-70 ohm resistor in series with the prescaler input close to the chip provided sufficient dampening to prevent oscillation.

2.4 Receiver

The balanced receiver local oscillator was partially characterized. Due to incorrect sizing of the transformer turn diameter, measured equivalent inductance of the four turn transformer was 120 nH. We shorted out two of turns to produce an equivalent 40 nH coil but with a much lower self resonant frequency.

With a 500 uamp bias current, a 1.250 volt differential signal was produced. turn of time of the oscillator was under 160 nsec. With all digital chips inactive, the -20 dB bandwdith was 4 Khz. Activating frequency locking and charge pumping increased the -20 dB bandwdith to 120 KHz. While this is still about a factor of four improvement over the transmitter, it is still much larger than expected.

A simple mechanism for testing the I & Q baseband circuits has been developed. It consists of injecting one tone into the I channel and another tone into the Q channel. Since the discriminator is insentive to amplitude errors, the output waveform should be a limited version of a sine wave whose frequency is the difference of the two tonse. Offset voltage sensitivity, frequency cutoff points, and saturation effects can easily be studies with two signal generators.

2.5 PEA Controller Chip

We have subcontracted the design of a custom CMOS chip to a master's student of Anantha Chandrakasan at MIT. This chip replaces the functionality of the VCXO, program SRAM, and FPGA PEA controller chip. We have named this design the PEA_C chip. While demonstrating microwatt power consumption of the RF sections using low duty cycle transmit and receive appears to be successful, the FPGA prototype showed power consumptions in the 20-40 milliwatt range.

The basic BodyLAN concept traded off power consumption in the RF sections with increased complexity in the digital control sections. Since the digital section must be 'on' all the time, feasibility of a micropower system is crucially dependent on whether the power consumption of the digital section can reduced by more than three orders of magnitude.

It is important to put the 20 microwatt target power consumption in perspective. With a 3 volt supply voltage and 4 MHz clock, charging and discharging a 0.55 pF capacitor will discipate 20 microwatts. Since a typical one micron CMOS process FF has about 10-15 fF of gate capacitance, this limits one to about 35-50 FFs toggling at 4 MHz. The question is, "is it possible to design aDate: chip to execute the desired functionality with this low a power consumption". Simulation results suggest that it is possible.

Whle a full discussion of the techniques used to achieve low power consumption will be included in the final report, we can report on some of the more successful tricks.

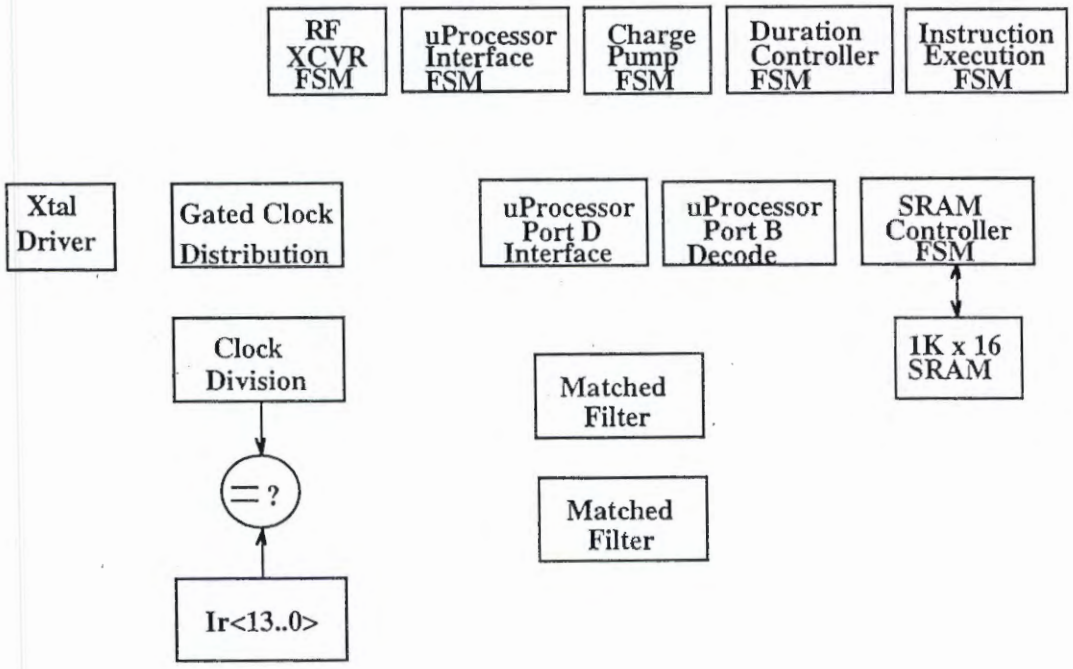
2.5.1 PEA_C Architecture

Except for the power supply, all PEA modem sections are controlled by the microprocessor/PEA_C chip combination in two major modes of operation. In the presynchronized mode of operation, the PEA periodically searches the RF spectrum for a particular sequecne of FM modulated RF bursts called Beacons. Once found, the PEA frequency locks its VCXO to the Beacons and enters the synchronized mode of operation. When synchronized, all PEA activities are scheduled by instructuions contained in the internal SRAM. These instructuion indicate when frequency locking, synchronization, receiving and transmitting take place. They also make it possible to time share the microprocessor for control an external sensor/transducer.

A block diagram of the PEA_C chip is shown in figure 2.5. Major sections include:

* crystal interface
* clock distribution
* frame counter
* microprocessor interface
* matched filter
* SRAM
* RF interface
* charge pump interface
* microprocessor wake-up FSM
* TDMA instruction exection FSM

Figure 2.4 Block Diagram of PEA_C Chip



2.5.2 Power Consumption Reduction Techniques

There are four major components of power consumption in CMOS digital circuits switching, short-circuit, leakage, and static. Switching power is the energy used to charge and discharge the capacitances associated with FETs, during transistions. Short-circuit power is also dissipated during switching. During a transistion both the p-network and the n-network on for a short while. The energy lost due to current flowing directly between supply and ground during a transistion is the short circuit component of power consumption. Leakage power consumption arises from the fact that FETs are not ideal switches and therefore some current will flow even when the devices are off. Lastly, there is static power dissipation. Static power is lost due to current flow between supply and ground while a logic circuit is not switching. It is one of the dominant components in PEA_C because of the need to sustain regulated voltages, and linear amplication.

There are three major principles used in low-power design: voltage scaling, minimizing switched capacitance, and minimizing the effective clock frequency. Voltage scaling involves examining the delay in the critical path and lowering the supply voltage until the delay in that path matches the period of the clock. Minimizing switched capacitance involves lowering the amount of capacitance switched per cycle. Lowering the effective clock frequency is designing circuits so they can be clocked as slowly and as infrequently as possible and still maintain functionality. All three techniques have been applied in the PEA_C design.

Voltage scaling is the most effective method of power reduction in CMOS digital circuits. Switching power, which is the major component of power dissipation in CMOS digital circuits, is proportional to the square of supply voltage. Short circuit power consumption, which is the second largest component of power dissipation, is proportional to the cube of supply voltage, since Isc is proportional to the square of supply voltage. Effective switched capacitance and clock frequency are only linear functions of switching power consumption. Therefore, reducing the supply voltage as much as possible must be the primary goal in low-power digital design.

Minimizing the delay in the critical path involves using the minimum number of logic levels necessary and possible pipelining. By using the minimum number of logic levels necessary, even at the expense of using more hardware, the number of gate delays between input and output is reduced leading to a faster critical path.

Minimizing the average amount of capacitance that is switched each cycle, the effective switched capacitance, is the next method of reducing power comsumption in CMOS logic circuits. The switching power dissipated by a CMOS circuit depends linearly on the amount of effective capacitance switched per cycle. The effective switched capacitance can be reduced by the choice of algorithm and architecture, logic design style, layout style, and duty ratio control.

Proper choice of algorithm and architecture are essential in low-power design. Choosing a proper algorithm involves examining methods of computation and using the method that requires the least number of operations to complete the computation, since this will lead to a minimum amount of switching. While it is easy to say that the architecture in low-power digital systems must be designed to minimize the possibility of wasting power through unnecessary or glitching, transistions, the issue is "can an architecture be found"?.

The final approach to low-power digital design is to lower the clock frequency as much as possible. The switching and the short circuit components of power are both linearly related to the frequency of operation. The primary method of reducing the effective frequency at which a circuit is clocked is through increased parallelism.

2.5.3 Low Power Finite State Machine Design

Low-power finite state machine (FSM) design is important since the PEA_C is essentially a conglomeration of FSMs. In the PEA_C desing, approximately 25 FSMs were employed. We have developed four design styles for subroutine based FSMs. A subroutine based FSM is defined as a finite state machine that only executes a single sequence based on parameters that are passed to the FSM. The four FSMs styles are delay-line, asynchronous, synchronous, and psuedo-grey.

All the FSMs investigated here have the same basic architecture. There is an activation signal and a counter/decoder. The decoder produces the completion signal. The activation signal is produced by an outside source. Once the activation signal is given, the FSM will be active until it's self-generated completion signal. Each of the FSM styles uses a different type of counter. The decoding hardware is responsible for combining the counter output and the input parameters to produce the necessary outputs at the correct time.

The primary goal of low-power FSM design is to reduce the effective switched capacitance (ESC) per cycle. In the PEA_C, with its very small duty cycles, the ESC can be dominated by the capacitance switched while the circuit is inactive. Therefore, the capacitance switched while inactive needs to be minimized. An architecture that has only two gates capacitances switching every cycle, the minimum using standard CMOS design, is thus used in these FSMs.

The delay-line FSM is based on a using a tapped delay line to produce the correct output at the correct time. The advantages of using a tapped delay line are the easy of design, a simple shift register will suffice, and the ease of decoding, just connect the outputs that are needed. The disadvantage of using a tapped delay line is the amount of hardware that is necessary to impliment the counter, 2N register cells for an N-bit counter.

The asynchronous FSM style is based on an asynchronous or "ripple" counter. Its advantage is the fact the counter uses a minimum amount of hardware to complete the task of counting. The delay in the switching times of the counter bits is the main disadvantage of using an asynchronous counter. These delays make designing a decoder without spurrious, glitching, transistions difficult. These glitching transistions can cause the circuit to malfunction and will increase the activity factor of the circuit.

The synchrounous style uses the following counter cell to implement a synchronous counter. Since the counter is synchronous, designing a glitch free decoder is easier. However, the power consummed by the extra hardware necessary for the synchronous counter can be more costly than the glitching transistions.

The pseudo-grey style FSM style is based on pairwise grey code counter. Pairwise grey code counts as follows. The advantage of using pseudo-grey code is the reduced activity factor of the counter, without increased counter cell complexity. The activity factor for a synchronous counter is 2.

If the power consumption were based strictly on the style of counter, The asynchronous design style would be prefered since the synchronous counter consummes the least amount of power, in most cases. However, in the low duty cycle situations encountered in the BodyLAN application, the power comsummed by a FSM machine in these styles depends not only on the counter, but on the decoding of the signals.

The method of decoding chosen will be a large factor in determining which finite-state machine uses the least amount of power. Two styles of decoding the signals were investigated, one uses demultiplexers and the other uses an AND-gate configuration. The power consummed by these two decoding styles increases drastically as the number of bits is increased However, over this range of values, the demultiplexer style of decoding has the lowest power consumption. However, this data only represents the case where the FSM must produce a different output every cycle (ie each counter output must produce a different signal). In the BodyLAN application, the FSM needs to produce a signal every two or more cycles. The power dissipated in the decoder decreases dependent on the number of signals necessary.

2.5.4 Matched Filter

The PEA has three major modes of operation: attachment, pre-synchronized, and synchronized. In the attachment mode, all parameters unique to a particular BodyLAN are not present. Attachment is the process by which the HUB transmits these parameters to a PEA. After attachment, the parameters which allow a PEA to synchronize itself to the HUB and communicate over the Command and Control Channel have been loaded into the PEA_C SRAM.

In both the attachment and pre-synchronized modes, the PEA searches the RF spectrum for Beacons. There are two flavors of Beacons which we call Attachment and Synchronization Beacons. When the PEA is in the attachement mode, it searches for Attachment Beacons while in the pre-synchronization mode it searches for Synchronization Beacons. Both Beacon flavors consist of 8 FM modulated RF bursts. These burst are separated by gaps which are fixed and built into the hardware. Each burst contains four bits. Bits of the Attachment Beacon are built into the hardware. Thus on power-up a PEA is able to search for Attachement Beacons because it 'knows' where the bursts are located relative to one another and the modulation bit sequence.

Searching for Beacons involves turning on the receiver continuously (i.e. 4-6 milliwatts of power consumption). We have thus been motivated to include hardware to minimize the search time. Accordingly, we have incorporated a digital matched filter. This filter generates a match when the last 520 bits matches that of a template. To match a Beacon, 488 of the 520 bits are 'don't cares'. Of the remaining 32 bits, we say that a match has occurs if any 29 out of the 32 bits matches that of an internally microprocessor register.

Complicating the process is the need to oversample the receiver output stream because bit level synchronization has not been established. In the current plan, we oversample only by a factor of two to one rather than the normal three to one or even four to one. Since each oversample needs its own state, a two to one oversample then requires 1040 bits of state and a detector for each state.

The matched filter section consists of two full matched filters, working on opposite clock phases. Each matched filter consists of a tapped delay line, a comparison circuit, an adder and another pair of comparison circuits. The tapped delay line produces the necessary bits from an input string. The first comparison circuit takes the 32 bits from the delay line and bitwise compares them to the code. The 32 bit output of the first comparison circuit is then summed to determine the total number of bits which matched. This 6 bit output of the adder is then compared against two thresholds using the second two comparison circuits to determine if the output is a hit.

The tapped delay line will consume the maximum amount of power, since the tapped delay line has the most hardware, 520 register cells, switching at the highest frequency, the symbol rate. Therefore, minimizing the power comsummed by the tapped delay line is a must. This power was reduced using two methods. The first method consisted of designing low-power register cells to use in the delay line and the second consisted of using parallelism to further reduce power consumption.

Four low-power shift register cells were designed and analysed, a C2MOS register, a true single-phase clock register (TSPCR), a low-power frequency divider, and another register with low clock load. Each register was designed using minimum sized transistors whenever possible. Using minimum size transistors in almost all cases means that the n and p networks for most of the registers are not balanced. Therefore, the rise and fall times of the registers will not be equal. While this is not ideal, it poses no real problems aas long as both the rise time and fall time meet the delay constrait.

The C2MOS register consists of two tri-state buffers connected in series and activited using clocks with oppositive phase. The minimum number of transistors are used in this design, eight, which limits gate capacitance, there are only two paths between source and ground, where the current needs to flow through four transistors, which will limite short circuit current. Unfortunately, this register require both clock phases for each register cell.

The true single-phase clock register is taken from the Berkeley Low-Power Cell Library. The advantage of using a TSPCR is the use of only one clock phase, which eliminates a large amount of routing capacitance. The disadvantages of using the TSPCR is the number of transistors, eleven, and the fact not all of the transistorscan be minimum sized, some must be larger to insure proper circuit operation.

The low-power frequency divider, is basically a standard CMOS register with a number of redundant transistors removed. The register consists of two D-latches clocked on opposite phase. Each register has the following form: The problem with this register is the number of transistors that are needed, sixteen, and the fact that both input and it's complement are needed as well as both clock phases, which leads to a lot of excess routing capacitance. The one small advantage is the fact both Q and Q are produced.

The final register design was developed from a D-latch in (Weste). Only four transistors are connected to the clock in this design and all of the transistors in the design are minimum sized. Also, all the p networks consist of one transitor and all the n networks consist of two transistors in series, the rise and fall times should be about equal. Unfortunately, this design uses twelve transistors and both clock phases.

Each of the registers was layed out in Magic and extracted to Hspice for simulation. The average switched capacitances for a rising (Data =1) and falling (Data = 0) transitions, driving another register of the same type, were then measured for a range of supply voltages. The results show the C2MOS register comsumes the least power.

The outputs of the delay-line are then compared to the code and summed. The code comparison is done using simple xor gates, which will give a one if the bits match and a zero if they do not match. The 32-bit comparitor outputs are then summed, first by compressing the 32 bits into eight 3-bit sums, then using a three structure to add the bits as shown This addition comprises the single largest path in the entire circuit.

2.5.5 Charge Pump

The microprocessor and a series of charge pumps act as the digital filter. The purpose of the digital filter is to change the frequency of the local oscillator by increasing the voltage across a varactor. This voltage is increased by adding charge to a capacitor connected to the varactor. The microprocessor processes the information provided by PEA_C and computes the degree of correction necessary. The degree of correction is translated to the number of times a charge pump needs to be triggered to make that correction. The number of times the charge pump needs to be triggered is transmitted to PEA_C, which gates a clock to the charge pump. The charge pump the adds the necessary charge to the capacitor to make the correction.

2.5.6 Duration Controller

The duration controller's primary function is to control the analog Duration Comparitor circuit. It secondary function is to provide the interface between the oscillator, receiving and transmitting, hardware. The duration controller has been broken down into four simpler components: digital counters, control output decoding, output decoding, and the central controller. The digital counters are used to produce time intervals that are oscillator dependant. The control signal decoder produces the control signals for the analog phase detector, the receiver oscillator hardware and the transmitter oscillator hardware. The output decoder pre-processes the information from the analog phase detector for the microprocessor. The controller provides timing information for the other components.

The charge pump control circuit takes a five-bit input from the microprocessor and produces a series of pulses for a specificed charge pump. The two most significant bits of the input determine which charge pump the pulses are directed to the VCXO, the receiver's LO, or the transmitter oscillator.

2.5.7 Power Consumption Results

Since the PEA_C has not been fabricated, physical measurement of the power dissipation is not possible. Therefore, extensive simulation was used to approximate the average capacitance switched per cycle. Switched capacitance is a good metric for computing power consumption since it is easily combined with the frequency and the supply voltage, both of which are known, to give an estimate of average power consumed.

Three different methods of determining the average switched capacitance of a circuit were employed. The first method uses irsim-cap, which is a switch level simulator that has extensions for computing switched capacitance. The second method uses hspice to measure the amount of current drawn from the supply. The final method is estimating the switched capacitance by hand calculation.

Irsim-cap is a modified version of the irsim-9.0 program developed by Stanford University. The modifications, performed by Paul Landman at UC Berkeley, include commands to measure only the capacitance switched vs. irsim-9.0 measurement of the total capacitance in the circuit. To measure the switched capacitance for a given simulation, irsim-cap records the number of times each node transistions and the capacitance of each node.

Estimating the switched capacitance using Hspice involves measuring the total power dissipated during a simulation and comparing that with the energy need to charge a capacitor. Since the supply voltage is constant, the effective switched capacitance is equal the to integral of the supply current divided by the supply voltage.

The final method of power estimation used was hand calculations. To estimate the power consumed using hand-calculations the capacitance of the cells must first be determined. Since the purpose of the hand-calculation method is to provide a quick estimate of the power consummed all cells were characterized by only the input and output capacitances ignoring any internal capacitances. The reasons for this is simple, first of all the activity factors for the inputs and outputs are generally easily derived, however, the activity factors for internal nodes are generally much more complex. Secondly, the number of input and output nodes for a cell is generally small, while the number of internal nodes can be very high.

To determine the input and output capacitances the capacitance per unit area for gate, p-diffusion, and n-diffusion were calculated from Spice parameters provided by Mosis. The total gate, p-diffusion, and n-diffusion area were determined by examining each cell. The capacitances per unit area and area measurements were then combined to produce an equivalent capacitance at each input and output nodes. The activity factors (a) for each input and output node were then determined. These activity factors multiplied by the capacitances produced an estimate of switched capacitance.

Each method of power estimation has it's advantages and disadvantages. Hspice is the most accurate of the power estimation techniques since it accounts for all the current drawn from all the sources, including short circuit, subthreshold, and leakage currents. However, simulating large designs in hspice is not feasable because the run time of an hspice simulation is so long. Therefore, hspice simulation should be restricted to those sections that require precision power estimation.

Irsim-cap is the second most accurate power estimation technique since it takes into account the internal capacitances as well as the external (input/output) capacitances. The main advantage to irsim-cap is the simulation speed. Since irsim-cap is a switch level simulator on average, it will run much faster than hspice, with results that are relatively accurate. The major disadvantage in using irsim-cap is the fact a circuit layout must be produced before the simulator can be used. Therefore, irsim-cap is ideal for power consumption estimation of large systems from layout.

Hand-calculations tend to be the least accurate of the power estimation techniques, since it does not account for any internal capacitance switching. Since not of the internal nodes are accounted for hand-calculated power estimates are increasingly low as circuit complexity increases. The advantage of hand-calculations is that sections do not need to be layed out. A power estimate, within an order of magnitude, can be achieved with only a paper design and logic cell characterizations.

All three power estimation methods were used on a set of circuits which exhibited increasing complexity. The circuit set included, in order of increasing complexity: a single inverter, a chain of five inverters, a four bit AND-AND array, a five-bit shift register, and a five bit full adder. For circuits with low complexity, all three of the power estimation techniques give values that are similar. As the systems become increasingly complex, the power estimate using hand analysis is increasingly low, which the analysis using irsim-cap is still approximately equal to the Hspice analysis. While hand analysis can be used to give a rough estimate of power consumption, within an order of magnitude, it is not reliable for complex circuits. However, irsim-cap power estimations are valid at high levels of complexity.

While the current talley has not been completed, the current estimate of PEA_C power consumption in the synchronized mode of operation supporting a 2K b/s channel is around 20 microwatts. An extensive description of PEA_C and its power consumption estimates on a section by section basis will be included in the final report.

3.0 Software

A protocol functional specification of the PC residing software was completed in the last reporting period. Due to funding exhaustion, no software implementation work was done in this reporting period.

An abbreviated firmware functional specification for the HUB and PEA microprocessors has been completed. Firmware for the MC68356 HUB microprocessor, because it is based on a Motorola 68000 compatible code, can be developed on BBN's ubiquitous SUN workstation platforms. Since there are no SUN platform environments for firmware development of the Microchip PIC16C64 PEA microprocessor, BBN has internally purchased the appropriate PC based development system. We now have development environments for both BodyLAN microprocessors.

4.0 Spread Spectrum Signals

We have described in previous technical reports, the design and performance of a TDMA signaling scheme based on Optical Orthogonal Codes (OOC). These codes are optimal for certain coditions. However, prior to this reporting period, our use of these codes in the BodyLAN application to avoid interference between multiple interacting BodyLANs did not conform to the optimum conditions. This has been an ongoing problem for several years. Recently, we have discovered a means for using OOCs and other similiar codes which results in optimum performance in the BodyLAN application domain. We have called this scheme Ordered Optically Orthogonal Coding (OOOC).

A new class of codes has been discovered which gives optimum performance in the BodyLAN application. Preliminary analysis suggest these codes to perform about as well as OOOC.

Funding exhaustion has caused all project work to be concentrated on the prototype hardware evaluation. BBN has accordingly sponsored all signal spectrum work off project.

4.1 Ordered Optically Orthogonal Coding

The signaling scheme previously proposed partitioned a 32.768 millisecond frame into 256 slots. One of the ten OOCs was selected, rotated by 0<=N<64 shift positions. During each of the three 'one' bit instances of the rotated codeword, a burst of four user data bits were transmitted or received. Thus during each slot, 12 data bits are transmitted. The current hardware supports both majority encoding, netting three error corrected bits per slot, or single bit error correction, netting eight corrected bits per slot. Error correction can be selected on a slot by slot basis.

Our previous plan was to setup a TDMA plan by choosing an OOC and a rotation value for each slot in which data by random selection. When two BodyLANs are precisely synchronized so that their slots coincide with one another, errors are possible because the two BodyLAN use exactly the same codeword and rotation values. Because the code diversity (Diversity = number of codewords times the number of rotations) is small, the error rate under under this idea situation is 0.78e-3.

When the slots of two BodyLANs are not synchronized, the error rate caused by burst collisions, increases because OOCs are not orthogonal crossing slots. This is easily visualized by examining the simplified burst sequence of two interfering BodyLANs shown below.

```
|  a0      a1  a2       |  a3  a4      a5     |
   b0  b1   |   b2  b3       b4   |     b5
```

Here a[0:3], a[3:5] and b[2:4] are each rotated codewords. If the slots of the two BodyLANs were precisely aligned with one another, we would be guaranteed that at only one of the bursts in each BodyLAN's codewords would collide. In the normal case, the slots are not aligned. this leads to the situation where the first and last burst of a codeword in one BodyLAN (e.g. b2 & b4) collide with the last and first burst of successive slots of the other BodyLAN (e.g. bursts a2 & b2 collide and burst a3 & b4 collide). This situation creates errors even when majority error correction is employed. In the example, b2 and b4 can both be simultaneously corrupted by collisions with a2 and a3.

In the new scheme, which we call Ordered Optically Orthogonal Coding (OOOC), the HUB software simply disallows selection of a shifted codeword which results in this type of collision. In the example above, the a[3:5] shifted codeword could not be selected because there exists a code word having the the same span as a2 to a3. Thus for the expected two BodyLAN case, the use of OOOC implies that a codeword can have at most zero or three collisions with the other BodyLAN.

With majority error coding, all single collision cases are corrected 100%. Only triple collisions can result in errors and then only when the received power level of the interfering BodyLAN is greater. The problem is that while the diversity of the (64,3,1) OOCs is relatively large (i.e. 640), the number of codewords is small. For the selected (64,3,1) OOC, there are only ten codewords. Thus as two non-synchronized BodyLANs frame systems slowly slide by one another, the probability that any given slot has a triple collision case is about 0.05.

We can reduce this problem by judiciously selecting a shift/codeword sequence for a given BodyLAN. Let us assume that the OOOC code diversity is larger than the number of codewords. We name the shift/codeword combinations a, b, c...y, z, a'...z', a"... Let us further assume that the shift/codeword sequence is generated with the rule that no shift/codeword is ever selected twice.

When two BodyLAN frames slowly side by one another, the probability of two codewords suffering triple collisions is essentially unity. The probability of two and three codewords suffer triple collisions drops rapidly to 1/(D-1) and 1/[(D-1)(D-2)] respectively. If we were to incorporate one or two floating slots in each BodyLAN frame which could temporarily replace the one or two slots suffering triple collisions, the error rate could again be reduced to zero with majority encoding. We will be examining this mechanism of collision avoidance during the next reporting period.

4.2 Linear Orthogonal Codes

A problem in using OOCs in the BodyLAN application is that they were designed assuming the transmitting agent would send either a codeword or nothing at all and all users were slot aligned. In the original application, a zero could go to a one, but a one could never go to a zero. This provides several advantages over the scheme employed in BodyLAN. Nevertheless, OOCs have been employed to achieve acceptible results. We have recently created new codes specifically taylored for the BodyLAN application. A preliminary analysis suggests results comperable to OOOCs. We call these codes Linear Orthogonal Codes (LOC).

Each codeword of an LOC is composed of three bursts separated by intervals La & Lb. Each codeword is generated by constructing a table of unallowed intervals. La[i] of each codeword equals its index i. Thus intervals 1, 2, 3,...N are unallowed. Lb[i] is determined by finding the smallest unused interval and then unallowing Lb[i] and La[i]+Lb[i]. Codesets having 6, 7, 8, 9, and 10 codewords are shown below:

Number Codewords.		Average Length	Maximum Span	Nu
6	{0,1,8}, {0,2,11}, {0,3,13}, {0,4,16}, {0,5,19}, {0,6,21}	15.7	22	3
7	{0,1,9}, {0,2,12}, {0,3,14}, {0,4,17}, {0,5,20}, {0,6,22}, {0,7,25}	18.1	26	4
8	{0,1,10}, {0,2,13}, {0,3,15}, {0,4,18}, {0,5,21}, {0,6,23}, {0,7,26}, {0,8,28},	20.3	29	4
9	{0,1,11}, {0,2,14}, {0,3,16}, {0,4,19}, {0,5,22}, {0,6,24}, {0,7,27}, {0,8,29}, {0,9,32},	22.6	33	5
10	{0,1,12}, {0,2,15}, {0,3,17}, {0,4,20}, {0,5,23}, {0,6,25}, {0,7,28}, {0,8,30}, {0,9,33}, {0,10,36},	24.9	37	6

The first N-1 of each LOC[N] are one unit longer than the first N-1 codewords of LOC[N-1]. Thus the average length of LOC[N] is about 2.3 units longer than the average length of LOC[N-1]. Each LOC[N] also has a number of intervals smaller than the maximum span which are allowed spaces between subsequent codewords.

Each codeword of a set has the orthogonal property that C[i] intersects C[j] in at most one position when shifted left or right an arbitrary number of positions. If we choose the space between codewords to be greater than the maximum span or equal to one of the Nu unused intervals less than the maximum span, then two code sequences formed from LOC[N] are orthogonal to one another. By this is meant that two codewords in one sequence can have either one or three burst collisions when one sequence is shifted left or right relative to the other sequence an arbitrary interval.

With majority coding, we can correct all one burst collisions. Thus a metric of a code's 'goodness', is the probability of triple burst collisions, i.e. where the same codeword in each sequence is aligned. If each of the two sequences used different codewords, then the probability of triple collisions would be zero. When only two BodyLANs are interfering with one another, selecting different codewords would result in zero uncorrectible errors. Unfortunately, if we were to assign each BodyLAN a random codeword, the probability of two BodyLANs meeting using the same code is 1/N. Since there are only a small number of codewords in LOC[N], 1/N is prohibitively large. Schemes to dynamically change codeword when interference is detected have been explored, but all involve complex protocols and substantial error degradation during the transition between one codeword and another.

As was done with OOOCs, we can partially solve this problem by constructing codeword/space symbols and using the symbols only once during each frame. Because two BodyLANs clocks are never frequency locked. there will always be a time when codewords in each BodyLAN exactly overlap. This will create a triple burst collision and probably cause an error even with majority encoding. The probability that two successive codewords exactly overlap is proportional to 1/(D-1), where D=number of symbols. A 'good' code is then one which has a large value of D.

For an LOC, the number of symbols equals the number of code words (Nc) times the number of interval alternatives (Ns) between codwords. By increasing Ns, the number of symbols (Nsym=Nc*Ns) can be increased indefinitely. Increasing Ns, however, causes the average symbol length to increase. Thus a better measure of a code's 'goodness' is which code yields the largest number of symbols for a specified average symbol length. For example, for an average symbol length of 64 units, LOC[6] is the optimum, yielding a total of 348 symbols. Doubling the average length typically quadruples the number of symbols because both Nc and Ns both double. For an average length of 128 units, LOC[12] is the optimum, yielding a 1536 symbols, a 4X improvement.

For LOC[12], a typical code sequence will have a codeword whose average length is 29.5 units followed by an interval with no bursts. This interval will average 98.5 units and range from as little as 36 to a maximum of 164. For the 92 symbols having spaces greater than 72, we can insert another codeword into the space interval. Thus the symbol set consists of a few symbols having a single codeword and a far larger number containing two symbols. The average length of the symbol set has decreased because most symbols have two codewords but the number of symbols has dramatically increased. This same concept can be applied over longer intervals. It thus appears possible to create a symbol set having an arbitrarily large number of symbols.

Note that the BodyLAN hardware allows arbitrary positioning of a codeword's first burst within a frame and specification of interburst gaps up to 64 units. This will allow use of all LOC codes for N<32 if we should so choose.

Dawn

PURCHASE REQUEST AND COMMITMENT

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PURCHASE INSTRUMENT NO.	REQUISITION NO.	DATE	PAGE
	HJ1500-4348-0535	16 DEC 94	1 OF 1 PAGES

TO: Purchasing and Contracting Officer

THRU: N/A

FROM: INTELLIGENCE CENTER & FORT HUACHUCA
DIRECTORATE OF COMBAT DEVELOPMENTS

It is requested that the supplies and services enumerated below or on attached list be:

PURCHASED FOR	DELIVERED TO	NOT LATER THAN *(Date)*
DIRECTORATE OF COMBAT DEVELOPMENTS SCIENCE & TECHNOLOGY DIVISION ATZS-CDS	SAME	

The supplies and services listed below cannot be secured through normal supply channels or other Army supply sources in the immediate vicinity, and their procurement will not violate existing regulations pertaining to local purchases for stock, therefore, local procurement is necessary for the following reason: *(Check appropriate box and complete item.)*

NAME AND TELEPHONE NO. OF PERSON TO CALL FOR ADDITIONAL INFORMATION
MR. ROBERT BOLLING
602-538-7500

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ITEM	DESCRIPTION OF SUPPLY OR SERVICES	QUANTITY	UNIT	ESTIMATED Unit Price	ESTIMATED Total Cost
1.	Provide funding in support of ARPA/ESTO Program: HDS-WIRELESS				$240,366.00
2.	REF: ARPA Order A841/14 BBN Systems and Technology DABT63-94-C-0017				

Fund Certification

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97504001301000500505T10A841142581 000000HJ150043480535JWBL00S02086	$240,366.00

DATE	TYPED NAME AND TITLE OF CERTIFYING OFFICER	SIGNATURE
16 DEC 94	ANTONIO Z. GUTHRIE DCD Budget Analyst ATZS-CDP X3-3264/3264	A Z Guthrie

DISCOUNT	
PURCHASE ORDER NUMBER	
DELIVERY SCHEDULE	

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DATE	TYPED NAME AND GRADE OF INITIATING OFFICER	SIGNATURE
16 DEC 94	DAWNE L. SPENCER, DAC, X3-3263	Dawne L. Spencer

DATE	TYPED NAME AND GRADE OF SUPPLY OFFICER	SIGNATURE
	SERVICES N/A	

DATE	TYPED NAME AND GRADE OF COMMANDING OFFICER OR DESIGNEE	SIGNATURE
16 DEC 94	JOHN DRAGOO C, Program Management Office	John D Dragoo

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EMERGENCY SITUATION PRECLUDES USE OF REQUISITION CHANNELS FOR SECURING ITEM

ITEM	DESCRIPTION OF SUPPLY OR SERVICES	QUANTITY	UNIT	ESTIMATED Unit Price	ESTIMATED Total Cost
	Provide funding in support of ARPA/ESTO To Program: HIGH DEFINITION DISPLAY TECH REF: ARPA ORDER A841/04 BBN Systems and Technologies NEW				$483,684.00

NAME AND TELEPHONE NO. OF PERSON TO CALL FOR ADDITIONAL INFORMATION
MR. ROBERT BOLLING
602-538-7500

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97404001301000500 5P4T10A841042594 000000HJ150040060533JWC900002086	$483,684.00

DATE	TYPED NAME AND TITLE OF CERTIFYING OFFICER	SIGNATURE
07 JAN 94	ANTONIO Z. GUTHRIE DCD Budget Analyst ATZS-CDP X3-3352	A.Z. Guthrie

DISCOUNT	
PURCHASE ORDER NUMBER	
DELIVERY SCHEDULE	

THE FOREGOING ITEMS ARE REQUIRED NOT LATER THAN AS INDICATED ABOVE FOR THE FOLLOWING PURPOSE

DATE	TYPED NAME AND GRADE OF INITIATING OFFICER	SIGNATURE
7 Jan 94	DAWNE L. SPENCER, DAC, X3-3263	Dawne L Spencer
10 Jan 94	TYPED NAME AND GRADE OF SUPPLY OFFICER: THOMAS J.MCMAHAN CPT, XO, DCD	Thomas J. McMahan

Approved by commanding officer or his designee

DATE	TYPED NAME AND GRADE OF COMMANDING OFFICER OR DESIGNEE	SIGNATURE
07 JAN 94	JOHN DRAGOO C, Program Management Office	John Dragoo

DA FORM 1 AUG 76 3953

PREVIOUS EDITIONS OF THIS FORM WILL BE USED UNTIL EXHAUSTED.

ADVANCED RESEARCH PROJECTS AGENCY
3701 NORTH FAIRFAX DRIVE
ARLINGTON, VA 22203-1714

To: Commander
U.S. Army Intelligence Ctr & FH
Program Management Office

Fort Huachuca, AZ 85613-6000
Attn: ATZS-CDP

Date: NOV 30 1994
AO: A841
Amendment: 14
Industrial Priority Rating: DO

1. Performer: BBN Systems and Technologies Contract No: DABT63-94-C-0017

2. This ARPA Order provides **incremental** funding in support of ARPA/ ESTO
Program: HDS-WIRELESS

Provided FY 95	Revised Planned FY 95	Revised Planned FY ___	Revised Planned FY ___	Revised Planned FY ___
$240,366	$0			

If outyear funding is provided, it is subject to the availability of funds; therefore, a "Limitation of Funds" clause should be included in the contract.

3. Special instructions:

4. This order is issued under provisions of DOD Directive 7200.1 and properly chargeable to allotment(s) set forth below, the available balances of which are sufficient to cover the estimated total price. See attached distribution for financial reporting and billing instructions.

Appro-priation	Limit	Supplemental Accounting Classification	ACCTG STA	Amount	Program Code	Program Element
9750400	1301			$240,366	5T10	62708E

These funds provided expire for obligation purposes on: 9/15/95 and can only be extended by an Amendment to this ARPA Order. These funds are available
for immediate obligation
on behalf of Advanced Research Projects Agency and are only to be used for the purposes necessary to accomplish the work specified herein.

for James E. Fargo
Authorizing/Certifying Official
Gregory Colocotronis, Comptroller

5. ARPA Instruction No. 21 entitled "ARPA/Agent General Requirements" is incorporated herein by reference.

6. Points of Contact: Name/Office/Telephone/Fax/E-Mail

Agent Technical:	MR. BOB BOLLING ;ATZS-CDT-T	AIC	(602) 538-7500
Fax:			
ARPA Technical:	Ken Gabriel	ESTO	(703) 696-2252
Fax:	(703) 696-2203 kgabriel@darpa.mil		
ARPA Business:	Robert Glaze	ESTO	(703) 696-2212
Fax:	(703) 696-2203 rglaze@darpa.mil		

7. A. Purpose Of Action: DUE BILL DELETE

B. FFRDC Ceiling: N/A

C. CAAS Category: N/A Object Class: N/A

8. Remarks:

Non-CAAS -- ARPA has reviewed the work to be performed under this ARPA Order Amendment and determined that it does NOT fall under the definition of "Contracted Advisory and Assistance Services" as identified under DoD Directive 4205.2.

All other terms and conditions of this Order remain unchanged by this Amendment.

Distribution for Financial Reporting and Billing Instructions

In accordance with DoD Directive 7200.1, the Status of Allotments (Financial Report) and budget execution reports must be forwarded to:

DFAS DAO-DE AFDW/FW
Room 1D476, The Pentagon
Washington, D.C. 20301-1155

Copies of all obligation documents and modifications must be sent to:

Advanced Research Projects Agency
Comptroller
Attention: FMD
3701 North Fairfax Drive
Arlington, VA 22203-1714

Fax No. (703) 696-2200

ADVANCED RESEARCH PROJECTS AGENCY
3701 NORTH FAIRFAX DRIVE
ARLINGTON, VA 22203-1714

To: Commander
U.S. Army Intelligence Ctr & FH
Program Management Office

Fort Huachuca, AZ 85613-6000
Attn: ATZS-CDP

DEC 15 1993
Date:
AO: A841
Amendment: 4
Industrial Priority Rating: DO

1. Performer: BBN Systems and Technologies Contract No: New
Proposal Title & No: BodyLAN: A Wireless Body Local Area Network
P94-LABS-C-002 Proposal Date: 07/08/93

2. This ARPA Order provides funding in support of ARPA/ ESTO Program: HIGH DEFINITION DISPLAY TECH

Provided	Planned	Planned	Planned	Planned
FY 94	FY 95	FY ___	FY ___	FY ___
$483,684	$240,366			

This Order provides FY 94 funding for 12 months of a total 18 month effort. If outyear funding is provided, it is subject to the availability of funds; therefore, a "Limitation of Funds" clause should be included in the contract.

3. Special instructions:
PROPOSAL AND SELECTION JUSTIFICATION PROVIDED SEPARATELY.

4. This order is issued under provisions of DOD Directive 7200.1 and properly chargeable to allotment(s) set forth below, the available balances of which are sufficient to cover the estimated total price. See attached distribution for financial reporting and billing instructions.

Appro-priation	Limit	Supplemental Accounting Classification	ACCTG STA	Amount	Program Code	Program Element
9740400	1301			$483,684	4T10	62708E

These funds provided expire for obligation purposes on: 6/30/94 and can only be extended by an amendment to this ARPA Order. These funds are available
for immediate obligation
on behalf of Advanced Research Projects Agency and are only to be used for the purposes necessary to accomplish the work specified herein.

Gregory Colocotronis
Authorizing/Certifying Official
Gregory Colocotronis, Comptroller

5. ARPA Instruction No. 21 entitled "ARPA/Agent General Requirements" is incorporated herein by reference.

6. Points of Contact: Name/Office/Telephone/Fax/E-Mail

Agent Technical:	Robert D. Bolling ; ATZS-CDA	AIC	602-538-2319
Fax:	602-538-7692		
ARPA Technical:	Ken Gabriel	ESTO	(703) 696-2252
Fax:	(703) 696-2203 kgabriel@arpa.mil		
ARPA Business:	Robert Glaze	ESTO	(703) 696-2212
Fax:	(703) 696-2203 rglaze@darpa.mil		

7. A. Purpose Of Action: New Contract

B. Source Of Selection: BAA, Number:93-27

C. FFRDC Ceiling: N/A

D. Tech Report Requirements: Quarterly, Final

E. SIRMR Approval: N/A

F. Security Classification: Unclassified

G. CAAS Category: N/A Object Class: N/A

H. Pre-contract Costs: N/A

8. Remarks:

Non-CAAS -- ARPA has reviewed the work to be performed under this ARPA Order Amendment and determined that it does NOT fall under the definition of "Contracted Advisory and Assistance Services" as identified under DoD Directive 4205.2.

Distribution for Financial Reporting and Billing Instructions

In accordance with DoD Directive 7200.1, the Status of Allotments (Financial Report) and budget execution reports must be forwarded to:

DFAS DAO-DE AFDW/FW
Room 3B287, The Pentagon
Washington, D.C. 20301-1155

Copies of all obligation documents and modifications must be sent to:

Advanced Research Projects Agency
Comptroller
Attention: FMD
3701 North Fairfax Drive
Arlington, VA 22203-1714

Fax No. (703) 696-2200

DEFENSE ADVANCED RESEARCH PROJECTS AGENCY
3701 NORTH FAIRFAX DRIVE
ARLINGTON, VA 22203-1714

PROCUREMENT GUIDANCE

Funding provided via PBAS Transaction Number NO PBAS.
This document provides official guidance pertaining to ARPA Order A841/32.
Performer: Bolt, Beranek & Newman, Inc. Contract No.: DABT63-94-C-0017

TECHNICAL POINTS OF CONTACT

AGENT (AIC)
Name/Office: Ms. Clara M Billock
Phone: (520) 533-3903
Fax: (520) 533-1195
Email:

DARPA
Name/Office: Kelly Archer/COMP
Phone: (703) 696-0242
Fax: (703) 696-2200
Email: karcher@darpa.mil

SPECIAL INSTRUCTIONS

DARPA Comptroller Office: Beth Carman (703) 696-2416

This document provides guidance for FY 1995 for 1 month(s) of a total 1 month effort.

DARPA has determined that work being funded by this document is not classified as Advisory & Assistance Services as defined in DoD Directive 4205.2.

FFRDC: N/A

Security: Unclassified

This amendment withdraws $9,889.28 of unobligated FY95 funds originally provided under ARPA Order A841-14, Line 1.

I certify that these funds are available for withdrawal and will not cause an overobligation.

_____
Signature

FUNDING PROFILE

	Provided FY 1995	Planned/ Revised FY____	Planned/ Revised FY____	Planned/ Revised FY____	Planned/ Revised FY____
Amount:	$-9,889.28				

For Carol J. Kramer	(DARPA Business POC)	07/12/2000 (Date)	(703) 696-2274 (Phone)	ckramer@darpa.mil (Email)
	(Office Director)	(Date)	(703) 696-2395 (Phone)	wieht@darpa.mil (Email)
Comptroller		07/13/2000 (Date)		

DARPA Form 49, June 97

SF 1034, OCT 83 PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

DEFENSE FINANCE AND ACCOUNTING
DRAWER P
FT HUACHUCA, AZ 85613-6000

VOUCHER NO.

DATE PREPARED 05/28/96

CONTRACT NO./DATE DABT63-94-C-0017 04/05/94

PAID BY
Account of:
DSSN 6424

TAX ID
PAYEE'S BBN SYSTEMS & TECHNOLOGIES
NAME DIV OF BOLT BERANEK & NEWMAN
ADDRESS P.O BX 4340
BOSTON MA 02211

FT HUACHUCA, AZ 85613-6000

DATE INVOICE RECV'D 04/29/96
DISCOUNT TERMS: NET 30 DAYS

FOB:
DEST

NO./DATE OF ORDER	INV DATE	DATE OF PERFORMANCE INVRCV'D	MDSE DEL	MDSE ACPT	FREIGHT	MERCHANDISE
20C	05/13/96	04/29/96	04/29/96	04/29/96	0.00	1084.05

TOTAL: MDSE+ 1084.05

AMOUNT VERIFIED CORRECT FOR $$ 1084.05
SIGNATURE OR INITIALS: /S/

PAYMENT: 2:PARTIAL 05/29/96

PURSUANT TO THE AUTHORITY VESTED IN ME, I CERTIFY THAT THIS VOUCHER IS CORRECT AND PROPER FOR PAYMENT.

AUTHORIZED CERTIFYING OFFICER DATE: 05/28/96
FOR: DAN GLEZNIK

DEFENSE ACCOUNTING OFFICER

ACCOUNTING CLASSIFICATIONS
97504001301600500510A3411400 2581 502084 US JWBL00 00JWBL HD1500434B0535 1084.05

PAYEE: BBN SYSTEMS & TECHNOLOGIES
DIV BOLT BERANEK & NEWMAN INC
P.O. BOX 4340
BOSTON MA 02211

CHECK AMT $$ 1084.05

CHECK NO.: ON US TREASURY DATE:

SF 1034-EDP PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

DEFENSE FINANCE AND ACCOUNTING
DRAWER P
FT HUACHUCA, AZ 85613-6000

VOUCHER NO.

DATE PREPARED 05/28/96

CONTRACT NO./DATE DABT63-94-C-0017 04/05/94

PAID BY
Account of:
DSSN 6424

TAX ID
PAYEE'S NAME BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
ADDRESS P.O BX 4340
BOSTON MA 02211

FT HUACHUCA, AZ 85613-6000

DATE INVOICE RECV'D 04/29/96
DISCOUNT TERMS NET 30 DAYS

FOB:
DEST

NO./DATE OF ORDER	INV DATE	DATE OF PERFORMANCE INVRCV'D	MDSE DEL	MDSE ACPT	FREIGHT	MERCHANDISE
20C	05/13/96	04/29/96	04/29/96	04/29/96	0.00	1084.05

TOTAL: MDSE+ 1084.05

AMOUNT VERIFIED CORRECT FOR $$ 1084.05
SIGNATURE OR INITIALS: /s/

PAYMENT: 2SPARTIAL 05/29/96

PURSUANT TO THE AUTHORITY VESTED IN ME, I CERTIFY THAT THIS VOUCHER IS CORRECT AND PROPER FOR PAYMENT.

AUTHORIZED CERTIFYING OFFICER DATE: 05/28/96
FOR: DAN BLIZNIK

DEFENSE ACCOUNTING OFFICER

ACCOUNTING CLASSIFICATIONS
97504001301000500ST10A8411400 2581 S02086 US JWBL00 00JWBL HJ150043480535 ~ 1084.05

PAYEE: BBN SYSTEMS & TECHNOLOGIES
DIV BOLT BERANEK & NEWMAN INC
P.O. BOX 4340
BOSTON MA 02211

CHECK AMT $$ 1084.05

CHECK NO.: ON US TREASURY DATE:

AFZS-DKO-I

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

US DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION DEFENSE ACCOUNTING OFFICE BLDG 41408 BOYD STREET ATTN: DFAS-IN/EM-TPD FT HUACHUCA, AZ 85635-6000	DTE VOU PREP 96/05/29 CONTRACT NO AND DATE DABT63-94C0017 REQUISITION NO & DATE	SCHEDULE NUM PAID BY DAN BLIZNIK FORT HUACHUCA,AZ 96/05/29 6424	VOUCHER NUM 219022

PAYEE'S NAME AND ADDRESS: BBN SYSTEMS & TECHNOLOGIES
DIV BOLT BERANEK & NEWMAN I
P.O. BOX 4340
BOSTON MA 02211

DISCOUNT TERMS

INVOICE NO	INT/(DISC) AMT	LATE/TERMS	RATE
20C	0.00	0	0.0000%

NUM & DT ORD	ARTICLES OR SERVICES	QTY ISS	UNIT PRICE	AMOUNT
000001		1.00 LO	1084.0500	1084.05

961500826 14CAPS

TOTAL 1084.05

PAYMENT
_ PROVISIONAL
_ COMPLETE
X PARTIAL
_ FINAL
_ PROGRESS
_ ADVANCE

APPROVED BY

BY

TITLE

EXCHANGE RATE =$1.00

DIFF

AMT VER CORRECT 1084.05

SIGNATURE OR INITIALS: VE: 76 PMT NO: 025

AUT-CER: TACKETT

PPA: 76

I CERTIFY THIS VOUCHER CORRECT AND PROPER FOR CHECK PAYMENT

96/05/29 DAN BLIZNIK — FORT HUACHUCA DEFENSE ACCOUNTING OFFICER

DATE — AUTHORIZED CERTIFYING OFFICER — TITLE

CHECK NUMBER 02587358

SF 1034

ACCOUNTING CLASSIFICATION

9750400.1301 00-5005 P5T10A8 2581 002086 US JWBL00 00JWBL HJ150043480535
ACCOUNTING AMOUNT: 1084.05

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

US DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION DEFENSE ACCOUNTING OFFICE BLDG 41408 BOYD STREET ATTN: DFAS-IN/EM-TPD FT HUACHUCA, AZ 85635-6000	DTE VOU PREP 96/05/29 CONTRACT NO AND DATE DABT63-94C0017 REQUISITION NO & DATE	SCHEDULE NUM 	VOUCHER NUM 219022 PAID BY DAN BLIZNIK FORT HUACHUCA,AZ 96/05/29 6424

PAYEE'S NAME AND ADDRESS: BBN SYSTEMS & TECHNOLOGIES
DIV BOLT BERANEK & NEWMAN I
P.O. BOX 4340
BOSTON MA 02211

DISCOUNT TERMS

INVOICE NO	INT/(DISC) AMT	LATE/TERMS	RATE
20C	0.00	0	0.0000%

NUM & DT ORD	ARTICLES OR SERVICES	QTY	UNIT ISS	PRICE	AMOUNT
000001		1.00	LO	1084.0500	1084.05

961500826 14CAPS

TOTAL 1084.05

PAYMENT
_ PROVISIONAL
_ COMPLETE
X PARTIAL
_ FINAL
_ PROGRESS
_ ADVANCE

APPROVED BY

BY

TITLE

EXCHANGE RATE DIFF
=$1.00

AMT VER CORRECT 1084.05

SIGNATURE OR INITIALS: VE: 76 PMT NO: 025

AUT-CER: TACKETT

PPA: 76

I CERTIFY THIS VOUCHER CORRECT AND PROPER FOR CHECK PAYMENT

96/05/29 DAN BLIZNIK — FORT HUACHUCA DEFENSE ACCOUNTING OFFICER

DATE — AUTHORIZED CERTIFYING OFFICER — TITLE

CHECK NUMBER 02587358

SF 1034

ACCOUNTING CLASSIFICATION

9750400.1301 00-5005 P5T10A8 2581 002086 US JWBL00 00JWBL HJ150043480535
ACCOUNTING AMOUNT: 1084.05

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

US DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION DEFENSE ACCOUNTING OFFICE DFAS-IN/EM-TP FORT HUACHUCA, AZ	DTE VOU PREP 95/06/09 CONTRACT NO AND DATE DABT63-94C0017 REQUISITION NO & DATE	SCHEDULE NUM VOUCHER NUM 221920 PAID BY M.E. BELZA, MAJ,FC FORT HUACHUCA 95/06/09 6424

PAYEE'S NAME AND ADDRESS: BBN SYSTEMS & TECHNOLOGIES
DIV BOLT BERANEK & NEWMAN I
P.O. BOX 4340
BOSTON MA 02211

DISCOUNT TERMS

INVOICE NO	INT/(DISC) AMT	LATE/TERMS	RATE
12C	0.00	0	0.0000%

NUM & DT ORD	ARTICLES OR SERVICES	QTY ISS	UNIT PRICE	AMOUNT
000001		1.00	38283.5300	38283.

95160082410CAPS TOTAL 38283

PAYMENT
_ PROVISIONAL
_ COMPLETE
X PARTIAL
_ FINAL
_ PROGRESS
_ ADVANCE

APPROVED BY
BY
TITLE

EXCHANGE RATE =$1.00
DIFF

AMT VER CORRECT 38283

SIGNATURE OR INITIALS: VE: 73 PMT NO: 016

AUT-CER: PALMER PPA: 73

I CERTIFY THIS VOUCHER CORRECT AND PROPER FOR CHECK PAYMENT
95/06/09 M.E. BELZA DEFENSE ACCOUNTING OFFICER

DATE AUTHORIZED CERTIFYING OFFICER TITLE

CHECK NUMBER 02521758

SF 1034

SF 1034 (CONTINUED) VOUCHER NUMBER: 221920 PAGE:

ACCOUNTING CLASSIFICATION

9740400.1301 00-5005 P4T10A8 2594 002086 US JWC900 00JWC9 HJ150040060552
ACCOUNTING AMOUNT: 38283.53

SF 1034-EDP PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

DEPARTMENT OF THE ARMY
DRAWER P
FT HUACHUCA, AZ 85613-6000

VOUCHER NO.

DATE PREPARED 06/08/95

CONTRACT NO./DATE DABT63-94-C-0017 04/05/94

P A I D B Y
Account of:
DSSN 6424

TAX ID
PAYEE'S NAME BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
ADDRESS P.O BX 4340
BOSTON MA 02211

FT HUACHUCA, AZ 85613-6000

DATE INVOICE RECV'D 05/15/95 FOB:
DISCOUNT TERMS NET 25 DAYS DEST

NO./DATE OF ORDER	INV DATE	DATE OF PERFORMANCE INVRCV'D	MDSE DEL	MDSE ACPT	FREIGHT	MERCHANDISE
12C	04/10/95	05/15/95	05/01/95	05/01/95	0.00	38283.

TOTAL: MDSE+ 38283.

AMOUNT VERIFIED CORRECT FOR $$ 38283.
SIGNATURE OR INITIALS: 73/

PAYMENT: 16PARTIAL 06/09/95

PURSUANT TO THE AUTHORITY VESTED IN ME, I CERTIFY THAT THIS VOUCHER IS CORRECT AND PROPER FOR PAYMENT.

AUTHORIZED CERTIFYING OFFICER DATE: 06/08/95
FOR: For M.E.BELZA, MAJOR
DEFENSE ACCOUNTING OFFICER
Finance and Accounting Officer

ACCOUNTING CLASSIFICATIONS
9740400130100050O5P4T10A64104 2594 S02086 US JWC900 00JWC9 HJ150040060552 38283.

PAYEE: BBN SYSTEMS & TECHNOLOGIES
DIV BOLT BERANEK & NEWMAN INC
P.O. BOX 4340
BOSTON MA 02211

CHECK AMT $$ 38283.

CHECK NO.: ON US TREASURY DATE:

Standard Form 1034
Revised January 1980
Department of the Treasury
I TFRM 4-2000
1034-120

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

VOUCHER NO. 12C

U.S. DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION	DATE VOUCHER PREPARED	SCHEDULE NO.
D.C.A.A. WALTHAM BRANCH 424 TRAPELLO RD WALTHAM, MA 02154-6397	10 April 1995 CONTRACT NUMBER AND DATE DABT63-94-C-0017 REQUISITION NUMBER AND DATE	951529 PAID BY

PAYEE'S NAME AND ADDRESS

BBN SYSTEMS AND TECHNOLOGIES
A Division of Bolt Beranek & Newman, Inc.
P.O. BOX 4340
BOSTON, MA 02211

Point of contact: John Freyermuth @ (617) 873-3716

DATE INVOICE RECEIVED

DISCOUNT TERMS

PAYEE'S ACCOUNT NUMBER 11592 1.1/10186

SHIPPED FROM | TO | WEIGHT | GOVERNMENT B/L NUMBER

NUMBER AND DATE OF ORDER	DATE OF DELIVERY OR SERVICE	ARTICLES OR SERVICES (Enter description, item number of contract or Federal supply schedule, and other information deemed necessary)	QUANTITY	UNIT PRICE COST	UNIT PRICE PER	AMOUNT (1)
	01 Apr thru 30 Apr 1995	For detail, see SF 1035 continuation sheet. Total amount claimed transferred from Page 2, SF 1035 COST REIMBURSABLE PROVISIONAL PAYMENT				$38,283.53

(Use continuation sheet(s) if necessary) **(Payee must NOT use the space below)** TOTAL $38,283.53

PAYMENT
- ☐ PROVISIONAL
- ☐ COMPLETE
- ☐ PARTIAL
- ☐ FINAL
- ☐ PROGRESS
- ☐ ADVANCE

APPROVED FOR Provisional Payment Subject to Later Audit

EXCHANGE RATE = $1.00

BY [2] John F.Gay

TITLE Auditor, Defense Contract Audit Agency

DIFFERENCES

Amount verified; correct for

(Signature or initials)

Pursuant to authority vested in me, I certify that this voucher is correct and proper for payment.

(Date) (Authorized Certifying Officer)[2] (Title)

ACCOUNTING CLASSIFICATION

PAID BY

CHECK NUMBER	ON ACCOUNT OF U.S. TREASURY	CHECK NUMBER	ON (Name of bank)
CASH $	DATE	PAYEE [3]	

[1] When stated in foreign currency, insert name of currency.
[2] If the ability to certify and authority to approve are combined in one person, one signature only is necessary; otherwise the approving officer will sign in the space provided, over his official title.
[3] When a voucher is receipted in the name of a company or corporation, the name of the person writing the company or corporate name, as well as the capacity in which he signs, must appear. For example: "John Doe Company, per John Smith, Secretary", or "Treasurer", as the case may be.

PER

TITLE

Previous edition usable

★U.S.GPO:1987-0-181-247/40205

NSN 7540-00-634-4206

PK

PRIVACY ACT STATEMENT
The information requested on this form is required under the provisions of 31 U.S.C. 82b and 82c, for the purpose of disbursing Federal money. The information requested is to identify the particular creditor and the amounts to be paid. Failure to furnish this information will hinder discharge of the payment obligation.

Standard Form 1034
Revised January 1980
Department of the Treasury
1 TFRM 4-2000
1034-120

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

VOUCHER NO. 12C

U.S. DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION
D.C.A.A.
WALTHAM BRANCH
424 TRAPELLO RD
WALTHAM, MA 02154-6397

DATE VOUCHER PREPARED: 10 April 1995

SCHEDULE NO.: 951529

CONTRACT NUMBER AND DATE: DABT63-94-C-0017

REQUISITION NUMBER AND DATE:

PAID BY:

PAYEE'S NAME AND ADDRESS

BBN SYSTEMS AND TECHNOLOGIES
A Division of Bolt Beranek & Newman, Inc.
P.O. BOX 4340
BOSTON, MA 02211

Point of contact: John Freyermuth @ (617) 873-3716

DATE INVOICE RECEIVED:

DISCOUNT TERMS:

PAYEE'S ACCOUNT NUMBER: 11592 1.1/10186

SHIPPED FROM | TO | WEIGHT | GOVERNMENT B/L NUMBER

NUMBER AND DATE OF ORDER	DATE OF DELIVERY OR SERVICE	ARTICLES OR SERVICES (Enter description, item number of contract or Federal supply schedule, and other information deemed necessary)	QUANTITY	UNIT PRICE COST	UNIT PRICE PER	AMOUNT (1)
	01 Apr thru 30 Apr 1995	For detail, see SF 1035 continuation sheet. Total amount claimed transferred from Page 2, SF 1035 COST REIMBURSABLE PROVISIONAL PAYMENT				$38,283.53

(Use continuation sheet(s) if necessary) **(Payee must NOT use the space below)** TOTAL $38,283.53

PAYMENT:
- ☐ PROVISIONAL
- ☐ COMPLETE
- ☐ PARTIAL
- ☐ FINAL
- ☐ PROGRESS
- ☐ ADVANCE

APPROVED FOR: Provisional Payment Subject to Later Audit

EXCHANGE RATE = $1.00

DIFFERENCES

BY [2]: John F.Gay

Amount verified; correct for

TITLE: Auditor, Defense Contract Audit Agency

(Signature or initials)

Pursuant to authority vested in me, I certify that this voucher is correct and proper for payment.

(Date) (Authorized Certifying Officer)[2] (Title)

ACCOUNTING CLASSIFICATION

PAID BY

CHECK NUMBER | ON ACCOUNT OF U.S. TREASURY | CHECK NUMBER | ON (Name of bank)

CASH $ | DATE | PAYEE [3]

[1] When stated in foreign currency, insert name of currency.
[2] If the ability to certify and authority to approve are combined in one person, one signature only is necessary; otherwise the approving officer will sign in the space provided, over his official title.
[3] When a voucher is receipted in the name of a company or corporation, the name of the person writing the company or corporate name, as well as the capacity in which he signs, must appear. For example: "John Doe Company, per John Smith, Secretary", or "Treasurer", as the case may be.

PER

TITLE

Previous edition usable

★U.S.GPO:1987-0-181-247/40205

NSN 7540-00-634-4206

PK

PRIVACY ACT STATEMENT
The information requested on this form is required under the provisions of 31 U.S.C. 82b and 82c, for the purpose of disbursing Federal money. The information requested is to identify the particular creditor and the amounts to be paid. Failure to furnish this information will hinder discharge of the payment obligation.

FORM 1035

CONTRACT NO. # DABT63-94-C-0017

BBN REF. # 11592 1.1
BBN INVOICE # 951529
SHEET NO. # 2 OF 3
VOUCHER #12C

BBN Systems and Technologies
A Division of Bolt Beranek and Newman, Inc.
P.O. Box 4340
Boston, MA 02211

Target/Estimated Cost	$634,557.00
Target/Fixed Fee	50,524.00
Total	$685,081.00
85% Fixed Fee	$42,945.40

Disbursing Office: Defense Finance & Accounting SVC
Defense Accounting Office
Drawer P
Fort Huachuca, AZ 85613-6000

Withholding Clause:

BBN Withholding:

Analysis of Current and Cumulative Costs and Fee Earned:

Major Cost Elements:	Amount for Current Period Billed	Cumulative Amounts From Inception to Date of This Billing
Direct Labor	$11,108.72	$159,084.52
Overhead	12,808.33	184,425.01
Travel	(150.00)	1,375.60
Material	1,544.08	10,688.00
Procurement Charge	267.36	746.47
Equipment/Software Rental	0.00	704.50
Computer Services	2,067.45	24,928.66
Books & Subscriptions	0.00	30.00
Subcontractors - Company	3,803.10	3,863.10
Postage & Express Mail	19.25	37.85
Training Conference	0.00	150.00
General Administration	6,629.89	93,638.98
Total Cost	$38,098.18	$479,672.69
CAS414	185.35	2,562.05
TOTAL	$38,283.53	$482,234.74

Continuation Sheet - Page # 3
BBN Reference # 11592 1.1
VOUCHER #12C
BBN INVOICE # 951529

Direct Labor:

FY	Pool	Hours	Direct Labor	Overhead	Overhead Rate	G&A	G&A Rate
95	10.0	255.5	$11,108.72	$12,808.33	115.3%	$6,074.95	25.4%

Other Direct Costs:

Value Added Costs:

FY	Pool	Direct Costs			
95	0	$2,184.81		554.94	25.4%
			Total G&A	$6,629.89	

Non Value Added Costs:

FY	Direct Costs
95	$5,366.43

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

US DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION DEFENSE ACCOUNTING OFFICE DFAS-IN/EM-TP FORT HUACHUCA, AZ	DTE VOU PREP SCHEDULE NUM 95/07/17 CONTRACT NO AND DATE DABT63-94C0017 REQUISITION NO & DATE	VOUCHER NUM 225186 PAID BY M.E. BELZA, MAJ,FC FORT HUACHUCA 95/07/17 6424

PAYEE'S NAME AND ADDRESS: BBN SYSTEMS & TECHNOLOGIES
DIV BOLT BERANEK & NEWMAN I
P.O. BOX 4340
BOSTON MA 02211

DISCOUNT TERMS

INVOICE NO	INT/(DISC) AMT	LATE/TERMS	RATE
13C	21.46	3	8.3750%
13F	0.00	0	0.0000%

NUM & DT ORD	ARTICLES OR SERVICES	QTY ISS	UNIT PRICE	AMOUNT
000001		1.00	43620.0400	43620.04

95198104624CAPS

TOTAL 43620.04

PAYMENT
_ PROVISIONAL
_ COMPLETE
X PARTIAL
_ FINAL
_ PROGRESS
_ ADVANCE

APPROVED BY

EXCHANGE RATE =$1.00

DIFF 21.46

BY

TITLE

AMT VER CORRECT 43641.50

SIGNATURE OR INITIALS: VE: 84 PMT NO: 017

AUT-CER: KNIEFEL

PPA: 84

I CERTIFY THIS VOUCHER CORRECT AND PROPER FOR CHECK PAYMENT
95/07/17 M.E. BELZA DEFENSE ACCOUNTING OFFICER

DATE AUTHORIZED CERTIFYING OFFICER TITLE

CHECK NUMBER 02530282

SF 1034

ACCOUNTING CLASSIFICATION

9740400.1301 00-5005 P4T10A8 2594 002086 US JWC900 00JWC9 HJ150040060552
ACCOUNTING AMOUNT: 43620.04
97X4930.5L40 00-0000 P000000 43AG 033181 US 14TT00 0014TT 4C0017DFASDA0
ACCOUNTING AMOUNT: 21.46

SF 1034-EDP PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

DEFENSE FINANCE AND ACCOUNTING
DRAWER P
FT HUACHUCA, AZ 85613-6000

VOUCHER NO.

DATE PREPARED 07/15/95

CONTRACT NO./DATE DABT63-94-C-0017 04/05/94

P A I D B Y
Account of:
DSSN 6424

TAX ID
PAYEE'S NAME BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
ADDRESS P.O BX 4340
BOSTON MA 02211

FT HUACHUCA, AZ 85613-6000

DATE INVOICE RECV'D 06/14/95
DISCOUNT TERMS NET 30 DAYS

FOB:
DEST

NO./DATE OF ORDER	INV DATE	DATE OF PERFORMANCE INVRCV'D	MDSE DEL	MDSE ACPT	FREIGHT	MERCHANDISE
13C	06/09/95	06/14/95	06/14/95	06/14/95	0.00	40403.11
13F	06/09/95	06/19/95	06/19/95	06/19/95	0.00	3216.93

TOTAL: MDSE+ 43620.04

INT+ 21.46

AMOUNT VERIFIED CORRECT FOR $$ 43641.50
SIGNATURE OR INITIALS: 84/

PAYMENT: 17PARTIAL 07/14/95

PURSUANT TO THE AUTHORITY VESTED IN ME, I CERTIFY THAT THIS VOUCHER IS CORRECT AND PROPER FOR PAYMENT.

AUTHORIZED CERTIFYING OFFICER DATE: 07/15/95
FOR: For M.E.BELZA, MAJOR
DEFENSE ACCOUNTING OFFICER
DEFENSE ACCOUNTING OFFICER

ACCOUNTING CLASSIFICATIONS

9740400130100050O5P4T10A64104	2594	S02086	US	JWC900	00JWC9	HJ150040060552	43620.04
97X4930.5L4000000000000000000	43AG	S33181	US	14TT00	0014TT	4C0017DFASDA0	21.46

PAYEE: BBN SYSTEMS & TECHNOLOGIES
DIV BOLT BERANEK & NEWMAN INC
P.O. BOX 4340
BOSTON MA 02211

CHECK AMT $$ 43641.50

CHECK NO.: ON US TREASURY DATE:

Standard Form 1034
Revised January 1980
Department of the Treasury
1 TFRM 4-2000
1034-120

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

VOUCHER NO. 13C

U.S. DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION
D.C.A.A.
WALTHAM BRANCH
424 TRAPELLO RD
WALTHAM, MA 02154-6397

DATE VOUCHER PREPARED: 09 June 1995
CONTRACT NUMBER AND DATE: DABT63-94-C-0017
REQUISITION NUMBER AND DATE:

SCHEDULE NO. 951688
PAID BY

PAYEE'S NAME AND ADDRESS
BBN SYSTEMS AND TECHNOLOGIES
A Division of Bolt Beranek & Newman, Inc.
P.O. BOX 4340
BOSTON, MA 02211
Point of contact: John Freyermuth @ (617) 873-3716

DATE INVOICE RECEIVED
DISCOUNT TERMS
PAYEE'S ACCOUNT NUMBER 11592 .1.1/10186

SHIPPED FROM | TO | WEIGHT | GOVERNMENT B/L NUMBER

NUMBER AND DATE OF ORDER	DATE OF DELIVERY OR SERVICE	ARTICLES OR SERVICES (Enter description, item number of contract or Federal supply schedule, and other information deemed necessary)	QUANTITY	UNIT PRICE COST	UNIT PRICE PER	AMOUNT (1)
	01 May thru 31 May 1995	For detail, see SF 1035 continuation sheet. Total amount claimed transferred from Page 2, SF 1035 COST REIMBURSABLE PROVISIONAL PAYMENT				$40,403.11

(Use continuation sheet(s) if necessary) **(Payee must NOT use the space below)** TOTAL $40,403.11

PAYMENT:
- ☐ PROVISIONAL
- ☐ COMPLETE
- ☐ PARTIAL
- ☐ FINAL
- ☐ PROGRESS
- ☐ ADVANCE

APPROVED FOR: Provisional Payment Subject to Later Audit
EXCHANGE RATE = $1.00
BY [2]: John F.Gay
TITLE: Auditor, Defense Contract Audit Agency

DIFFERENCES
Amount verified; correct for
(Signature or initials)

Pursuant to authority vested in me, I certify that this voucher is correct and proper for payment.

(Date) (Authorized Certifying Officer)[2] (Title)

ACCOUNTING CLASSIFICATION

PAID BY

CHECK NUMBER	ON ACCOUNT OF U.S. TREASURY	CHECK NUMBER	ON (Name of bank)
CASH $	DATE	PAYEE [3]	

[1] When stated in foreign currency, insert name of currency.
[2] If the ability to certify and authority to approve are combined in one person, one signature only is necessary; otherwise the approving officer will sign in the space provided, over his official title.
[3] When a voucher is receipted in the name of a company or corporation, the name of the person writing the company or corporate name, as well as the capacity in which he signs, must appear. For example: "John Doe Company, per John Smith, Secretary", or "Treasurer", as the case may be.

PER
TITLE

Previous edition usable
*U.S.GPO:1987-0-181-247/40205
NSN 7540-00-634-4206

PK

PRIVACY ACT STATEMENT
The information requested on this form is required under the provisions of 31 U.S.C. 82b and 82c, for the purpose of disbursing Federal money. The information requested is to identify the particular creditor and the amounts to be paid. Failure to furnish this information will hinder discharge of the payment obligation.

Standard Form 1034
Revised January 1980
Department of the Treasury
1 TFRM 4-2000
1034-120

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

VOUCHER NO. 13F

U.S. DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION
Defense Finance & Accounting SVC
Defense Accounting Office
Drawer P
Fort Huachuca, AZ 85613-6000

DATE VOUCHER PREPARED: 09 June 1995

CONTRACT NUMBER AND DATE: DABT63-94-C-0017

REQUISITION NUMBER AND DATE:

SCHEDULE NO. 951688

PAID BY

PAYEE'S NAME AND ADDRESS

BBN SYSTEMS AND TECHNOLOGIES
A Division of Bolt Beranek & Newman, Inc.
P.O. BOX 4340
BOSTON, MA 02211

Point of contact: John Freyermuth @ (617) 873-3716

DATE INVOICE RECEIVED

DISCOUNT TERMS: 11592 1.1/10186

PAYEE'S ACCOUNT NUMBER

SHIPPED FROM | TO | WEIGHT | GOVERNMENT B/L NUMBER

NUMBER AND DATE OF ORDER	DATE OF DELIVERY OR SERVICE	ARTICLES OR SERVICES (Enter description, item number of contract or Federal supply schedule, and other information deemed necessary)	QUANTITY	UNIT PRICE COST	UNIT PRICE PER	AMOUNT (1)
	01 May thru 31 May 1995	Total Fee for 01 May thru 31 May, 1995				
		Based on 82% completion X $50,524.00				$41,612.90
		Less Total Fee invoiced to date				38,395.97
		Total Amount Due This Invoice				$3,216.93
		COST REIMBURSABLE PROVISIONAL PAYMENT				

APPROVED FOR PAYMENT: $ 3216.93
I certify acceptance of the Supplies or Service herein on 19 Jun 95
Contracting Officer — Date

(Use continuation sheet(s) if necessary) (Payee must NOT use the space below.) TOTAL

PAYMENT:
- ☐ PROVISIONAL
- ☐ COMPLETE
- ☐ PARTIAL
- ☐ FINAL
- ☐ PROGRESS
- ☐ ADVANCE

APPROVED FOR = $ Provisional Payment Subject to Later Audit

EXCHANGE RATE = $1.00

DIFFERENCES

BY [2]

TITLE

Amount verified; correct for

(Signature or initials)

Pursuant to authority vested in me, I certify that this voucher is correct and proper for payment.

(Date) (Authorized Certifying Officer)[2] (Title)

ACCOUNTING CLASSIFICATION

PAID BY

CHECK NUMBER | ON ACCOUNT OF U.S. TREASURY | CHECK NUMBER | ON (Name of bank)

CASH $ | DATE | PAYEE [3]

[1] When stated in foreign currency, insert name of currency.
[2] If the ability to certify and authority to approve are combined in one person, one signature only is necessary; otherwise the approving officer will sign in the space provided, over his official title.
[3] When a voucher is receipted in the name of a company or corporation, the name of the person writing the company or corporate name, as well as the capacity in which he signs, must appear. For example: "John Doe Company, per John Smith, Secretary", or "Treasurer", as the case may be.

PER

TITLE

Previous edition usable

★U.S.GPO:1987-0-181-247/40205

NSN 7540-00-634-4206

PRIVACY ACT STATEMENT
The information requested on this form is required under the provisions of 31 U.S.C. 82b and 82c, for the purpose of disbursing Federal money. The information requested is to identify the particular creditor and the amounts to be paid. Failure to furnish this information will hinder discharge of the payment obligation.

PK

FORM 1035

CONTRACT NO. # DABT63-94-C-0017

BBN REF. # 11592 1.1
BBN INVOICE # 951688
SHEET NO. # 2 of 2
VOUCHER #13F

BBN Systems and Technologies
A Division of Bolt Beranek and Newman, Inc.
P.O. Box 4340
Boston, MA 02211

Target/Estimated Cost	$634,557.00
Target/Fixed Fee	50,524.00
Total	$685,081.00
85% Fixed Fee	$42,945.40

Disbursing Office: Defense Finance & Accounting SVC
Defense Accounting Office
Drawer P
Fort Huachuca, AZ 85613-6000

Fixed Fee:

Fixed Fee Due (82% X $50,524.00)	$41,612.90
Less Fixed Fee Billed	38,395.97
Fixed Fee To Be Billed	$3,216.93

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

US DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION DEFENSE ACCOUNTING OFFICE DFAS-IN/EM-TP FORT HUACHUCA, AZ	DTE VOU PREP 95/08/23 CONTRACT NO AND DATE DABT63-94C0017 REQUISITION NO & DATE	SCHEDULE NUM VOUCHER NUM 228868 PAID BY M.E. BELZA, MAJ,FC FORT HUACHUCA 95/08/23 6424

PAYEE'S NAME AND ADDRESS: BBN SYSTEMS & TECHNOLOGIES
DIV BOLT BERANEK & NEWMAN I
P.O. BOX 4340
BOSTON MA 02211

DISCOUNT TERMS

INVOICE NO	INT/(DISC) AMT	LATE/TERMS	RATE
14C	0.00	0	0.0000%

NUM & DT ORD	ARTICLES OR SERVICES	QTY ISS	UNIT PRICE	AMOUNT
000001		1.00	38406.1600	38406.

95235081946CAPS

TOTAL 38406.

PAYMENT
_ PROVISIONAL
_ COMPLETE
X PARTIAL
_ FINAL
_ PROGRESS
_ ADVANCE

APPROVED BY

BY

TITLE

EXCHANGE RATE =$1.00

DIFF

AMT VER CORRECT 38406.

SIGNATURE OR INITIALS: VE: 73 PMT NO: 018

AUT-CER: PALMER

PPA: 73

I CERTIFY THIS VOUCHER CORRECT AND PROPER FOR CHECK PAYMENT
95/08/23 M.E. BELZA DEFENSE ACCOUNTING OFFICER

DATE AUTHORIZED CERTIFYING OFFICER TITLE

CHECK NUMBER 02539689

SF 1034

SF 1034 (CONTINUED) VOUCHER NUMBER: 228868 PAGE: 2

ACCOUNTING CLASSIFICATION

9740400.1301 00-5005 P4T10A8 2594 002086 US JWC900 00JWC9 HJ1500400600552
ACCOUNTING AMOUNT: 38406.16

SF 1034-EDP PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

DEFENSE FINANCE AND ACCOUNTING
DRAWER P
FT HUACHUCA, AZ 85613-6000

VOUCHER NO.

DATE PREPARED 08/22/95

CONTRACT NO./DATE DABT63-94-C-0017 04/05/94

PAID BY
Account of:
DSSN 6424

TAX ID
PAYEE'S NAME BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
ADDRESS P.O BX 4340
BOSTON MA 02211

FT HUACHUCA, AZ 85613-6000

DATE INVOICE RECV'D 07/30/95
DISCOUNT TERMS NET 30 DAYS

FOB:
DEST

NO./DATE OF ORDER	INV DATE	DATE OF PERFORMANCE INVRCV'D	MDSE DEL	MDSE ACPT	FREIGHT	MERCHANDI
14C	07/25/95	07/30/95	07/30/95	07/30/95	0.00	3840

TOTAL: MDSE+ 3840

AMOUNT VERIFIED CORRECT FOR $$ 38406
SIGNATURE OR INITIALS: 73/

PAYMENT: 1SPARTIAL 08/29/95

PURSUANT TO THE AUTHORITY VESTED IN ME, I CERTIFY THAT THIS VOUCHER IS CORREC AND PROPER FOR PAYMENT.

AUTHORIZED CERTIFYING OFFICER DATE: 08/22/95
FOR: For M.E.BELZA
MAJ, FC
DEFENSE ACCOUNTING OFFICER

ACCOUNTING CLASSIFICATIONS
97404001301000500SP4T10A64104 2594 S02086 US JWC900 00JWC9 HJ150040060552 3840

PAYEE: BBN SYSTEMS & TECHNOLOGIES
DIV BOLT BERANEK & NEWMAN INC
P.O. BOX 4340
BOSTON MA 02211

CHECK AMT $$ 38406

CHECK NO.: ON US TREASURY DATE:

Standard Form 1034
Revised January 1980
Department of the Treasury
1 TFRM 4-2000
1034-120

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

VOUCHER NO. 14C

U.S. DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION
D.C.A.A.
WALTHAM BRANCH
424 TRAPELLO RD
WALTHAM, MA 02154-6397

DATE VOUCHER PREPARED: 25 July 1995
CONTRACT NUMBER AND DATE: DABT63-94-C-0017
REQUISITION NUMBER AND DATE:
SCHEDULE NO. 960088
PAID BY

PAYEE'S NAME AND ADDRESS
BBN SYSTEMS AND TECHNOLOGIES
A Division of Bolt Beranek & Newman, Inc.
P.O. BOX 4340
BOSTON, MA 02211
Point of contact: John Freyermuth @ (617) 873-3716

DATE INVOICE RECEIVED
DISCOUNT TERMS
PAYEE'S ACCOUNT NUMBER 11592 1.1/10186
SHIPPED FROM TO WEIGHT
GOVERNMENT B/L NUMBER

NUMBER AND DATE OF ORDER	DATE OF DELIVERY OR SERVICE	ARTICLES OR SERVICES (Enter description, item number of contract or Federal supply schedule, and other information deemed necessary)	QUANTITY	UNIT PRICE COST	UNIT PRICE PER	AMOUNT (1)
	01 Jun thru 30 Jun 1995	For detail, see SF 1035 continuation sheet. Total amount claimed transferred from Page 2, SF 1035 COST REIMBURSABLE PROVISIONAL PAYMENT				$38,406.16

(Use continuation sheet(s) if necessary) (Payee must NOT use the space below) TOTAL $38,406.16

PAYMENT:
- ☐ PROVISIONAL
- ☐ COMPLETE
- ☐ PARTIAL
- ☐ FINAL
- ☑ PROGRESS
- ☐ ADVANCE

APPROVED FOR: Provisional Payment Subject to Later Audit
EXCHANGE RATE: 1. = $1.00
DIFFERENCES
BY [2]: John F.Gay
Amount verified; correct for
TITLE: Auditor, Defense Contract Audit Agency
(Signature or initials)

Pursuant to authority vested in me, I certify that this voucher is correct and proper for payment.

(Date) (Authorized Certifying Officer)[2] (Title)

ACCOUNTING CLASSIFICATION

PAID BY

CHECK NUMBER	ON ACCOUNT OF U.S. TREASURY	CHECK NUMBER	ON (Name of bank)
CASH $	DATE	PAYEE [3]	

[1] When stated in foreign currency, insert name of currency.
[2] If the ability to certify and authority to approve are combined in one person, one signature only is necessary; otherwise the approving officer will sign in the space provided, over his official title.
[3] When a voucher is receipted in the name of a company or corporation, the name of the person writing the company or corporate name, as well as the capacity in which he signs, must appear. For example: "John Doe Company, per John Smith, Secretary", or "Treasurer", as the case may be.

PER
TITLE

Previous edition usable
★U.S.GPO:1987-0-181-247/40205
NSN 7540-00-634-4206

PK

PRIVACY ACT STATEMENT
The information requested on this form is required under the provisions of 31 U.S.C. 82b and 82c, for the purpose of disbursing Federal money. The information requested is to identify the particular creditor and the amounts to be paid. Failure to furnish this information will hinder discharge of the payment obligation.

FORM 1035

CONTRACT NO. # DABT63-94-C-0017

BBN REF. # 11592 1.1
BBN INVOICE # 960088
SHEET NO. # 2 OF 3
VOUCHER #14C

BBN Systems and Technologies
A Division of Bolt Beranek and Newman, Inc.
P.O. Box 4340
Boston, MA 02211

Target/Estimated Cost	$634,557.00
Target/Fixed Fee	50,524.00
Total	$685,081.00
85% Fixed Fee	$42,945.40

Disbursing Office: Defense Finance & Accounting SVC
Defense Accounting Office
Drawer P
Fort Huachuca, AZ 85613-6000

Withholding Clause:

BBN Withholding:

Analysis of Current and Cumulative Costs and Fee Earned:

Major Cost Elements:	Amount for Current Period Billed	Cumulative Amounts From Inception to Date of This Billing
Direct Labor	$13,265.52	$187,082.28
Overhead	20,960.85	222,372.12
Travel	0.00	1,375.60
Material	214.14	11,047.26
Procurement Charge	8.56	625.75
Equipment/Software Rental	0.00	704.50
Computer Services	2,144.21	27,429.87
Books & Subscriptions	0.00	30.00
Subcontractors - Company	0.00	3,863.10
Material W/O Procurement	25.00	25.00
Postage & Express Mail	9.00	46.85
Training Conference	0.00	150.00
General Administration	1,557.50	103,310.79
Total Cost	$38,184.78	$558,063.12
CAS414	221.38	2,980.89
TOTAL	$38,406.16	$561,044.01

Continuation Sheet - Page # 3
BBN Reference # 11592 1.1
VOUCHER #14C
BBN INVOICE # 960088

Direct Labor:

FY	Pool	Hours	Direct Labor	Overhead	Overhead Rate	G&A	G&A Rate
95	10	320.5	$13,265.52	$15,732.91	118.6%	$6,814.63	23.5%
			0.00	5,227.94 *		(5,252.04) *	
			$13,265.52	$20,960.85			

Other Direct Costs:

Value Added Costs:

FY	Pool	Direct Costs		
				($510.99) *
95	0	$2,152.77		505.90	23.5%
			Total G&A	$1,557.50

Non Value Added Costs:

FY	Direct Costs
95	$248.14

*Retroactive Rate Adjustment

[illegible] VOUCHER NO.

DATE PREPARED 03/06/96

[illegible] 04/05/94

PAID BY
Account of:
DSSN 6424

[illegible]
FT HUACHUCA, AZ 85613-6000

[illegible] FOB:
DEST

VENDOR	INV DATE	DATE OF PERFORMANCE INVOLV'D	MDSE DEL	MDSE ACPT	FREIGHT	MERCHANDISE
PAC	02/23/96	03-01/96	02/26/96	02/26/96	0.00	11087.12

TOTAL: MDSE+ 11087.12

APPROVED/VERIFIED CORRECT FOR ** 11087.12
SIGNATURE OR INITIALS: 95/

[illegible] 04/01/96

[illegible] I CERTIFY THAT THIS VOUCHER IS CORRECT AND PROPER FOR PAYMENT.

[illegible] DATE: 03/06/96
FOR: BAJI BLEMIK

CERTIFYING OFFICER

[illegible]
[illegible] 2594 S02085 US JWCY00 00JWCY H31500400660582 4403.25
[illegible] 2581 S02085 US JWBL00 00JWBL H31500403480555 6683.87

[illegible] CHECK AMT ** 11087.12

[illegible]
DEPOSIT TICKET # MEMBERS FCU
P.O. BOX 9340
BOSTON MA 02211

CHECK NO.: [illegible] DATE:

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

US DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION DEFENSE ACCOUNTING OFFICE BLDG 41408 BOYD STREET ATTN: DFAS-IN/EM-TPD FT HUACHUCA, AZ 85635-6000	DTE VOU PREP 96/04/01 CONTRACT NO AND DATE DABT63-94C0017 REQUISITION NO & DATE	SCHEDULE NUM VOUCHER NUM 213428 PAID BY DAN BLIZNIK FORT HUACHUCA,AZ 96/04/01 6424

PAYEE'S NAME AND ADDRESS: BBN SYSTEMS & TECHNOLOGIES
DIV BOLT BERANEK & NEWMAN I
P.O. BOX 4340
BOSTON MA 02211

DISCOUNT TERMS

INVOICE NO	INT/(DISC) AMT	LATE/TERMS	RATE
19C	0.00	0	0.0000%

NUM & DT ORD	ARTICLES OR SERVICES	QTY ISS	UNIT PRICE	AMOUNT
000001		1.00	4403.2500	4403.25
000002		1.00	6683.8700	6683.87

960670832S1CAPS TOTAL 11087.12

PAYMENT
_ PROVISIONAL
_ COMPLETE
X PARTIAL
_ FINAL
_ PROGRESS
_ ADVANCE

APPROVED BY
BY
TITLE

EXCHANGE RATE =$1.00 DIFF

AMT VER CORRECT 11087.12

SIGNATURE OR INITIALS: VE: 95 PMT NO: 024

AUT-CER: KNIEFEL PPA: 95

I CERTIFY THIS VOUCHER CORRECT AND PROPER FOR CHECK PAYMENT

96/04/01 DAN BLIZNIK FORT HUACHUCA DEFENSE ACCOUNTING OFFICER

DATE AUTHORIZED CERTIFYING OFFICER TITLE

CHECK NUMBER 02579036

SF 1034

ACCOUNTING CLASSIFICATION

9740400.1301 00-5005 P4T10A8 2594 002086 US JWC900 00JWC9 HJ150040060552
ACCOUNTING AMOUNT: 4403.25
9750400.1301 00-5005 P5T10A8 2581 002086 US JWBL00 00JWBL HJ150043480535
ACCOUNTING AMOUNT: 6683.87

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

US DEPARTMENT, BUREAU, (	DTE VOU PREP	SCHEDL NUM	VOUCHER NUM
ESTABLISHMENT AND LOCATION	95/05/22		220112
DEFENSE ACCOUNTING OFFICE	CONTRACT NO' AND DATE		PAID BY
DFAS-IN/EM-TP	DABT63-94C0017		M.E. BELZA, MAJ,FC
FORT HUACHUCA, AZ			FORT HUACHUCA
	REQUISITION NO & DATE		95/05/22
			6424

PAYEE'S NAME AND ADDRESS: BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMA
P.O BX 4340
BOSTON MA 02211

DISCOUNT TERMS

INVOICE NO	INT/(DISC) AMT	LATE/TERMS	RATE
11C	0.00	0	0.0000%
11F	0.00	0	0.0000%
5C	0.00	0	0.0000%

NUM & DT ORD	ARTICLES OR SERVICES	QTY ISS	UNIT PRICE	AMOUNT
000001		1.00	103152.6300	103152.63
000002		1.00	13818.9200	-13818.92

95142083924CAPS TOTAL 89333.71

PAYMENT
_ PROVISIONAL
_ COMPLETE
X PARTIAL
_ FINAL
_ PROGRESS
_ ADVANCE

APPROVED BY
BY
TITLE

EXCHANGE RATE DIFF
=$1.00

AMT VER CORRECT 89333.71

SIGNATURE OR INITIALS: VE: 91 PMT NO: 014

AUT-CER: PALMER PPA: 91

I CERTIFY THIS VOUCHER CORRECT AND PROPER FOR CHECK PAYMENT

95/05/22 M.E. BELZA DEFENSE ACCOUNTING OFFICER

DATE AUTHORIZED CERTIFYING OFFICER TITLE

CHECK NUMBER 02517461

SF 1034

ACCOUNTING CLASSIFICATI

9740400.1301 00-5005 P4T10A8 2594 002086 US JWC900 00JWC9 HJ150040060552
ACCOUNTING AMOUNT: 103152.63
9750400.1301 00-5005 P5T10A8 2581 002086 US JWBL00 00JWBL HJ150043480535
ACCOUNTING AMOUNT: -13818.92

SF 1034-EDP PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

DEPARTMENT OF THE ARMY
DRAWER P
FT HUACHUCA, AZ 85613-6000

VOUCHER NO.

DATE PREPARED 05/19/95

CONTRACT NO./DATE DABT63-94-C-0017 04/05/94

P A I D B Y
Account of:
DSSN 6424

TAX ID
PAYEE'S NAME BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
ADDRESS P.O BX 4340
BOSTON MA 02211

FT HUACHUCA, AZ 85613-6000

DATE INVOICE RECV'D 04/20/95
DISCOUNT TERMS NET 30 DAYS

FOB:
DEST

NO./DATE OF ORDER	INV DATE	DATE OF PERFORMANCE INVRCV'D	MDSE DEL	MDSE ACPT	FREIGHT	MERCHANDISE
11C	04/10/95	04/20/95	03/31/95	04/10/95	0.00	95545.24
11F	04/10/95	04/20/95	03/31/95	04/25/95	0.00	7607.39
5C	09/14/94	11/14/94	08/31/94	09/19/94	0.00	-13818.92

DEDUCTION TAKEN FOR DUPLICATED PAYMENTS AGAINST YOUR INVOICE NO 5C - DOV 205017 chk 02482350 dtd 12 Dec 94 9P and DOV 201241 chk 02470552 dtd 13 Oct 94 5P

TOTAL: MDSE+ 89333.71

AMOUNT VERIFIED CORRECT FOR $$ 89333.71
SIGNATURE OR INITIALS: 91/

PAYMENT: 14PARTIAL 05/22/95

PURSUANT TO THE AUTHORITY VESTED IN ME, I CERTIFY THAT THIS VOUCHER IS CORRECT AND PROPER FOR PAYMENT.

AUTHORIZED CERTIFYING OFFICER DATE: 05/19/95
FOR: For M.E.BELZA, MAJOR
DEFENSE ACCOUNTING OFFICER
Finance and Accounting Officer

ACCOUNTING CLASSIFICATIONS

97404001301000500 5P4T10A64104	2594	S02086	US	JWC900	00JWC9	HJ150040060552	103152.63
97504001301000500 5T10A8411400	2581	S02086	US	JWBL00	00JWBL	HJ150043480535	-13818.92

PAYEE: BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
P.O BX 4340
BOSTON MA 02211

CHECK AMT $$ DUP 89333.71

CHECK NO.: ON US TREASURY DATE:

Standard Form 1034
Revised January 1990
Department of the Treasury
I TFRM 4-2000
1034-120

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

VOUCHER NO. 11F

U.S. DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION
Defense Finance & Accounting SVC
Defense Accounting Office
Drawer P
Fort Huachuca, AZ 85613-6000

DATE VOUCHER PREPARED: 10 April 1995

CONTRACT NUMBER AND DATE: DABT63-94-C-0017

REQUISITION NUMBER AND DATE:

SCHEDULE NO. 951339

PAID BY

PAYEE'S NAME AND ADDRESS

BBN SYSTEMS AND TECHNOLOGIES
A Division of Bolt Beranek & Newman, Inc.
P.O. BOX 4340
BOSTON, MA 02211

Point of contact: John Freyermuth @ (617) 873-3716

DATE INVOICE RECEIVED

DISCOUNT TERMS: 11592 1.1/10186

PAYEE'S ACCOUNT NUMBER

SHIPPED FROM | TO | WEIGHT | GOVERNMENT B/L NUMBER

NUMBER AND DATE OF ORDER	DATE OF DELIVERY OR SERVICE	ARTICLES OR SERVICES (Enter description, item number of contract or Federal supply schedule, and other information deemed necessary)	QUANTITY	UNIT PRICE COST	UNIT PRICE PER	AMOUNT (1)
	16 Feb thru 31 Mar 1995	Total Fee for 16 February thru 31 March, 1995				
		Based on 70% completion X $50,524.00				$35,347.79
		Less Total Fee invoiced to date				27,740.40
		Total Amount Due This Invoice				$7,607.39
		COST REIMBURSABLE PROVISIONAL PAYMENT				

APPROVED FOR PAYMENT: $
I certify acceptance of the Supplies or Services herein
Contracting Officer
25 Apr 95
Date

(Use continuation sheet(s) if necessary) (Payee must NOT use the space below) TOTAL

PAYMENT:
- ☐ PROVISIONAL
- ☐ COMPLETE
- ☐ PARTIAL
- ☐ FINAL
- ☐ PROGRESS
- ☐ ADVANCE

APPROVED FOR: Provisional =$ Payment Subject to Later Audit

EXCHANGE RATE =$1.00

DIFFERENCES

BY [2]

TITLE

Amount verified; correct for

(Signature or initials)

Pursuant to authority vested in me, I certify that this voucher is correct and proper for payment.

(Date) (Authorized Certifying Officer)[2] (Title)

ACCOUNTING CLASSIFICATION

PAID BY

CHECK NUMBER	ON ACCOUNT OF U.S. TREASURY	CHECK NUMBER	ON (Name of bank)
CASH $	DATE	PAYEE [3]	

[1] When stated in foreign currency, insert name of currency.
[2] If the ability to certify and authority to approve are combined in one person, one signature only is necessary; otherwise the approving officer will sign in the space provided, over his official title.
[3] When a voucher is receipted in the name of a company or corporation, the name of the person writing the company or corporate name, as well as the capacity in which he signs, must appear. For example: "John Doe Company, per John Smith, Secretary", or "Treasurer", as the case may be.

PER

TITLE

Previous edition usable

*U.S.GPO:1987-0-181-247/40205

NSN 7540-00-634-4206

PRIVACY ACT STATEMENT
The information requested on this form is required under the provisions of 31 U.S.C. 82b and 82c, for the purpose of disbursing Federal money. The information requested is to identify the particular creditor and the amounts to be paid. Failure to furnish this information will hinder discharge of the payment obligation.

PK

FORM 1035

CONTRACT NO. # DBAT63-94-C-0017

BBN REF. # 11592 1.1
BBN INVOICE # 951169
SHEET NO. # 2 of 2
VOUCHER #11F

BBN Systems and Technologies
A Division of Bolt Beranek and Newman, Inc.
P.O. Box 4340
Boston, MA 02211

Target/Estimated Cost	$634,557.00
Target/Fixed Fee	50,524.00
Total	$685,081.00
85% Fixed Fee	$42,945.40

Disbursing Office: Defense Finance & Accounting SVC
Defense Accounting Office
Drawer P
Fort Huachuca, AZ 85613-6000

Fixed Fee:

Fixed Fee Due (70% X $50,524.00)	$35,347.79
Less Fixed Fee Billed	27,740.40
Fixed Fee To Be Billed	$7,607.39

Standard Form 1034
Revised January 1980
Department of the Treasury
1 TFRM 4-2000
1034-120

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

VOUCHER NO. 11C

U.S. DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION
D.C.A.A.
WALTHAM BRANCH
424 TRAPELLO RD
WALTHAM, MA 02154-6397

DATE VOUCHER PREPARED: 10 April 1995

CONTRACT NUMBER AND DATE: DABT63-94-C-0017

REQUISITION NUMBER AND DATE:

SCHEDULE NO. 951339

PAID BY

PAYEE'S NAME AND ADDRESS
BBN SYSTEMS AND TECHNOLOGIES
A Division of Bolt Beranek & Newman, Inc.
P.O. BOX 4340
BOSTON, MA 02211
Point of contact: John Freyermuth @ (617) 873-3716

DATE INVOICE RECEIVED

DISCOUNT TERMS

PAYEE'S ACCOUNT NUMBER 11592 1.1/10186

SHIPPED FROM | TO | WEIGHT | GOVERNMENT B/L NUMBER

NUMBER AND DATE OF ORDER	DATE OF DELIVERY OR SERVICE	ARTICLES OR SERVICES (Enter description, item number of contract or Federal supply schedule, and other information deemed necessary)	QUANTITY	UNIT PRICE COST	UNIT PRICE PER	AMOUNT (1)
	16 Feb thru 31 Mar 1995	For detail, see SF 1035 continuation sheet. Total amount claimed transferred from Page 2, SF 1035 COST REIMBURSABLE PROVISIONAL PAYMENT				$95,545.24

(Use continuation sheet(s) if necessary) **(Payee must NOT use the space below)** TOTAL $95,545.24

PAYMENT:
- ☐ PROVISIONAL
- ☐ COMPLETE
- ☐ PARTIAL
- ☐ FINAL
- ☐ PROGRESS
- ☐ ADVANCED

APPROVED FOR Provisional Payment Subject to Later Audit

EXCHANGE RATE = $1.00

DIFFERENCES

BY [2] John F.Gay

Amount verified; correct for

TITLE Auditor, Defense Contract Audit Agency

(Signature or initials)

Pursuant to authority vested in me, I certify that this voucher is correct and proper for payment.

(Date) (Authorized Certifying Officer)[2] (Title)

ACCOUNTING CLASSIFICATION

PAID BY

CHECK NUMBER | ON ACCOUNT OF U.S. TREASURY | CHECK NUMBER | ON (Name of bank)

CASH $ | DATE | PAYEE [3]

[1] When stated in foreign currency, insert name of currency.
[2] If the ability to certify and authority to approve are combined in one person, one signature only is necessary; otherwise the approving officer will sign in the space provided, over his official title.
[3] When a voucher is receipted in the name of a company or corporation, the name of the person writing the company or corporate name, as well as the capacity in which he signs, must appear. For example: "John Doe Company, per John Smith, Secretary", or "Treasurer", as the case may be.

PER

TITLE

Previous edition usable

*U.S.GPO:1987-0-181-247/40205

NSN 7540-00-634-4206

PK

PRIVACY ACT STATEMENT

The information requested on this form is required under the provisions of 31 U.S.C. 82b and 82c, for the purpose of disbursing Federal money. The information requested is to identify the particular creditor and the amounts to be paid. Failure [illegible] disclosure of the payment obligation.

FORM 1035

CONTRACT NO. # DABT63-94-C-0017

BBN REF. # 11592 1.1
BBN INVOICE # 951339
SHEET NO. # 2 OF 3
VOUCHER #11C

BBN Systems and Technologies
A Division of Bolt Beranek and Newman, Inc.
P.O. Box 4340
Boston, MA 02211

~~Target/Estimated Cost~~	$634,557.00
Target/Fixed Fee	50,524.00
Total	$685,081.00
85% Fixed Fee	$42,945.40

Disbursing Office: Defense Finance & Accounting SVC
Defense Accounting Office
Drawer P
Fort Huachuca, AZ 85613-6000

Withholding Clause:

BBN Withholding:

Analysis of Current and Cumulative Costs and Fee Earned:

Major Cost Elements:	Amount for Current Period Billed	Cumulative Amounts From Inception to Date of This Billing
Direct Labor	$28,944.36	$147,975.80
Overhead	33,372.78	171,616.68
Travel	0.00	1,525.60
Material	2,108.39	9,143.92
Procurement Charge	105.42	479.11
Equipment/Software Rental	0.00	704.50
Computer Services	11,596.24	22,861.21
Books & Subscriptions	0.00	30.00
Subcontractors - Company	0.00	60.00
Postage & Express Mail	9.60	18.60
Training Conference	0.00	150.00
General Administration	18,800.81	87,009.09
Total Cost	$94,937.60	$441,574.51
CAS414	607.64	2,376.70
TOTAL	$95,545.24	$443,951.21

SF 1034-EDP PUBLIC VOUC[illegible] FOR PURCHASES AND SERVIC[illegible] OTHER THAN PERSONAL

DEPARTMENT OF THE ARMY
DRAWER P
FT HUACHUCA, AZ 85613-6000

VOUCHER NO.

DATE PREPARED 05/19/95

CONTRACT NO./DATE DABT63-94-C-0017 04/05/94

P A I D B Y
Account of:

NAME DIV OF BOLT BERANEK & NEWMAN FT HUACHUCA, AZ 85613-6000
ADDRESS BBN SYSTEMS & TECHNOLOGIES
BOSTON MA 02211

DATE INVOICE RECV'D 05/16/95 FOB:
DISCOUNT TERMS NET 30 DAYS DEST

NO./DATE OF ORDER	INV DATE	DATE OF PERFORMANCE INVRCV'D	MDSE DEL	MDSE ACPT	FREIGHT	MERCHANDISE
12F	05/10/95	05/16/95	04/30/95	05/16/95	0.00	3048.18

TOTAL: MDSE+ 3048.18

AMOUNT VERIFIED CORRECT FOR $$ 3048.18
SIGNATURE OR INITIALS: 91/

PAYMENT: 1SPARTIAL 06/15/95

PURSUANT TO THE AUTHORITY VESTED IN ME, I CERTIFY THAT THIS VOUCHER IS CORRECT AND PROPER FOR PAYMENT.

AUTHORIZED CERTIFYING OFFICER DATE: 05/19/95
FOR: For M.E.BELZA, MAJOR
DEFENSE ACCOUNTING OFFICER
Finance and Accounting Officer

ACCOUNTING CLASSIFICATIONS
97404001301000500SP4T10A64104 2594 S02086 US JWC900 00JWC9 HJ150040060552 3048.18

PAYEE: BBN SYSTEMS & TECHNOLOGIES CHECK AMT $$ 3048.18
DIV BOLT BERANEK & NEWMAN INC
P.O. BOX 4340
BOSTON MA 02211

CHECK NO.: ON US TREASURY DATE:

AT2S-RMP

ACCOUNTING CLASSIFICATION

9740400.1301 00-5005 P4T10A8 2594 002086 US JWC900 00JWC9 HJ150040060562
ACCOUNTING AMOUNT: 3048.18

SF 1034-EDP PUBLIC VOUCH FOR PURCHASES AND SERVICI OTHER THAN PERSONAL

DEPARTMENT OF THE ARMY
DRAWER P
FT HUACHUCA, AZ 85613-6000

VOUCHER NO.

DATE PREPARED 06/08/95

CONTRACT NO./DATE DABT63-94-C-0017 04/05/94

P A I D B Y
Account of:
DSSN 6424

TAX ID
PAYEE'S NAME BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
ADDRESS P.O BX 4340
BOSTON MA 02211

FT HUACHUCA, AZ 85613-6000

DATE INVOICE RECV'D 05/15/95
DISCOUNT TERMS NET 25 DAYS

FOB:
DEST

NO./DATE OF ORDER	INV DATE	DATE OF PERFORMANCE INVRCV'D	MDSE DEL	MDSE ACPT	FREIGHT	MERCHANDISE
12C	04/10/95	05/15/95	05/01/95	05/01/95	0.00	38283.53

TOTAL: MDSE+ 38283.53

AMOUNT VERIFIED CORRECT FOR $$ 38283.53
SIGNATURE OR INITIALS: 73/

PAYMENT: 16PARTIAL 06/09/95

PURSUANT TO THE AUTHORITY VESTED IN ME, I CERTIFY THAT THIS VOUCHER IS CORRECT AND PROPER FOR PAYMENT.

AUTHORIZED CERTIFYING OFFICER DATE: 06/08/95
FOR: For M.E.BELZA, MAJOR
DEFENSE ACCOUNTING OFFICER
Finance and Accounting Officer

ACCOUNTING CLASSIFICATIONS
97404001301000500 5P4T10A64104 2594 S02086 US JWC900 00JWC9 HJ150040060552 38283.53

PAYEE: BBN SYSTEMS & TECHNOLOGIES
DIV BOLT BERANEK & NEWMAN INC
P.O. BOX 4340
BOSTON MA 02211

CHECK AMT $$ 38283.53

CHECK NO.: ON US TREASURY DATE:

A12SRMP

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

US DEPARTMENT, BUREAU, OR
ESTABLISHMENT AND LOCATION
DEFENSE ACCOUNTING OFFICE
DFAS-IN/EM-TP
FORT HUACHUCA, AZ

DTE VOU PREP: 95/06/09
SCHEDULE NUM:
VOUCHER NUM: 221920
CONTRACT NO AND DATE: DABT63-94C0017
PAID BY: M.E. BELZA, MAJ,FC
FORT HUACHUCA
REQUISITION NO & DATE: 95/06/09
6424

PAYEE'S NAME AND ADDRESS: BBN SYSTEMS & TECHNOLOGIES
DIV BOLT BERANEK & NEWMAN I
P.O. BOX 4340
BOSTON MA 02211

DISCOUNT TERMS

INVOICE NO	INT/(DISC) AMT	LATE/TERMS	RATE
12C	0.00	0	0.0000%

NUM & DT ORD	ARTICLES OR SERVICES	QTY ISS	UNIT PRICE	AMOUNT
000001		1.00	38283.5300	38283.53

95160082410CAPS

TOTAL 38283.53

PAYMENT
_ PROVISIONAL
_ COMPLETE
X PARTIAL
_ FINAL
_ PROGRESS
_ ADVANCE

APPROVED BY
BY
TITLE

EXCHANGE RATE DIFF
=$1.00

AMT VER CORRECT 38283.53

SIGNATURE OR INITIALS: VE: 73 PMT NO: 016

AUT-CER: PALMER

PPA: 73

I CERTIFY THIS VOUCHER CORRECT AND PROPER FOR CHECK PAYMENT
95/06/09 M.E. BELZA
DEFENSE ACCOUNTING OFFICER

DATE AUTHORIZED CERTIFYING OFFICER TITLE

CHECK NUMBER 02521758

SF 1034

SF 1034 (CONTINUED) VOUCHER NUMBER: 221920 PAGE:

ACCOUNTING CLASSIFICATION

9740400.1301 00-5005 P4T10A8 2594 002086 US JWC900 00JWC9 HJ150040060552
ACCOUNTING AMOUNT: 38283.59

SF 1034-EDP PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

DEPARTMENT OF THE ARMY
DRAWER P
FT HUACHUCA, AZ 85613-6000

VOUCHER NO.

DATE PREPARED 02/16/95

CONTRACT NO./DATE DABT63-94-C-0017 04/05/94

PAID BY
Account of:
DSSN 6424

TAX ID
PAYEE'S NAME BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
ADDRESS P.O BX 4340
BOSTON MA 02211

FT HUACHUCA, AZ 85613-6000

DATE INVOICE RECV'D 01/24/95 FOB:
DISCOUNT TERMS NET 30 DAYS DEST

NO./DATE OF ORDER	INV DATE	DATE OF PERFORMANCE INVRCV'D	MDSE DEL	MDSE ACPT	FREIGHT	MERCHANDISE
9C	01/19/95	01/24/95	12/31/94	01/24/95	0.00	69633.08
9F	01/19/95	01/25/95	01/25/95	01/25/95	0.00	5878.99

TOTAL: MDSE+ 75512.07

AMOUNT VERIFIED CORRECT FOR $$ 75512.07
SIGNATURE OR INITIALS: 76/

PAYMENT: 12PARTIAL 02/23/95

PURSUANT TO THE AUTHORITY VESTED IN ME, I CERTIFY THAT THIS VOUCHER IS CORRECT AND PROPER FOR PAYMENT.

AUTHORIZED CERTIFYING OFFICER DATE: 02/16/95
FOR: For M.E.BELZA, MAJOR
DEFENSE ACCOUNTING OFFICER
Finance and Accounting Officer

ACCOUNTING CLASSIFICATIONS
97504001301000500503T10A84112 2581 S02086 US JWBL00 003WBL HJ150043480535 75512.0

PAYEE: BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
P.O BX 4340
BOSTON MA 02211

CHECK AMT $$ 75512.0

CHECK NO.: ON US TREASURY DATE:

AFZS-FM

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

US DEPARTMENT, BUREAU, OR
ESTABLISHMENT AND LOCATION
DEFENSE ACCOUNTING OFFICE
DFAS-IN/EM-TP
FORT HUACHUCA, AZ

DTE VOU PREP: 95/02/17
SCHEDULE NUM:
VOUCHER NUM: 211810
CONTRACT NO AND DATE: DABT63-94C0017
PAID BY: M.E. BELZA, MAJ,FC
FORT HUACHUCA
REQUISITION NO & DATE: 95/02/17
6424

PAYEE'S NAME AND ADDRESS: BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMA
P.O BX 4340
BOSTON MA 02211

DISCOUNT TERMS

INVOICE NO	INT/(DISC) AMT	LATE/TERMS	RATE
9C	0.00	0	0.0000%
9F	0.00	0	0.0000%

NUM & DT ORD	ARTICLES OR SERVICES	QTY ISS	UNIT PRICE	AMOUNT
000001		1.00	75512.0700	75512.07

95048100212CAPS

TOTAL 75512.07

PAYMENT
_ PROVISIONAL
_ COMPLETE
X PARTIAL
_ FINAL
_ PROGRESS
_ ADVANCE

APPROVED BY

BY

TITLE

EXCHANGE RATE =$1.00

DIFF

AMT VER CORRECT 75512.07

SIGNATURE OR INITIALS: VE: 76 PMT NO: 012

AUT-CER: KNIEFEL

PPA: 76

I CERTIFY THIS VOUCHER CORRECT AND PROPER FOR CHECK PAYMENT
95/02/17 M.E. BELZA
DEFENSE ACCOUNTING OFFICER

DATE AUTHORIZED CERTIFYING OFFICER TITLE

CHECK NUMBER 02496002

SF 1034

SF 1034 (CONTINUED) VOUCHER NUMBER: 211810 PAGE: 2

ACCOUNTING CLASSIFICATION

9750400.1301 00-5005 P5T10A8 2581 002086 US JWBL00 00JWHL HJ1500434B0535
ACCOUNTING AMOUNT: 75512.07

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

US DEPARTMENT, BUREAU, OR	DTE VOU PREP SCHEDULE NUM	VOUCHER NUM
ESTABLISHMENT AND LOCATION	95/04/03	215781
DEFENSE ACCOUNTING OFFICE	CONTRACT NO AND DATE	PAID BY
DFAS-IN/EM-TP	DABT63-94C0017	M.E. BELZA, MAJ,FC
FORT HUACHUCA, AZ		FORT HUACHUCA
	REQUISITION NO & DATE	95/04/03
		6424

PAYEE'S NAME AND ADDRESS: BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMA
P.O BX 4340
BOSTON MA 02211

DISCOUNT TERMS

INVOICE NO	INT/(DISC) AMT	LATE/TERMS	RATE
10C	0.00	0	0.0000%
10F	0.00	0	0.0000%

NUM & DT ORD	ARTICLES OR SERVICES	QTY ISS	UNIT PRICE	AMOUNT
000001		1.00	112629.8400	112629.84

9508072151CAPS TOTAL 112629.84

PAYMENT
_ PROVISIONAL
_ COMPLETE
X PARTIAL
_ FINAL
_ PROGRESS
_ ADVANCE

APPROVED BY
BY
TITLE

EXCHANGE RATE =$1.00
DIFF
AMT VER CORRECT 112629.84

SIGNATURE OR INITIALS: VE: 76 PMT NO: 013

AUT-CER: PALMER PPA: 76

I CERTIFY THIS VOUCHER CORRECT AND PROPER FOR CHECK PAYMENT

95/04/03 M.E. BELZA DEFENSE ACCOUNTING OFFICER

DATE AUTHORIZED CERTIFYING OFFICER TITLE

CHECK NUMBER 0250.378

SF 1034

ACCOUNTING CLASSIFICATION

9750400.1301 00-5005 P5T10A8 2581 002086 US JWBL00 00JWBL HJ150043480535
ACCOUNTING AMOUNT: 112629.84

SF 1034-EDP PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

DEPARTMENT OF THE ARMY
ORANGER P
FT HUACHUCA, AZ 85613-6000

VOUCHER NO.

DATE PREPARED 03/28/95

CONTRACT NO./DATE DABT63-94-C-0017 04/05/94

P A I D B Y
Account of:
DSSN 6424

TAX ID
PAYEE'S NAME BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
ADDRESS P.O BX 4340
BOSTON MA 02211

FT HUACHUCA, AZ 85613-6000

DATE INVOICE RECV'D 03/07/95
DISCOUNT TERMS NET 30 DAYS

FOB:
DEST

NO./DATE OF ORDER	INV DATE	DATE OF PERFORMANCE INVRCV'D	MDSE DEL	MDSE ACPT	FREIGHT	MERCHANDISE
10C	02/28/95	03/07/95	02/28/95	02/28/95	0.00	104323.41
10F	02/28/95	03/12/95	02/15/95	03/13/95	0.00	8306.43

TOTAL: MDSE+ 112629.84

AMOUNT VERIFIED CORRECT FOR $$ 112629.84
SIGNATURE OR INITIALS: 76/

PAYMENT: 13PARTIAL 04/06/95

PURSUANT TO THE AUTHORITY VESTED IN ME, I CERTIFY THAT THIS VOUCHER IS CORRECT AND PROPER FOR PAYMENT.

AUTHORIZED CERTIFYING OFFICER DATE: 03/28/95
FOR: For M.E.BELZA, MAJOR
DEFENSE ACCOUNTING OFFICER
Finance and Accounting Officer

ACCOUNTING CLASSIFICATIONS
97X0400130100050050ST10A84112 2581 S02086 US JWBL00 00JWBL HJ150043480535 112629.84

PAYEE: BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
P.O BX 4340
BOSTON MA 02211

CHECK AMT $$ 112629.84

CK NO.: ON US TREASURY DATE:

Standard Form 1034
Revised January 1980
Department of the Treasury
I TFRM 4-2000
1034-120

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

VOUCHER NO. 10F

U.S. DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION
Defense Finance & Accounting SVC
Defense Accounting Office
Drawer P
Fort Huachuca, AZ 85613-6000

DATE VOUCHER PREPARED: 28 February 1995
CONTRACT NUMBER AND DATE: DABT63-94-C-0017
REQUISITION NUMBER AND DATE:

SCHEDULE NO. 951169
PAID BY

PAYEE'S NAME AND ADDRESS
BBN SYSTEMS AND TECHNOLOGIES
A Division of Bolt Beranek & Newman, Inc.
P.O. BOX 4340
BOSTON, MA 02211
Point of contact: John Freyermuth @ (617) 873-3716

DATE INVOICE RECEIVED
DISCOUNT TERMS 11592 1.1/10186
PAYEE'S ACCOUNT NUMBER
GOVERNMENT B/L NUMBER

SHIPPED FROM | TO | WEIGHT

NUMBER AND DATE OF ORDER	DATE OF DELIVERY OR SERVICE	ARTICLES OR SERVICES (Enter description, item number of contract or Federal supply schedule, and other information deemed necessary)	QUANTITY	UNIT PRICE COST	UNIT PRICE PER	AMOUNT (1)
	01 Jan thru 15 Feb 1995	Total Fee for 01 January thru 15 February, 1995 Based on 55% completion X $50,524.00 Less Total Fee invoiced to date				$27,740.40 19,433.97
		Total Amount Due This Invoice COST REIMBURSABLE PROVISIONAL PAYMENT				$8,306.43

APPROVED FOR PAYMENT: $ $8,306.43
I certify acceptance of the Supplies or Services herein on 12 MAR 95
John P. Mavris
Contracting Officer
13 Mar 95
Date

(Use continuation sheet(s) if necessary) (Payee must NOT use the space below) TOTAL

PAYMENT:
- ☐ PROVISIONAL
- ☐ COMPLETE
- ☐ PARTIAL
- ☐ FINAL
- ☐ PROGRESS
- ☐ ADVANCE

APPROVED FOR Provisional Payment =$ Subject to Later Audit
EXCHANGE RATE =$1.00
DIFFERENCES
BY [2]
TITLE
Amount verified; correct for
(Signature or initials)

Pursuant to authority vested in me, I certify that this voucher is correct and proper for payment.

(Date) (Authorized Certifying Officer)[2] (Title)

ACCOUNTING CLASSIFICATION

PAID BY

CHECK NUMBER	ON ACCOUNT OF U.S. TREASURY	CHECK NUMBER	ON (Name of bank)
CASH $	DATE	PAYEE [3]	

[1] When stated in foreign currency, insert name of currency.
[2] If the ability to certify and authority to approve are combined in one person, one signature only is necessary; otherwise the approving officer will sign in the space provided, over his official title.
[3] When a voucher is receipted in the name of a company or corporation, the name of the person writing the company or corporate name, as well as the capacity in which he signs, must appear. For example: "Joan Doe Company, per John Smith, Secretary", or "Treasurer", as the case may be.

PER
TITLE

Previous edition usable
★U.S.GPO:1987-0-181-247/40205
NSN 7540-00-634-4206

PK

PRIVACY ACT STATEMENT
The information requested on this form is required under the provisions of 31 U.S.C. 82b and 82c, for the purpose of disbursing Federal money. The information requested is to identify the particular creditor and the amounts to be paid. Failure to furnish this information will hinder discharge of the payment obligation.

FORM 1035

CONTRACT NO. # DBAT63-94-C-0017

BBN REF. # 11592 1.1
BBN INVOICE # 951169
SHEET NO. # 2 of 2
VOUCHER #10F

BBN Systems and Technologies
A Division of Bolt Beranek and Newman, Inc.
P.O. Box 4340
Boston, MA 02211

Target/Estimated Cost	$634,557.00
Target/Fixed Fee	50,524.00
Total	$685,081.00
85% Fixed Fee	$42,945.40

Disbursing Office: Defense Finance & Accounting SVC
Defense Accounting Office
Drawer P
Fort Huachuca, AZ 85613-6000

Fixed Fee:

Fixed Fee Due (55% X $50,524.00)	$27,740.40
Less Fixed Fee Billed	19,433.97
Fixed Fee To Be Billed	$8,306.43

ard Form 1034
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rtment of the Treasury
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-120

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

VOUCHER NO. 10C

DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION
D.C.A.A.
WALTHAM BRANCH
24 TRAPELLO RD
WALTHAM, MA 02154-6397

DATE VOUCHER PREPARED: 28 February 1995

SCHEDULE NO.: 951169

CONTRACT NUMBER AND DATE: DABT63-94-C-0017

REQUISITION NUMBER AND DATE:

PAID BY

PAYEE'S NAME AND ADDRESS

BBN SYSTEMS AND TECHNOLOGIES
A Division of Bolt Beranek & Newman, Inc.
P.O. BOX 4340
BOSTON, MA 02211

Point of contact: John Freyermuth @ (617) 873-3716

DATE INVOICE RECEIVED

DISCOUNT TERMS

PAYEE'S ACCOUNT NUMBER: 11592 1.1/10186

SHIPPED FROM | TO | WEIGHT | GOVERNMENT B/L NUMBER

NUMBER AND DATE OF ORDER	DATE OF DELIVERY OR SERVICE	ARTICLES OR SERVICES (Enter description, item number of contract or Federal supply schedule, and other information deemed necessary)	QUANTITY	UNIT PRICE COST	UNIT PRICE PER	AMOUNT (1)
	01 Jan thru 15 Feb 1995	For detail, see SF 1035 continuation sheet. Total amount claimed transferred from Page 2, SF 1035 COST REIMBURSABLE PROVISIONAL PAYMENT				$104,323.41

(Use continuation sheet(s) if necessary) **(Payee must NOT use the space below)** TOTAL $104,323.41

PAYMENT:
[ ] PROVISIONAL
[ ] COMPLETE
[ ] PARTIAL
[ ] FINAL
[ ] PROGRESS
[ ] ADVANCE

APPROVED FOR: Provisional Payment Subject to Later Audit
EXCHANGE RATE: =$1.00

DIFFERENCES

BY [2]: John F.Gay

Amount verified; correct for

TITLE: Auditor, Defense Contract Audit Agency

(Signature or initials)

Pursuant to authority vested in me, I certify that this voucher is correct and proper for payment.

(Date) (Authorized Certifying Officer)[2] (Title)

ACCOUNTING CLASSIFICATION

CHECK NUMBER	ON ACCOUNT OF U.S. TREASURY	CHECK NUMBER	ON (Name of bank)
CASH $	DATE	PAYEE [3]	

When stated in foreign currency, insert name of currency.
If the ability to certify and authority to approve are combined in one person, one signature only is necessary; otherwise the approving officer will sign in the space provided, over his official title.
When a voucher is received in the name of a company or corporation, the name of the person writing the company or corporate name, as well as the capacity in which he signs, must appear. For example: "John Doe Company, per John Smith, Secretary", or "Treasurer", as the case may be.

PER

TITLE

previous edition usable
PK

*U.S.GPO:1987-0-181-247/40205

NSN 7540-00-634-4206

PRIVACY ACT STATEMENT
The information requested on this form is required under the provisions of 31 U.S.C. 82b and 82c, for the purpose of disbursing Federal money. The information requested is to identify the particular creditor and the amounts to be paid. Failure to furnish this information will hinder discharge of the payment obligation.

Continuation Sheet - Page # 3
BBN Reference # 11592 1.1
Bureau Voucher # 10C
Invoice # 951169

Direct Labor:

FY	Pool	Hours	Direct Labor	Overhead	Overhead Rate	G&A	G&A Rate
95	10.0	945.9	$34,881.24	$40,218.08	115.3%	$19,075.25	25.4%

Other Direct Costs:

Value Added Costs:

FY	Pool	Direct Costs			
95	0	$6,419.64		1,630.60	25.4%
			Total G&A	$20,705.85	

Non Value Added Costs:

FY	Direct Costs
95	$1,519.58

SF 1034-EDF PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

DEPARTMENT OF THE ARMY
DRAWER P
FT HUACHUCA, AZ 85613-6000

VOUCHER NO.

DATE PREPARED 03/28/95

CONTRACT NO./DATE DABT63-94-C-0017 04/05/94

P A I D B Y
Account of:
DSSN 6424

TAX ID
PAYEE'S NAME BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
ADDRESS P.O BX 4340
BOSTON MA 02211

FT HUACHUCA, AZ 85613-6000

DATE INVOICE RECV'D 03/07/95 FOB:
DISCOUNT TERMS NET 30 DAYS DEST

NO./DATE OF ORDER	INV DATE	DATE OF PERFORMANCE INVRCV'D	MDSE DEL	MDSE ACPT	FREIGHT	MERCHANDISE
10C	02/28/95	03/07/95	02/28/95	02/28/95	0.00	104323.41
10F	02/28/95	03/12/95	02/15/95	03/13/95	0.00	8306.43

TOTAL: MDSE+ 112629.84

AMOUNT VERIFIED CORRECT FOR $$ 112629.84
SIGNATURE OR INITIALS: 76/

PAYMENT: 13PARTIAL 04/06/95

PURSUANT TO THE AUTHORITY VESTED IN ME, I CERTIFY THAT THIS VOUCHER IS CORRECT AND PROPER FOR PAYMENT.

AUTHORIZED CERTIFYING OFFICER DATE: 03/28/95
FOR: For M.E.BELZA, MAJOR
DEFENSE ACCOUNTING OFFICER
Finance and Accounting Officer

ACCOUNTING CLASSIFICATIONS
97504001301000500505T10AB4112 2581 S02086 US JWBL00 00JWBL HJ150043480535 112629.84

PAYEE: BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
P.O BX 4340
BOSTON MA 02211

CHECK AMT $$ 112629.84

CHECK NO.: ON US TREASURY DATE:

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

US DEPARTMENT, BUREAU, OR
ESTABLISHMENT AND LOCATION
DEFENSE ACCOUNTING OFFICE
DFAS-IN/EM-TP
FORT HUACHUCA, AZ

DTE VOU PREP: 95/04/03
SCHEDULE NUM:
VOUCHER NUM: 215781
CONTRACT NO AND DATE: DABT63-94C0017
PAID BY: M.E. BELZA, MAJ,FC
FORT HUACHUCA
REQUISITION NO & DATE: 95/04/03
6424

PAYEE'S NAME AND ADDRESS: BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMA
P.O BX 4340
BOSTON MA 02211

DISCOUNT TERMS

INVOICE NO	INT/(DISC) AMT	LATE/TERMS	RATE
10C	0.00	0	0.0000%
10F	0.00	0	0.0000%

NUM & DT ORD	ARTICLES OR SERVICES	QTY	UNIT ISS	PRICE	AMOUNT
000001		1.00		112629.8400	112629.84

9508807215ICAPS

TOTAL 112629.84

PAYMENT
_ PROVISIONAL
_ COMPLETE
X PARTIAL
_ FINAL
_ PROGRESS
_ ADVANCE

APPROVED BY
BY
TITLE

EXCHANGE RATE =$1.00
DIFF

AMT VER CORRECT 112629.84

SIGNATURE OR INITIALS: VE: 76 PMT NO: 013

AUT-CER: PALMER

PPA: 76

I CERTIFY THIS VOUCHER CORRECT AND PROPER FOR CHECK PAYMENT
95/04/03 M.E. BELZA
DEFENSE ACCOUNTING OFFICER

DATE AUTHORIZED CERTIFYING OFFICER TITLE

CHECK NUMBER 02506375

SF 1034

ACCOUNTING CLASSIFICATION

9750400.1301 00-5005 P5T10A8 2581 002086 US JWBL00 00JWBL HJ150043480535
ACCOUNTING AMOUNT: 112629.84

SF 1034-EDP PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

DEPARTMENT OF THE ARMY
DRAWER P
FT HUACHUCA, AZ 85613-6000

VOUCHER NO.

DATE PREPARED 05/19/95

CONTRACT NO./DATE DABT63-94-C-0017 04/05/94

PAID BY
Account of:
DSSN 6424

TAX ID
PAYEE'S NAME BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
ADDRESS P.O BX 4340
BOSTON MA 02211

FT HUACHUCA, AZ 85613-6000

DATE INVOICE RECV'D 04/20/95
DISCOUNT TERMS NET 30 DAYS

FOB:
DEST

NO./DATE OF ORDER	INV DATE	DATE OF PERFORMANCE INVRCV'D	MDSE DEL	MDSE ACPT	FREIGHT	MERCHANDISE
11C	04/10/95	04/20/95	03/31/95	04/10/95	0.00	95545.24
11F	04/10/95	04/20/95	03/31/95	04/25/95	0.00	7607.39
5C	09/14/94	11/14/94	08/31/94	09/19/94	0.00	-13818.92

DEDUCTION TAKEN FOR DUPLICATED PAYMENTS AGAINST YOUR
INVOICE NO 5C - DOV 205017 chk 02482350 dtd 12 Dec 94 9P
and DOV 201241 chk 02470552 dtd 13 Oct 94 5P

TOTAL: MDSE+ 89333.71

AMOUNT VERIFIED CORRECT FOR $$ 89333.71
SIGNATURE OR INITIALS: 91/

PAYMENT: 14PARTIAL 05/22/95

PURSUANT TO THE AUTHORITY VESTED IN ME, I CERTIFY THAT THIS VOUCHER IS CORRECT AND PROPER FOR PAYMENT.

AUTHORIZED CERTIFYING OFFICER DATE: 05/19/95
FOR: For M.E.BELZA, MAJOR
DEFENSE ACCOUNTING OFFICER
Finance and Accounting Officer

ACCOUNTING CLASSIFICATIONS

97404001301000500 5P4T10A64104	2594	S02086	US	JWC900	00JWC9	HJ150040060552	103152.63
97504001301000500 5T10A8411400	2581	S02086	US	JWBL00	00JWBL	HJ150043480535	-13818.92

PAYEE: BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
P.O BX 4340
BOSTON MA 02211

CHECK AMT $$ 89333.71

CHECK NO.: ON US TREASURY DATE:

AF25-RMP-A

Standard Form 1034
Revised January 1980
Department of the Treasury
1 TFRM 4–2000
1034–120

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

VOUCHER NO. 11F

U.S. DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION
Defense Finance & Accounting SVC
Defense Accounting Office
Drawer P
Fort Huachuca, AZ 85613-6000

DATE VOUCHER PREPARED: 10 April 1995

SCHEDULE NO. 951339

CONTRACT NUMBER AND DATE: DABT63-94-C-0017

REQUISITION NUMBER AND DATE:

PAID BY

PAYEE'S NAME AND ADDRESS

BBN SYSTEMS AND TECHNOLOGIES
A Division of Bolt Beranek & Newman, Inc.
P.O. BOX 4340
BOSTON, MA 02211

Point of contact: John Freyermuth @ (617) 873-3716

DATE INVOICE RECEIVED

DISCOUNT TERMS: 11592 1.1/10186

PAYEE'S ACCOUNT NUMBER

SHIPPED FROM | TO | WEIGHT | GOVERNMENT B/L NUMBER

NUMBER AND DATE OF ORDER	DATE OF DELIVERY OR SERVICE	ARTICLES OR SERVICES (Enter description, item number of contract or Federal supply schedule, and other information deemed necessary)	QUANTITY	UNIT PRICE COST	UNIT PRICE PER	AMOUNT (1)
	16 Feb thru 31 Mar 1995	Total Fee for 16 February thru 31 March, 1995				
		Based on 70% completion X $50,524.00				$35,347.79
		Less Total Fee invoiced to date				27,740.40
		Total Amount Due This Invoice				$7,607.39
		COST REIMBURSABLE PROVISIONAL PAYMENT				

APPROVED FOR PAYMENT: $
I certify acceptance of the Supplies or Services herein
TOTAL
DIFFERENCES
$1.00
Contracting Officer
25 Apr 95
Date

(Use continuation sheet(s) if necessary) (Payee must NOT use the space below)

PAYMENT:
- ☐ PROVISIONAL
- ☐ COMPLETE
- ☐ PARTIAL
- ☐ FINAL
- ☐ PROGRESS
- ☐ ADVANCE

APPROVED FOR $ Provisional Payment Subject to Later Audit

EXCHANGE RATE = $1.00

BY [2]

TITLE

Amount verified; correct for

(Signature or initials)

Pursuant to authority vested in me, I certify that this voucher is correct and proper for payment.

(Date) (Authorized Certifying Officer)[2] (Title)

ACCOUNTING CLASSIFICATION

PAID BY

CHECK NUMBER | ON ACCOUNT OF U.S. TREASURY | CHECK NUMBER | ON (Name of bank)

CASH $ | DATE | PAYEE [3]

[1] When stated in foreign currency, insert name of currency.
[2] If the ability to certify and authority to approve are combined in one person, one signature only is necessary; otherwise the approving officer will sign in the space provided, over his official title.
[3] When a voucher is receipted in the name of a company or corporation, the name of the person writing the company or corporate name, as well as the capacity in which he signs, must appear. For example: "John Doe Company, per John Smith, Secretary", or "Treasurer", as the case may be.

PER

TITLE

Previous edition usable

★U.S.GPO:1987-0-181-247/40205

NSN 7540-00-634-4206

PK

PRIVACY ACT STATEMENT
The information requested on this form is required under the provisions of 31 U.S.C. 82b and 82c, for the purpose of disbursing Federal money. The information requested is to identify the particular creditor and the amounts to be paid. Failure to furnish this information will hinder discharge of the payment obligation.

FORM 1035

CONTRACT NO. # DBAT63-94-C-0017

BBN REF. # 11592 1.1
BBN INVOICE # 951169
SHEET NO. # 2 of 2
VOUCHER #11F

BBN Systems and Technologies
A Division of Bolt Beranek and Newman, Inc.
P.O. Box 4340
Boston, MA 02211

Target/Estimated Cost	$634,557.00
Target/Fixed Fee	50,524.00
Total	$685,081.00
85% Fixed Fee	$42,945.40

Disbursing Office: Defense Finance & Accounting SVC
Defense Accounting Office
Drawer P
Fort Huachuca, AZ 85613-6000

Fixed Fee:

Fixed Fee Due (70% X $50,524.00)	$35,347.79
Less Fixed Fee Billed	27,740.40
Fixed Fee To Be Billed	$7,607.39

Standard Form 1034
Revised January 1980
Department of the Treasury
1 TFRM 4-2000
1034-120

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

VOUCHER NO. 11C

U.S. DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION
D.C.A.A.
WALTHAM BRANCH
424 TRAPELLO RD
WALTHAM, MA 02154-6397

DATE VOUCHER PREPARED: 10 April 1995

SCHEDULE NO. 951339

CONTRACT NUMBER AND DATE: DABT63-94-C-0017

REQUISITION NUMBER AND DATE:

PAID BY

PAYEE'S NAME AND ADDRESS

BBN SYSTEMS AND TECHNOLOGIES
A Division of Bolt Beranek & Newman, Inc.
P.O. BOX 4340
BOSTON, MA 02211

Point of contact: John Freyermuth @ (617) 873-3716

DATE INVOICE RECEIVED

DISCOUNT TERMS

PAYEE'S ACCOUNT NUMBER: 11592 1.1/10186

SHIPPED FROM | TO | WEIGHT | GOVERNMENT B/L NUMBER

NUMBER AND DATE OF ORDER	DATE OF DELIVERY OR SERVICE	ARTICLES OR SERVICES (Enter description, item number of contract or Federal supply schedule, and other information deemed necessary)	QUANTITY	UNIT PRICE COST	UNIT PRICE PER	AMOUNT (1)
	16 Feb thru 31 Mar 1995	For detail, see SF 1035 continuation sheet. Total amount claimed transferred from Page 2, SF 1035 COST REIMBURSABLE PROVISIONAL PAYMENT				$95,545.24

(Use continuation sheet(s) if necessary) **(Payee must NOT use the space below)** **TOTAL** $95,545.24

PAYMENT:
- ☐ PROVISIONAL
- ☐ COMPLETE
- ☐ PARTIAL
- ☐ FINAL
- ☐ PROGRESS
- ☐ ADVANCE

APPROVED FOR: Provisional Payment Subject to Later Audit

EXCHANGE RATE: =$1.00

DIFFERENCES

BY [2]: John F.Gay

Amount verified; correct for

TITLE: Auditor, Defense Contract Audit Agency

(Signature or initials)

Pursuant to authority vested in me, I certify that this voucher is correct and proper for payment.

(Date) (Authorized Certifying Officer)[2] (Title)

ACCOUNTING CLASSIFICATION

PAID BY

CHECK NUMBER | ON ACCOUNT OF U.S. TREASURY | CHECK NUMBER | ON (Name of bank)

CASH $ | DATE | PAYEE [3]

[1] When stated in foreign currency, insert name of currency.
[2] If the ability to certify and authority to approve are combined in one person, one signature only is necessary; otherwise the approving officer will sign in the space provided, over his official title.
[3] When a voucher is receipted in the name of a company or corporation, the name of the person writing the company or corporate name, as well as the capacity in which he signs, must appear. For example: "John Doe Company, per John Smith, Secretary", or "Treasurer", as the case may be.

PER

TITLE

Previous edition usable

★U.S.GPO:1987-0-181-247/40205

NSN 7540-00-634-4206

PK

PRIVACY ACT STATEMENT
The information requested on this form is required under the provisions of 31 U.S.C. 82b and 82c, for the purpose of disbursing Federal money. The information requested is to identify the particular creditor and the amounts to be paid. Failure to furnish this information will hinder discharge of the payment obligation.

FORM 1035

CONTRACT NO. # DABT63-94-C-0017

BBN REF. # 11592 1.1
BBN INVOICE # 951339
SHEET NO. # 2 OF 3
VOUCHER #11C

BBN Systems and Technologies
A Division of Bolt Beranek and Newman, Inc.
P.O. Box 4340
Boston, MA 02211

Target/Estimated Cost	$634,557.00
Target/Fixed Fee	50,524.00
Total	$685,081.00
85% Fixed Fee	$42,945.40

Disbursing Office: Defense Finance & Accounting SVC
Defense Accounting Office
Drawer P
Fort Huachuca, AZ 85613-6000

Withholding Clause:

BBN Withholding:

Analysis of Current and Cumulative Costs and Fee Earned:

Major Cost Elements:	Amount for Current Period Billed	Cumulative Amounts From Inception to Date of This Billing
Direct Labor	$28,944.36	$147,975.80
Overhead	33,372.78	171,616.68
Travel	0.00	1,525.60
Material	2,108.39	9,143.92
Procurement Charge	105.42	479.11
Equipment/Software Rental	0.00	704.50
Computer Services	11,596.24	22,861.21
Books & Subscriptions	0.00	30.00
Subcontractors - Company	0.00	60.00
Postage & Express Mail	9.60	18.60
Training Conference	0.00	150.00
General Administration	18,800.81	87,009.09
Total Cost	$94,937.60	$441,574.51
CAS414	607.64	2,376.70
TOTAL	$95,545.24	$443,951.21

US DEPARTMENT, BUREAU
ESTABLISHMENT AND LOCATION
DEFENSE ACCOUNTING OFFICE
DFAS-IN/EM-TP
FORT HUACHUCA, AZ

DTE VOU PREP: 95/05/22
SCHE E NUM
VOUCHER NUM: 220112
CONTRACT NO AND DATE: DABT63-94C0017
REQUISITION NO & DATE: 6424
PAID BY: M.E. BELZA, MAJ,FC
FORT HUACHUCA
95/05/22

PAYEE'S NAME AND ADDRESS: BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMA
P.O BX 4340
BOSTON MA 02211

DISCOUNT TERMS

INVOICE NO	INT/(DISC) AMT	LATE/TERMS	RATE
11C	0.00	0	0.0000%
11F	0.00	0	0.0000%
5C	0.00	0	0.0000%

NUM & DT ORD	ARTICLES OR SERVICES	QTY ISS	UNIT PRICE	AMOUNT
000001		1.00	103152.6300	103152.63
000002		1.00	13818.9200	-13818.92

95142083924CAPS

TOTAL 89333.71

PAYMENT
_ PROVISIONAL
_ COMPLETE
X PARTIAL
_ FINAL
_ PROGRESS
_ ADVANCE

APPROVED BY
BY
TITLE

EXCHANGE RATE DIFF
=$1.00

AMT VER CORRECT 89333.71

SIGNATURE OR INITIALS: VE: 91 PMT NO: 014

AUT-CER: PALMER

PPA: 91

I CERTIFY THIS VOUCHER CORRECT AND PROPER FOR CHECK PAYMENT
95/05/22 M.E. BELZA
DEFENSE ACCOUNTING OFFICER

DATE AUTHORIZED CERTIFYING OFFICER TITLE

CHECK NUMBER 02517461

SF 1034

ACCOUNTING CLASSIFICATION

9740400.1301 00-5005 P4T10A8 2594 002086 US JWC900 00JWC9 HJ150040060552
ACCOUNTING AMOUNT: 103152.63
9750400.1301 00-5005 P5T10A8 2581 002086 US JWBL00 00JWBL HJ150043480535
ACCOUNTING AMOUNT: -13818.92

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

US DEPARTMENT, BUREAU, OR
ESTABLISHMENT AND LOCATION
DEFENSE ACCOUNTING OFFICE
DFAS-IN/EM-TP
FORT HUACHUCA, AZ

DTE VOU PREP: 95/01/17
SCHEDULE NUM:
VOUCHER NUM: 209256
CONTRACT NO AND DATE: DABT63-94C0017
REQUISITION NO & DATE: 95/01/17 6424
PAID BY: M.E. BELZA, MAJ,FC FORT HUACHUCA

PAYEE'S NAME AND ADDRESS: BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMA
P.O BX 4340
BOSTON MA 02211

DISCOUNT TERMS

PAYEE'S ACCOUNT NUMBER

INVOICE NO: SC SF

NUM & DT ORD	ARTICLES OR SERVICES	QTY CST	UNIT PRICE PER	AMOUNT
000001		1.00	62300.510000	62300

950120731300CAPS

TOTAL 62300.51

PAYMENT
_ PROVISIONAL
_ COMPLETE
X PARTIAL
_ FINAL
_ PROGRESS
_ ADVANCE

APPROVED BY
BY
TITLE

EXCHANGE RATE DIFF
=$1.00

AMT VER CORRECT 62300.51

SIGNATURE OR INITIALS: VE: 76 PMT NO: 010
AUT-CER: PALMER

PPA: 76

I CERTIFY THIS VOUCHER CORRECT AND PROPER FOR CHECK PAYMENT
95/01/17 M.E. BELZA
DEFENSE ACCOUNTING OFFICER

DATE AUTHORIZED CERTIFYING OFFICER TITLE

ACCOUNTING CLASSIFICATION

9740400.1301 00-5005 P4T10A8 2594 002086 US JWC900 00JWC9 HJ150040060552
ACCOUNTING AMOUNT: 62300.51

SF 1034-EDP PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

DEPARTMENT OF THE ARMY
DRAWER P
FT HUACHUCA, AZ 85613-6000

VOUCHER NO.

DATE PREPARED 01/11/95

CONTRACT NO./DATE DABT63-94-C-0017 04/05/94

P A I D B Y
Account of:
DSSN 6424

TAX ID
PAYEE'S NAME BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
ADDRESS P.O BX 4340
BOSTON MA 02211

FT HUACHUCA, AZ 85613-6000

DATE INVOICE RECV'D 12/24/94 FOB:
DISCOUNT TERMS NET 30 DAYS DEST

NO./DATE OF ORDER	INV DATE	DATE OF PERFORMANCE INVRCV'D	MDSE DEL	MDSE ACPT	FREIGHT	MERCHANDISE
8C	12/19/94	12/24/94	11/30/94	12/24/94	0.00	58019.99
8F	12/19/94	12/24/94	11/30/94	12/24/94	0.00	4280.52

TOTAL: MDSE+ 62300.51

AMOUNT VERIFIED CORRECT FOR $$ 62300.51
SIGNATURE OR INITIALS: 76/

PAYMENT: 1OPARTIAL 01/23/95

PURSUANT TO THE AUTHORITY VESTED IN ME, I CERTIFY THAT THIS VOUCHER IS CORRECT AND PROPER FOR PAYMENT.

AUTHORIZED CERTIFYING OFFICER DATE: 01/11/95
FOR: For M.E.BELZA, MAJOR
DEFENSE ACCOUNTING OFFICER
Finance and Accounting Officer

ACCOUNTING CLASSIFICATIONS
9740400130010005005P4T10A8410 2594 S02086 US JWC900 00JWC9 HJ150040060552 62300.51

PAYEE: BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
P.O BX 4340
BOSTON MA 02211

CHECK AMT $$ 62300.51

CHECK NO.: ON US TREASURY DATE:

BT 160

Standard Form 1034
Revised January 1980
Department of the Treasury
1 TFRM 4-2000
1034-120

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

VOUCHER NO. 8F

U.S. DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION
Defense Finance & Accounting SVC
Defense Accounting Office
Drawer P
Fort Huachuca, AZ 85613-6000

DATE VOUCHER PREPARED: 19 December 1994

CONTRACT NUMBER AND DATE: DABT63-94-C-0017

REQUISITION NUMBER AND DATE:

SCHEDULE NO. 950876

PAID BY

PAYEE'S NAME AND ADDRESS
BBN SYSTEMS AND TECHNOLOGIES
A Division of Bolt Beranek & Newman, Inc.
P.O. BOX 4340
BOSTON, MA 02211
Point of contact: Deb Veino @ (617) 873-2426

DATE INVOICE RECEIVED

DISCOUNT TERMS: 11592 1.1/10186

PAYEE'S ACCOUNT NUMBER

SHIPPED FROM | TO | WEIGHT | GOVERNMENT B/L NUMBER

NUMBER AND DATE OF ORDER	DATE OF DELIVERY OR SERVICE	ARTICLES OR SERVICES (Enter description, item number of contract or Federal supply schedule, and other information deemed necessary)	QUANTITY	UNIT PRICE COST	UNIT PRICE PER	AMOUNT (1)
	01 Nov thru 30 Nov 1994	Total Fee for 01 November thru 30November, 1994				
		Based on 38% completion X $35,671.00				$13,554.98
		Less Total Fee invoiced to date				9,274.46
		Total Amount Due This Invoice				$4,280.52
		COST REIMBURSABLE PROVISIONAL PAYMENT				

(Use continuation sheet(s) if necessary) (Payee must NOT use the space below) TOTAL

PAYMENT:
- ☐ PROVISIONAL
- ☐ COMPLETE
- ☐ PARTIAL
- ☐ FINAL
- ☐ PROGRESS
- ☐ ADVANCE

APPROVED FOR $ Provisional Payment Subject to Later Audit

EXCHANGE RATE = $1.00

DIFFERENCES

BY [2]

TITLE

APPROVED FOR PAYMENT: $4,280.52
I certify acceptance of the Supplies or Services herein on 12/28/94

Amount verified; correct for (Signature or initials)

Pursuant to authority vested in me, I certify that this voucher is correct and proper for payment.

Debra A Veino 12/28/94
Contracting Officer Date

(Date) (Authorized Certifying Officer) (Title)

ACCOUNTING CLASSIFICATION

PAID BY

CHECK NUMBER	ON ACCOUNT OF U.S. TREASURY	CHECK NUMBER	ON (Name of bank)
CASH $	DATE	PAYEE [3]	

PER

TITLE

[1] When stated in foreign currency, insert name of currency.
[2] If the ability to certify and authority to approve are combined in one person, one signature only is necessary; otherwise the approving officer will sign in the space provided, over his official title.
[3] When a voucher is receipted in the name of a company or corporation, the name of the person writing the company or corporate name, as well as the capacity in which he signs, must appear. For example: "John Doe Company, per John Smith, Secretary", or "Treasurer", as the case may be.

Previous edition usable

*U.S.GPO:1987-0-181-247/40205

NSN 7540-00-634-4206

PK

PRIVACY ACT STATEMENT
The information requested on this form is required under the provisions of 31 U.S.C. 82b and 82c, for the purpose of

Standard Form 1034
Revised January 1980
Department of the Treasury
I TFRM 4-2000
1034-120

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

VOUCHER NO. 8F

U.S. DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION
Defense Finance & Accounting SVC
Defense Accounting Office
Drawer P
Fort Huachuca, AZ 85613-6000

DATE VOUCHER PREPARED: 19 December 1994

CONTRACT NUMBER AND DATE: DABT63-94-C-0017

REQUISITION NUMBER AND DATE:

SCHEDULE NO. 950876

PAID BY

PAYEE'S NAME AND ADDRESS
BBN SYSTEMS AND TECHNOLOGIES
A Division of Bolt Beranek & Newman, Inc.
P.O. BOX 4340
BOSTON, MA 02211
Point of contact: Deb Veino @ (617) 873-2426

DATE INVOICE RECEIVED

DISCOUNT TERMS 11592 1.1/10186

PAYEE'S ACCOUNT NUMBER

SHIPPED FROM | TO | WEIGHT | GOVERNMENT B/L NUMBER

NUMBER AND DATE OF ORDER	DATE OF DELIVERY OR SERVICE	ARTICLES OR SERVICES (Enter description, item number of contract or Federal supply schedule, and other information deemed necessary)	QUANTITY	UNIT PRICE COST	UNIT PRICE PER	AMOUNT (1)
	01 Nov thru 30 Nov 1994	Total Fee for 01 November thru 30November, 1994				
		Based on 38% completion X $35,671.00				$13,554.98
		Less Total Fee invoiced to date				9,274.46
		Total Amount Due This Invoice				$4,280.52
		COST REIMBURSABLE PROVISIONAL PAYMENT				

(Use continuation sheet(s) if necessary) **(Payee must NOT use the space below)** TOTAL

PAYMENT:
- ☐ PROVISIONAL
- ☐ COMPLETE
- ☐ PARTIAL
- ☐ FINAL
- ☐ PROGRESS
- ☐ ADVANCE

APPROVED FOR Provisional Payment Subject to Later Audit

EXCHANGE RATE $ = $1.00

DIFFERENCES

BY [2]

Amount verified; correct for

TITLE

(Signature or initials)

Pursuant to authority vested in me, I certify that this voucher is correct and proper for payment.

(Date) (Authorized Certifying Officer)[2] (Title)

ACCOUNTING CLASSIFICATION

PAID BY

CHECK NUMBER	ON ACCOUNT OF U.S. TREASURY	CHECK NUMBER	ON (Name of bank)
CASH $	DATE	PAYEE [3]	

[1] When stated in foreign currency, insert name of currency.
[2] If the ability to certify and authority to approve are combined in one person, one signature only is necessary; otherwise the approving officer will sign in the space provided, over his official title.
[3] When a voucher is receipted in the name of a company or corporation, the name of the person writing the company or corporate name, as well as the capacity in which he signs, must appear. For example: "John Doe Company, per John Smith, Secretary", or "Treasurer", as the case may be.

PER

TITLE

Previous edition usable

*U.S.GPO:1987-0-181-247/40205

NSN 7540-00-634-4206

PX

PRIVACY ACT STATEMENT
The information requested on this form is required under the provisions of 31 U.S.C. 82b and 82c, for the purpose of disbursing Federal money. The information requested is to identify the particular creditor and the amounts to be paid. Failure

FORM 1035

CONTRACT NO. # DBAT63-94-C-0017

BBN REF. # 11592 1.1
BBN INVOICE # 950876
SHEET NO. # 2 of 2
VOUCHER #8F

BBN Systems and Technologies
A Division of Bolt Beranek and Newman, Inc.
P.O. Box 4340
Boston, MA 02211

Target/Estimated Cost	$448,013.00
Target/Fixed Fee	35,671.00
Total	$483,684.00
85% Fixed Fee	$30,320.35

Disbursing Office: Defense Finance & Accounting SVC
Defense Accounting Office
Drawer P
Fort Huachuca, AZ 85613-6000

Fixed Fee:

Fixed Fee Due (38% X $35,671.00)	$13,554.98
Less Fixed Fee Billed	$9,274.46
Fixed Fee To Be Billed	$4,280.52

Standard Form 1034
Revised January 1980
Department of the Treasury
1 TFRM 4-2000
1034-120

PU C VOUCHER FOR PURCHASES AN SERVICES OTHER THAN PERSONAL

VOUCHER NO. 8C

U.S. DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION

D.C.A.A.
WALTHAM BRANCH
424 TRAPELLO RD
WALTHAM, MA 02154-6397

DATE VOUCHER PREPARED: 19 December 1994

SCHEDULE NO. 950876

CONTRACT NUMBER AND DATE: DABT63-94-C-0017

REQUISITION NUMBER AND DATE:

PAID BY

PAYEE'S NAME AND ADDRESS

BBN SYSTEMS AND TECHNOLOGIES
A Division of Bolt Beranek & Newman, Inc.
P.O. BOX 4340
BOSTON, MA 02211

Point of contact: Deb Veino @ (617) 873-2426

DATE INVOICE RECEIVED

DISCOUNT TERMS

PAYEE'S ACCOUNT NUMBER: 11592 1.1/10186

SHIPPED FROM | TO | WEIGHT | GOVERNMENT B/L NUMBER

NUMBER AND DATE OF ORDER	DATE OF DELIVERY OR SERVICE	ARTICLES OR SERVICES (Enter description, item number of contract or Federal supply schedule, and other information deemed necessary)	QUANTITY	UNIT PRICE COST	UNIT PRICE PER	AMOUNT (1)
	01 Nov thru 30 Nov 1994	For detail, see SF 1035 continuation sheet. Total amount claimed transferred from Page 2, SF 1035 COST REIMBURSABLE PROVISIONAL PAYMENT				$58,019.99

(Use continuation sheet(s) if necessary) **(Payee must NOT use the space below)** TOTAL $58,019.99

PAYMENT:
- ☐ PROVISIONAL
- ☐ COMPLETE
- ☐ PARTIAL
- ☐ FINAL
- ☐ PROGRESS
- ☐ ADVANCE

APPROVED FOR: Provisional Payment Subject to Later Audit

EXCHANGE RATE = $1.00

BY [2]: A. Reynolds

TITLE: Auditor, Defense Contract Audit Agency

DIFFERENCES

Amount verified; correct for

(Signature or initials)

Pursuant to authority vested in me, I certify that this voucher is correct and proper for payment.

(Date) | (Authorized Certifying Officer)[2] | (Title)

ACCOUNTING CLASSIFICATION

PAID BY

CHECK NUMBER	ON ACCOUNT OF U.S. TREASURY	CHECK NUMBER	ON (Name of bank)
CASH $	DATE	PAYEE [3]	

[1] When stated in foreign currency, insert name of currency.
[2] If the ability to certify and authority to approve are combined in one person, one signature only is necessary; otherwise the approving officer will sign in the space provided, over his official title.
[3] When a voucher is receipted in the name of a company or corporation, the name of the person writing the company or corporate name, as well as the capacity in which he signs, must appear. For example: "John Doe Company, per John Smith, Secretary", or "Treasurer", as the case may be.

PER

TITLE

Previous edition usable

★U.S.GPO:1987-0-181-247/40205

NSN 7540-00-634-4206

PRIVACY ACT STATEMENT
The information requested on this form is required under the provisions of 31 U.S.C. 82b and 82c, for the purpose of disbursing Federal money. The information requested is to identify the particular creditor and the amounts to be paid. Failure to furnish this information will hinder discharge of the payment obligation.

Standard Form 1034
Revised January 1980
Department of the Treasury
1 TFRM 4-2000
1034-120

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

VOUCHER NO. 8C

U.S. DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION

D.C.A.A.
WALTHAM BRANCH
424 TRAPELLO RD
WALTHAM, MA 02154-6397

DATE VOUCHER PREPARED: 19 December 1994

CONTRACT NUMBER AND DATE: DABT63-94-C-0017

REQUISITION NUMBER AND DATE:

SCHEDULE NO. 950876

PAID BY

PAYEE'S NAME AND ADDRESS

BBN SYSTEMS AND TECHNOLOGIES
A Division of Bolt Beranek & Newman, Inc.
P.O. BOX 4340
BOSTON, MA 02211

Point of contact: Deb Veino @ (617) 873-2426

DATE INVOICE RECEIVED

DISCOUNT TERMS

PAYEE'S ACCOUNT NUMBER 11592 1.1/10186

SHIPPED FROM | TO | WEIGHT | GOVERNMENT B/L NUMBER

NUMBER AND DATE OF ORDER	DATE OF DELIVERY OR SERVICE	ARTICLES OR SERVICES (Enter description, item number of contract or Federal supply schedule, and other information deemed necessary)	QUANTITY	UNIT PRICE COST	UNIT PRICE PER	AMOUNT (1)
	01 Nov thru 30 Nov 1994	For detail, see SF 1035 continuation sheet. Total amount claimed transferred from Page 2, SF 1035 COST REIMBURSABLE PROVISIONAL PAYMENT				$58,019.99

(Use continuation sheet(s) if necessary) **(Payee must NOT use the space below)** **TOTAL** $58,019.99

PAYMENT:
- ☐ PROVISIONAL
- ☐ COMPLETE
- ☐ PARTIAL
- ☐ FINAL
- ☐ PROGRESS
- ☐ ADVANCE

APPROVED FOR Provisional Payment Subject to Later Audit

EXCHANGE RATE = $1.00

DIFFERENCES

BY [2] A. Reynolds

Amount verified; correct for

TITLE Auditor, Defense Contract Audit Agency

(Signature or initials)

Pursuant to authority vested in me, I certify that this voucher is correct and proper for payment.

(Date) (Authorized Certifying Officer)[2] (Title)

ACCOUNTING CLASSIFICATION

PAID BY

CHECK NUMBER | ON ACCOUNT OF U.S. TREASURY | CHECK NUMBER | ON (Name of bank)

CASH $ | DATE | PAYEE [3]

[1] When stated in foreign currency, insert name of currency.
[2] If the ability to certify and authority to approve are combined in one person, one signature only is necessary; otherwise the approving officer will sign in the space provided, over his official title.
[3] When a voucher is receipted in the name of a company or corporation, the name of the person writing the company or corporate name, as well as the capacity in which he signs, must appear. For example: "John Doe Company, per John Smith, Secretary", or "Treasurer", as the case may be.

PER

TITLE

Previous edition usable

*U.S.GPO:1987-0-181-247/40205

NSN 7540-00-634-4206

PK

PRIVACY ACT STATEMENT

The information requested on this form is required under the provisions of 31 U.S.C. 82b and 82c, for the purpose of disbursing Federal money. The information requested is to identify the particular creditor and the amounts to be paid. Failure

FORM 1035

CONTRACT NO. # DABT63-94-C-0017

BBN REF. # 11592 1.1
BBN INVOICE # 950876
SHEET NO. # 2 OF 3
VOUCHER #8C

BBN Systems and Technologies
A Division of Bolt Beranek and Newman, Inc.
P.O. Box 4340
Boston, MA 02211

Target/Estimated Cost	$448,013.00
Target/Fixed Fee	35,671.00
Total	$483,684.00
85% Fixed Fee	$30,320.35

Disbursing Office: Defense Finance & Accounting SVC
Defense Accounting Office
Drawer P
Fort Huachuca, AZ 85613-6000

Withholding Clause:
BBN Withholding:

Analysis of Current and Cumulative Costs and Fee Earned:

Major Cost Elements:	Amount for Current Period Billed	Cumulative Amounts From Inception to Date of This Billing
Direct Labor	$19,177.71	$60,250.27
Overhead	22,111.89	70,469.17
Travel	11.60	1,525.60
Material	3,376.25	4,957.83
Procurement Charge	182.23	284.61
Equipment/Software Rental	268.25	704.50
Computer Services	1,653.75	1,653.75
Books & Subscriptions	0.00	30.00
Postage & Express Mail	0.00	9.00
Training Conference	0.00	150.00
General Administration	10,956.86	33,599.15
Total Cost	$57,738.54	$173,633.88
CAS414	281.45	815.60
TOTAL	$58,019.99	$174,449.48

Continuation Sheet - Page # 3
BBN Reference # 11592 1.1
Bureau Voucher # 8C
Invoice # 950876

Direct Labor:

FY	Pool	Hours	Direct Labor	Overhead	Overhead Rate	G&A	G&A Rate
95	10	526.3	$19,177.71	$22,111.89	115.3%	$10,487.56	25.4%

Other Direct Costs:

Value Added Costs:

FY	Pool	Direct Costs		
95	10	$1,847.58	$469.30	25.4%
		Total G&A	$10,956.86	

Non Value Added Costs:

FY	Direct Costs
95	$3,644.50

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

US DEPARTMENT, BUREAU, OR
ESTABLISHMENT AND LOCATION
DEFENSE ACCOUNTING OFFICE
DFAS-IN/EM-TP
FORT HUACHUCA, AZ

DTE VOU PREP: 95/02/03
SCHEDULE NUM:
VOUCHER NUM: 210567
CONTRACT NO AND DATE: DABT63-94C0017
PAID BY: M.E. BELZA, MAJ,FC
FORT HUACHUCA
REQUISITION NO & DATE: 95/02/03
6424

PAYEE'S NAME AND ADDRESS: BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMA
P.O BX 4340
BOSTON MA 02211

DISCOUNT TERMS

PAYEE'S ACCOUNT NUMBER

INVOICE NO: 7F

NUM & DT ORD	ARTICLES OR SERVICES	QTY CST	UNIT PRICE PER	AMOUNT
000001		1.00	1783.500000	1783

950230716430APS

TOTAL 1783.55

PAYMENT
_ PROVISIONAL
_ COMPLETE
X PARTIAL
_ FINAL
_ PROGRESS
_ ADVANCE

APPROVED BY

BY

TITLE

EXCHANGE RATE DIFF
=$1.00

AMT VER CORRECT 1783.55

SIGNATURE OR INITIALS: VE: 76 PMT NO: 011
AUT-CER: REEVES

PPA: 76

I CERTIFY THIS VOUCHER CORRECT AND PROPER FOR CHECK PAYMENT
95/02/03 M.E. BELZA
DEFENSE ACCOUNTING OFFICER

DATE AUTHORIZED CERTIFYING OFFICER TITLE

ACCOUNTING CLASSIFICATION

9740400.1301 00-5005 P4T10A8 2594 002086 US JWC900 00JW09 HJ1300400060552
ACCOUNTING AMOUNT: 1783.55

SF 1034-EDP PUBLIC VOUC[redacted] FOR PURCHASES AND SERVI[redacted] OTHER THAN PERSONAL

DEPARTMENT OF THE ARMY
DRAWER P
FT HUACHUCA, AZ 85613-6000

VOUCHER NO.

DATE PREPARED 01/20/95

CONTRACT NO./DATE DABT63-94-C-0017 04/05/94

P A I D B Y
Account of:
DSSN 6424

TAX ID
PAYEE'S NAME BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
ADDRESS P.O BX 4340
BOSTON MA 02211

FT HUACHUCA, AZ 85613-6000

DATE INVOICE RECV'D 01/05/95
DISCOUNT TERMS NET 30 DAYS

FOB:
DEST

NO./DATE OF ORDER	INV DATE	DATE OF PERFORMANCE INVRCV'D	MDSE DEL	MDSE ACPT	FREIGHT	MERCHANDISE
7F	11/09/94	01/05/95	01/05/95	01/10/95	0.00	1783.5

TOTAL: MDSE+ 1783.5

AMOUNT VERIFIED CORRECT FOR $$ 1783.5
SIGNATURE OR INITIALS: 76/

PAYMENT: 11PARTIAL 02/09/95

PURSUANT TO THE AUTHORITY VESTED IN ME, I CERTIFY THAT THIS VOUCHER IS CORRECT AND PROPER FOR PAYMENT.

AUTHORIZED CERTIFYING OFFICER: DATE: 01/20/95
FOR: For M.E.BELZA, MAJOR
DEFENSE ACCOUNTING OFFICER
Finance and Accounting Officer

ACCOUNTING CLASSIFICATIONS
97404001300100050O5P4T10A8410 2594 S02086 US JWC900 00JWC9 HJ150040060552 1783.5

PAYEE: BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
P.O BX 4340
BOSTON MA 02211

CHECK AMT $$ 1783.5

CHECK NO.: ON US TREASURY DATE:

Standard Form 1034
Revised January 1980
Department of the Treasury
I TFRM 4-2000
1034-120

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

VOUCHER NO. 7F

U.S. DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION
Defense Finance & Accounting SVC
Defense Accounting Office
Drawer P
Fort Huachuca, AZ 85613-6000

DATE VOUCHER PREPARED: 09 November 1994

SCHEDULE NO. 950706

CONTRACT NUMBER AND DATE: DABT63-94-C-0017

REQUISITION NUMBER AND DATE:

PAID BY

PAYEE'S NAME AND ADDRESS

BBN SYSTEMS AND TECHNOLOGIES
A Division of Bolt Beranek & Newman, Inc.
P.O. BOX 4340
BOSTON, MA 02211

Point of contact: Deb Veino @ (617) 873-2426

DATE INVOICE RECEIVED

DISCOUNT TERMS: 11592 1.1/10186

PAYEE'S ACCOUNT NUMBER

SHIPPED FROM TO WEIGHT

GOVERNMENT B/L NUMBER

NUMBER AND DATE OF ORDER	DATE OF DELIVERY OR SERVICE	ARTICLES OR SERVICES (Enter description, item number of contract or Federal supply schedule, and other information deemed necessary)	QUANTITY	UNIT PRICE COST	UNIT PRICE PER	AMOUNT
	01 Oct thru 31 Oct 1994	Total Fee for 01 October thru 31 October, 1994				
		Based on 26% completion X $35,671.00				$9,274.46
		Less Total Fee invoiced to date				7,490.91
		Total Amount Due This Invoice				
		COST REIMBURSABLE PROVISIONAL PAYMENT				

APPROVED FOR PAYMENT: $ ~~$1,783.55~~
I certify acceptance of ~~the~~ Supplies / Services herein on 5 Jan 95
Contracting Officer

(Use continuation sheet(s) if necessary) (Payee must NOT use the space below) TOTAL

DIFFERENCES: 5 Jan 95 Date

PAYMENT:
- ☐ PROVISIONAL
- ☐ COMPLETE
- ☐ PARTIAL
- ☐ FINAL
- ☐ PROGRESS
- ☐ ADVANCE

APPROVED FOR = $ Provisional Payment Subject to Later Audit

EXCHANGE RATE = $1.00

BY [2]

TITLE

Amount verified; correct for

(Signature or initials)

Pursuant to authority vested in me, I certify that this voucher is correct and proper for payment.

(Date) (Authorized Certifying Officer)[2] (Title)

ACCOUNTING CLASSIFICATION

PAID BY

CHECK NUMBER ON ACCOUNT OF U.S. TREASURY

CHECK NUMBER ON (Name of bank)

CASH $ DATE

PAYEE [3]

[1] When stated in foreign currency, insert name of currency.
[2] If the ability to certify and authority to approve are combined in one person, one signature only is necessary; otherwise the approving officer will sign in the space provided, over his official title.
[3] When a voucher is receipted in the name of a company or corporation, the name of the person writing the company or corporate name, as well as the capacity in which he signs, must appear. For example: "John Doe Company, per John Smith, Secretary", or "Treasurer", as the case may be.

PER

TITLE

Previous edition usable

* U.S.GPO:1987-0-181-247/40205

NSN 7540-00-634-4

FM

PRIVACY ACT STATEMENT
The information requested on this form is required under the provisions of 31 U.S.C. 82b and 82c, for the purpose of disbursing Federal money. The information requested is to identify the particular creditor and the amounts to be paid. Failure to furnish this information will hinder discharge of the payment obligation.

FORM 1035

CONTRACT NO. # DBAT63-94-C-0017

BBN REF. # 11592 1.1
BBN INVOICE # 950706
SHEET NO. # 2 OF 2
VOUCHER #7F

BBN Systems and Technologies
A Division of Bolt Beranek and Newman, Inc.
P.O. Box 4340
Boston, MA 02211

Target/Estimated Cost	$448,013.00
Target/Fixed Fee	35,671.00
Total	$483,684.00
85% Fixed Fee	$30,320.35

Disbursing Office: Defense Finance & Accounting SVC
Defense Accounting Office
Drawer P
Fort Huachuca, AZ 85613-6000

Fixed Fee:

Fixed Fee Due (26% X $35,671.00)	$9,274.46
Less Fixed Fee Billed	$7,490.91
Fixed Fee To Be Billed	$1,783.55

SF 1034-EDP PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

DEPARTMENT OF THE ARMY
DRAWER P
FT HUACHUCA, AZ 85613-6000

VOUCHER NO.

DATE PREPARED 01/11/95

CONTRACT NO./DATE DABT63--94-C-0017 04/05/94

P A I D B Y
Account of:
DSSN 6424

TAX ID
PAYEE'S NAME BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
ADDRESS P.O BX 4340
BOSTON MA 02211

FT HUACHUCA, AZ 85613-6000

DATE INVOICE RECV'D 12/24/94
DISCOUNT TERMS NET 30 DAYS

FOB:
DEST

NO./DATE OF ORDER	INV DATE	DATE OF PERFORMANCE INVRCV'D	MDSE DEL	MDSE ACPT	FREIGHT	MERCHANDISE
8C	12/19/94	12/24/94	11/30/94	12/24/94	0.00	58019.99
8F	12/19/94	12/24/94	11/30/94	12/24/94	0.00	4280.52

TOTAL: MDSE+ 62300.51

AMOUNT VERIFIED CORRECT FOR $$ 62300.51
SIGNATURE OR INITIALS: 76/

PAYMENT: 1OPARTIAL 01/23/95

PURSUANT TO THE AUTHORITY VESTED IN ME, I CERTIFY THAT THIS VOUCHER IS CORRECT AND PROPER FOR PAYMENT.

AUTHORIZED CERTIFYING OFFICER DATE: 01/11/95
FOR: For M.E.BELZA, MAJOR
DEFENSE ACCOUNTING OFFICER
Finance and Accounting Officer

ACCOUNTING CLASSIFICATIONS
97404001300100050O5P4T10A8410 2594 S02086 US JWC900 00JWC9 HJ150040060552 62300.51

PAYEE: BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
P.O BX 4340
BOSTON MA 02211

CHECK AMT $$ 62300.51

CHECK NO.: ON US TREASURY DATE:

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

US DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION DEFENSE ACCOUNTING OFFICE DFAS-IN/EM-TP FORT HUACHUCA, AZ	DTE VOU PREP 94/10/26 CONTRACT NO AND DATE DABT63-94C0017 REQUISITION NO & DATE	SCHEDULE NUM VOUCHER NUM Z02139 PAID BY M.E. BELZA, MAJ,FC FORT HUACHUCA 94/10/26 6424

PAYEE'S NAME AND ADDRESS: BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMA
P.O BX 4340
BOSTON MA 02211

DISCOUNT TERMS

PAYEE'S ACCOUNT NUMBER

NUM & DT ORD	ARTICLES OR SERVICES	QTY CST	UNIT PRICE PER	AMOUNT
000001		1.00	1783.550000	1783.

942990830003CAPS

TOTAL 1783.55

PAYMENT
_ PROVISIONAL
_ COMPLETE
X PARTIAL
_ FINAL
_ PROGRESS
_ ADVANCE

APPROVED BY

BY

TITLE

EXCHANGE RATE =$1.00

DIFF 8.90

AMT VER CORRECT 1795.19

SIGNATURE OR INITIALS: VE: 91 PMT NO: 006

AUT-CER: PALMER

PPA: 91

I CERTIFY THIS VOUCHER CORRECT AND PROPER FOR PAYMENT
94/10/26 M.E. BELZA DEFENSE ACCOUNTING OFFICER

DATE AUTHORIZED CERTIFYING OFFICER TITLE

ACCOUNTING CLASSIFICATION

9740400.1301 00-5005 P4T10A8 2594 002086 US JWC900 00JW @ HJ1500400060552

ACCOUNTING AMOUNT: 1795.19

CHECK NUMBER 02472958

SF 1034

SF 1034-EDP PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

DEFENSE FINANCE AND ACCOUNTING
DRAWER P
FT HUACHUCA, AZ 85613-6000

VOUCHER NO.

DATE PREPARED 10/25/94

CONTRACT NO./DATE DABT63-94-C-0017 04/05/94

P A I D B Y
Account of:
DSSN 6424

TAX ID
PAYEE'S NAME BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
ADDRESS P.O BX 4340
BOSTON MA 02211

FT HUACHUCA, AZ 85613-6000

DATE INVOICE RECV'D 08/23/94
DISCOUNT TERMS NET 30 DAYS

FOB:
DEST

NO./DATE OF ORDER	DATE OF PERFORMANCE INV DATE	INVRCV'D	MDSE DEL	MDSE ACPT	AMOUNT
4F	08/18/94	08/23/94	07/31/94	08/24/94	1783.55

TOTAL: MDSE+ 1783.55

INT+ 11.64

AMOUNT VERIFIED CORRECT FOR $$ 1795.19

SIGNATURE OR INITIALS: 91/

PAYMENT: 6PARTIAL 09/22/94

PURSUANT TO THE AUTHORITY VESTED IN ME, I CERTIFY THAT THIS VOUCHER IS CORRECT AND PROPER FOR PAYMENT.

AUTHORIZED CERTIFYING OFFICER

DATE: 10/25/94

FOR: For M.E.BELZA, MAJOR
DEFENSE ACCOUNTING OFFICER
DEFENSE ACCOUNTING OFFICER

ACCOUNTING CLASSIFICATIONS

97404001300100050O5P4T10A8410	2594	S02086	US	JWC900	00JWC9	HJ150040060552	1783.
21420200000057110532579 6UC000	43AB	S02086	US	7UUC00	007UUC	4C0017DIRCONTR	2.
21520200000057110532579 6W0000	43AB	S02086	US	7WE100	007WE1	4C0017DIRCONTR	8.

PAYEE: BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
P.O BX 4340
BOSTON MA 02211

CHECK AMT $$ 1795.

DCAA

CHECK NO.:

ON US TREASURY DATE:

Standard Form 1034
Revised January 1990
Department of the Treasury
I TFRM 6-2000
1034-120

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

VOUCHER NO: 4F

U.S. DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION
Defense Finance & Accounting SVC
Defense Accounting Office
Drawer P
Fort Huachuca, AZ 85613-6000

DATE VOUCHER PREPARED: 16 August 1994

CONTRACT NUMBER AND DATE: DABT63-94-C-0017

REQUISITION NUMBER AND DATE:

SCHEDULE NO: 950207

PAID BY:

PAYEE'S NAME AND ADDRESS

BBN SYSTEMS AND TECHNOLOGIES
A Division of Bolt Beranek & Newman, Inc.
P.O. BOX 4340
BOSTON, MA 02211

Point of contact: Deb Velno @ (617) 873-2426

DATE INVOICE RECEIVED:

DISCOUNT TERMS: 11592 1.1/10186

PAYEE'S ACCOUNT NUMBER:

SHIPPED FROM | TO | WEIGHT | GOVERNMENT B/L NUMBER

NUMBER AND DATE OF ORDER	DATE OF DELIVERY OR SERVICE	ARTICLES OR SERVICES (Enter description, item number of contract or Federal supply schedule, and other information deemed necessary)	QUANTITY	UNIT PRICE COST	UNIT PRICE PER	AMOUNT (1)
	01 Jul thru 31 Jul 1994	Total Fee for 01 July thru 31 July, 1994				
		Based on 15% completion X $35,671.00				$5,350.65
		Less Total Fee invoiced to date				3,567.10
		Total Amount Due This Invoice				$1,783.55
		COST REIMBURSABLE PROVISIONAL PAYMENT @ 1783.55				
(Use continuation sheet(s) if necessary)		(Payee must NOT use the space below)			TOTAL	

PAYMENT:
- ☐ PROVISIONAL
- ☐ COMPLETE
- ☐ PARTIAL
- ☐ FINAL
- ☐ PROGRESS
- ☐ ADVANCE

APPROVED FOR PROVISIONAL PAYMENT: $ — EXCHANGE RATE
Payment is subject to Letter Agt Supplies or Services herein.
I certify acceptance of the Supplies or 1.00
BY [2]
TITLE Contracting Officer — Date 8 Sep 94

DIFFERENCES:

Amount verified; correct for

(Signature or initials)

Pursuant to authority vested in me, I certify that this voucher is correct and proper for payment.

(Date) | (Authorized Certifying Officer)[1] | (Title)

ACCOUNTING CLASSIFICATION

PAID BY

CHECK NUMBER	ON ACCOUNT OF U.S. TREASURY	CHECK NUMBER	ON (Name of bank)
CASH $	DATE	PAYEE [3]	

[1] When stated in foreign currency, insert name of currency.
[2] If the ability to certify and authority to approve are combined in one person, one signature only is necessary; otherwise the approving officer will sign in the space provided, over his official title.
[3] When a voucher is receipted in the name of a company or corporation, the name of the person writing the company or corporate name, as well as the capacity in which he signs, must appear. For example: "John Doe Company, per John Smith, Secretary", or "Treasurer", as the case may be.

PER

TITLE

Previous edition usable

FM

* U.S.GPO:1987-0-181-247/40208

NSN 7540-00-634-42

PRIVACY ACT STATEMENT
The information requested on this form is required under the provisions of 31 U.S.C. 82b and 82c, for the purpose of disbursing Federal money. The information requested is to identify the particular creditor and the amounts to be paid. Failure to furnish this information will hinder discharge of the payment obligation.

WYCC:10 96-CZ-01

FORM 1035

CONTRACT NO. # DBAT63-94-C-0017

BBN REF. # 11592 1.1
BBN INVOICE # 950207
SHEET NO. # 2 OF 2
VOUCHER #4F

BBN Systems and Technologies
A Division of Bolt Beranek and Newman, Inc.
P.O. Box 4340
Boston, MA 02211

Target/Estimated Cost	$448,013.00
Target/Fixed Fee	35,671.00
Total	$483,684.00
85% Fixed Fee	$30,320.35

Disbursing Office: Defense Finance & Accounting SVC
Defense Accounting Office
Drawer P
Fort Huachuca, AZ 85613-6000

Fixed Fee:

Fixed Fee Due (15% X $35,671.00)	$5,350.65
Less Fixed Fee Billed	3,567.10
Fixed Fee To Be Billed	$1,783.55

10-25-94 07:55AM

SF 1034

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

US DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION DEFENSE ACCOUNTING OFFICE DFAS-IN/EM-TP FORT HUACHUCA, AZ	DTE VOU PREP 94/11/21 CONTRACT NO AND DATE DABT63-94C0017 REQUISITION NO & DATE	SCHEDULE NUM VOUCHER NUM 204129 PAID BY M.E. BELZA, MAJ,FC FORT HUACHUCA 94/11/21 6424

PAYEE'S NAME AND ADDRESS: BBN SYSTEMS & TECHNOLOGIES DIV OF BOLT BERANEK & NEWMA P.O BX 4340 BOSTON MA 02211

DISCOUNT TERMS

PAYEE'S ACCOUNT NUMBER

NUM & DT ORD	ARTICLES OR SERVICES	QTY CST	UNIT PRICE PER	AMOUNT
000001		1.00	12775.380000	12775

943250728O2CAPS

TOTAL 12775.38

PAYMENT
_ PROVISIONAL
_ COMPLETE
X PARTIAL
_ FINAL
_ PROGRESS
_ ADVANCE

APPROVED BY

BY

TITLE

EXCHANGE RATE =$1.00

DIFF

AMT VER CORRECT 12775.38

SIGNATURE OR INITIALS: VE: 92 PMT NO: 007

AUT-CER: PALMER

PPA: 92

I CERTIFY THIS VOUCHER CORRECT AND PROPER FOR CHECK PAYMENT

94/11/21 M.E. BELZA DEFENSE ACCOUNTING OFFICER

DATE AUTHORIZED CERTIFYING OFFICER TITLE

ACCOUNTING CLASSIFICATION

9740400.1301 00-5005 P4T10A8 2594 002086 US JWC900 00JWC9 HJ150040060552

ACCOUNTING AMOUNT: 12775.38

SF 1034-EDP PUBLIC VOUCH[illegible] FOR PURCHASES AND SERVIC[illegible] OTHER THAN PERSONAL

DEPARTMENT OF THE ARMY
DRAWER P'
FT HUACHUCA, AZ 85613-6000

VOUCHER NO.

DATE PREPARED 11/19/94

CONTRACT NO./DATE DABT63-94-C-0017 04/05/94

P A I D B Y
Account of:
DSSN 6424

TAX ID
PAYEE'S NAME BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
ADDRESS P.O BX 4340
BOSTON MA 02211

FT HUACHUCA, AZ 85613-6000

DATE INVOICE RECV'D 10/25/94
DISCOUNT TERMS NET 30 DAYS

FOB:
DEST

NO./DATE OF ORDER	DATE OF PERFORMANCE INV DATE	INVRCV'D	MDSE DEL	MDSE ACPT	AMOUNT
6C	10/21/94	10/25/94	10/21/94	10/21/94	11705.25
6F	10/21/94	10/25/94	10/25/94	10/25/94	1070.13

TOTAL: MDSE+ 12775.38

AMOUNT VERIFIED CORRECT FOR $$ 12775.38
SIGNATURE OR INITIALS: 92/

PAYMENT: 7PARTIAL 11/25/94

PURSUANT TO THE AUTHORITY VESTED IN ME, I CERTIFY THAT THIS VOUCHER IS CORRECT AND PROPER FOR PAYMENT.

AUTHORIZED CERTIFYING OFFICER DATE: 11/19/94
FOR: For M.E.BELZA, MAJOR
DEFENSE ACCOUNTING OFFICER
Finance and Accounting Officer

ACCOUNTING CLASSIFICATIONS
9740400130010005005P4T10A8410 2594 S02086 US JWC900 00JWC9 HJ150040060552 12775.38

PAYEE: BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
P.O BX 4340
BOSTON MA 02211

CHECK AMT $$ 12775.38

CHECK NO.: ON US TREASURY DATE:

BT 201 11/2

Standard Form 1034
Revised January 1990
Department of the Treasury
I TFRM 4-2000
1034-120

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

VOUCHER NO. 6C

U.S. DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION
D.C.A.A.
WALTHAM BRANCH
424 TRAPELLO RD
WALTHAM, MA 02154-6397

DATE VOUCHER PREPARED: 21 October 1994

SCHEDULE NO.: 950586

CONTRACT NUMBER AND DATE: DABT63-94-C-0017

REQUISITION NUMBER AND DATE:

PAID BY:

PAYEE'S NAME AND ADDRESS

BBN SYSTEMS AND TECHNOLOGIES
A Division of Bolt Beranek & Newman, Inc.
P.O. BOX 4340
BOSTON, MA 02211

Point of contact: Deb Veino @ (617) 873-2426

DATE INVOICE RECEIVED:

DISCOUNT TERMS: 11592 1.1/10186

PAYEE'S ACCOUNT NUMBER:

SHIPPED FROM | TO | WEIGHT | GOVERNMENT B/L NUMBER

NUMBER AND DATE OF ORDER	DATE OF DELIVERY OR SERVICE	ARTICLES OR SERVICES (Enter description, item number of contract or Federal supply schedule, and other information deemed necessary)	QUANTITY	UNIT PRICE COST	UNIT PRICE PER	AMOUNT (1)
	01 Sep thru 30 Sep 1994	For detail, see SF 1035 continuation sheet. Total amount claimed transferred from Page 2, SF 1035 COST REIMBURSABLE PROVISIONAL PAYMENT				$11,705.25

(Use continuation sheet(s) if necessary) **(Payee must NOT use the space below)** **TOTAL** $11,705.25

PAYMENT:
- ☐ PROVISIONAL
- ☐ COMPLETE
- ☐ PARTIAL
- ☐ FINAL
- ☐ PROGRESS
- ☐ ADVANCE

APPROVED FOR: Provisional =$ Payment Subject to Later Audit

EXCHANGE RATE =$1.00

DIFFERENCES

BY [2] A. Reynolds

Amount verified; correct for

TITLE: Auditor, Defense Contract Audit Agency

(Signature or initials)

Pursuant to authority vested in me, I certify that this voucher is correct and proper for payment.

(Date) | (Authorized Certifying Officer)[2] | (Title)

ACCOUNTING CLASSIFICATION

PAID BY

CHECK NUMBER	ON ACCOUNT OF U.S. TREASURY	CHECK NUMBER	ON (Name of bank)
CASH $	DATE	PAYEE [3]	

[1] When stated in foreign currency, insert name of currency.
[2] If the ability to certify and authority to approve are combined in one person, one signature only is necessary; otherwise the approving officer will sign in the space provided, over his official title.
[3] When a voucher is receipted in the name of a company or corporation, the name of the person writing the company or corporate name, as well as the capacity in which he signs, must appear. For example: "John Doe Company, per John Smith, Secretary", or "Treasurer", as the case may be.

PER

TITLE

Previous edition usable

★U.S.GPO:1987-0-181-247/40205

NSN 7540-00-634-4206

PM

PRIVACY ACT STATEMENT
The information requested on this form is required under the provisions of 31 U.S.C. 82b and 82c, for the purpose of disbursing Federal money. The information requested is to identify the particular creditor and the amounts to be paid. Failure to furnish this information will hinder discharge of the payment obligation.

Standard Form 1034
Revised January 1980
Department of the Treasury
1 TFRM 4-2000
1034-120

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

VOUCHER NO. 6C

U.S. DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION
D.C.A.A.
WALTHAM BRANCH
424 TRAPELLO RD
WALTHAM, MA 02154-6397

DATE VOUCHER PREPARED: 21 October 1994

SCHEDULE NO. 950586

CONTRACT NUMBER AND DATE: DABT63-94-C-0017

REQUISITION NUMBER AND DATE:

PAID BY

PAYEE'S NAME AND ADDRESS

BBN SYSTEMS AND TECHNOLOGIES
A Division of Bolt Beranek & Newman, Inc.
P.O. BOX 4340
BOSTON, MA 02211

Point of contact: Deb Veino @ (617) 873-2426

DATE INVOICE RECEIVED

DISCOUNT TERMS: 11592 1.1/10186

PAYEE'S ACCOUNT NUMBER

SHIPPED FROM | TO | WEIGHT | GOVERNMENT B/L NUMBER

NUMBER AND DATE OF ORDER	DATE OF DELIVERY OR SERVICE	ARTICLES OR SERVICES (Enter description, item number of contract or Federal supply schedule, and other information deemed necessary)	QUANTITY	UNIT PRICE COST	UNIT PRICE PER	AMOUNT (1)
	01 Sep thru 30 Sep 1994	For detail, see SF 1035 continuation sheet. Total amount claimed transferred from Page 2, SF 1035 COST REIMBURSABLE PROVISIONAL PAYMENT				$11,705.25

(Use continuation sheet(s) if necessary) **(Payee must NOT use the space below)** **TOTAL** $11,705.25

PAYMENT:
- ☐ PROVISIONAL
- ☐ COMPLETE
- ☐ PARTIAL
- ☐ FINAL
- ☐ PROGRESS
- ☐ ADVANCE

APPROVED FOR Provisional =$ Payment Subject to Later Audit

EXCHANGE RATE =$1.00

BY [2] A. Reynolds

TITLE Auditor, Defense Contract Audit Agency

DIFFERENCES

Amount verified; correct for

(Signature or initials)

Pursuant to authority vested in me, I certify that this voucher is correct and proper for payment.

(Date) (Authorized Certifying Officer)[2] (Title)

ACCOUNTING CLASSIFICATION

PAID BY

CHECK NUMBER ON ACCOUNT OF U.S. TREASURY | CHECK NUMBER ON (Name of bank)

CASH $ DATE | PAYEE [3]

[1] When stated in foreign currency, insert name of currency.
[2] If the ability to certify and authority to approve are combined in one person, one signature only is necessary; otherwise the approving officer will sign in the space provided, over his official title.
[3] When a voucher is receipted in the name of a company or corporation, the name of the person writing the company or corporate name, as well as the capacity in which he signs, must appear. For example: "John Doe Company, per John Smith, Secretary", or "Treasurer", as the case may be.

PER

TITLE

Previous edition usable

*U.S.GPO:1987-0-181-247/40205

NSN 7540-00-634-4206

PM

PRIVACY ACT STATEMENT
The information requested on this form is required under the provisions of 31 U.S.C. 82b and 82c, for the purpose of disbursing Federal money. The information requested is to identify the particular creditor and the amounts to be paid. Failure to furnish this information will hinder discharge of the payment obligation.

FORM 1035

CONTRACT NO. # DBAT63-94-C-0017

BBN REF. # 11592 1.1
BBN INVOICE # 950586
SHEET NO. # 2 OF 3
VOUCHER #6C

BBN Systems and Technologies
A Division of Bolt Beranek and Newman, Inc.
P.O. Box 4340
Boston, MA 02211

Target/Estimated Cost	$448,013.00
Target/Fixed Fee	35,671.00
Total	$483,684.00
85% Fixed Fee	$30,320.35

Disbursing Office: Defense Finance & Accounting SVC
Defense Accounting Office
Drawer P
Fort Huachuca, AZ 85613-6000

Withholding Clause:
BBN Withholding:

Analysis of Current and Cumulative Costs and Fee Earned:

Major Cost Elements:	Amount for Current Period Billed	Cumulative Amounts From Inception to Date of This Billing
Direct Labor	$3,725.87	$33,149.74
Overhead	4,295.93	39,222.27
Travel	0.00	1,120.00
Material	1,067.12	1,067.12
Procurement Charge	75.16	76.66
Equipment/Software Rental	436.25	436.25
Books & Subscriptions	0.00	30.00
Postage & Express Mail	0.00	9.00
Training Conference	0.00	150.00
General Administration	2,056.61	18,203.01
Total Cost	$11,656.94	$93,464.05
CAS414	48.31	431.23
TOTAL	$11,705.25	$93,895.28

Continuation Sheet - Page # 3
BBN Reference # 11592 1.1
Bureau Voucher # 6C
Invoice # 950586

Direct Labor:

FY	Pool	Hours	Direct Labor	Overhead	Overhead Rate	G&A	G&A Rate
95	10	152.8	$3,725.87	$4,295.93	115.3%	$2,037.53	25.4%
		152.8	$3,725.87	$4,295.93			

Other Direct Costs:

Value Added Costs:

FY	Pool	Direct Costs			
95	0	$75.16		$19.08	25.4%
		$75.16	Total G&A	$2,056.61	

Non Value Added Costs:

FY	Direct Costs
95	$1,503.37
	$1,503.37

Standard Form 1034
Revised January 1980
Department of the Treasury
I TFRM 4-2000
1034-120

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

VOUCHER NO. 6F

U.S. DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION
Defense Finance & Accounting SVC
Defense Accounting Office
Drawer P
Fort Huachuca, AZ 85613-6000

DATE VOUCHER PREPARED: 21 October 1994

SCHEDULE NO. 950586

CONTRACT NUMBER AND DATE: DABT63-94-C-0017

REQUISITION NUMBER AND DATE:

PAID BY

PAYEE'S NAME AND ADDRESS

BBN SYSTEMS AND TECHNOLOGIES
A Division of Bolt Beranek & Newman, Inc.
P.O. BOX 4340
BOSTON, MA 02211

Point of contact: Deb Veino @ (617) 873-2426

DATE INVOICE RECEIVED

DISCOUNT TERMS: 11592 1.1/10186

PAYEE'S ACCOUNT NUMBER

SHIPPED FROM | TO | WEIGHT | GOVERNMENT B/L NUMBER

NUMBER AND DATE OF ORDER	DATE OF DELIVERY OR SERVICE	ARTICLES OR SERVICES (Enter description, item number of contract or Federal supply schedule, and other information deemed necessary)	QUANTITY	UNIT PRICE COST	UNIT PRICE PER	AMOUNT (1)
	01 Sep thru 30 Sep 1994	Total Fee for 01 September thru 30 September, 1994				
		Based on 21% completion X $35,671.00				$7,490.91
		Less Total Fee invoiced to date				6,420.78
		Total Amount Due This Invoice				$1,070.13
		COST REIMBURSABLE PROVISIONAL PAYMENT				

APPROVED FOR PAYMENT: $ ~~$1,070.13~~
I certify acceptance of the ~~Supplies~~ or Services therein on 25 Oct 94
Patricia Bosnell

(Use continuation sheet(s) if necessary) (Payee must NOT use the space below) TOTAL

PAYMENT:
- ☐ PROVISIONAL
- ☐ COMPLETE
- ☐ PARTIAL
- ☐ FINAL
- ☐ PROGRESS
- ☐ ADVANCE

APPROVED FOR Provisional Payment $ Subject to Later Audit

EXCHANGE RATE Contracting Officer = $1:00

DIFFERENCES 25 Oct 94 Date

BY [2]

Amount verified; correct for

TITLE

(Signature or initials)

Pursuant to authority vested in me, I certify that this voucher is correct and proper for payment.

(Date) (Authorized Certifying Officer)[2] (Title)

ACCOUNTING CLASSIFICATION

PAID BY

CHECK NUMBER | ON ACCOUNT OF U.S. TREASURY | CHECK NUMBER | ON (Name of bank)

CASH $ | DATE | PAYEE [3]

[1] When stated in foreign currency, insert name of currency.
[2] If the ability to certify and authority to approve are combined in one person, one signature only is necessary; otherwise the approving officer will sign in the space provided, over his official title.
[3] When a voucher is receipted in the name of a company or corporation, the name of the person writing the company or corporate name, as well as the capacity in which he signs, must appear. For example: "John Doe Company, per John Smith, Secretary", or "Treasurer", as the case may be.

PER

TITLE

Previous edition usable

*U.S.GPO:1987-0-181-247/40205

NSN 7540-00-634-4206

PM

PRIVACY ACT STATEMENT
The information requested on this form is required under the provisions of 31 U.S.C. 82b and 82c, for the purpose of disbursing Federal money. The information requested is to identify the particular creditor and the amounts to be paid. Failure to furnish this information will hinder discharge of the payment obligation.

FORM 1035

CONTRACT NO. # DBAT63-94-C-0017

BBN REF. # 11592 1.1
BBN INVOICE # 950586
SHEET NO. # 2 OF 2
VOUCHER #6F

BBN Systems and Technologies
A Division of Bolt Beranek and Newman, Inc.
P.O. Box 4340
Boston, MA 02211

Target/Estimated Cost	$448,013.00
Target/Fixed Fee	35,671.00
Total	$483,684.00
85% Fixed Fee	$30,320.35

Disbursing Office: Defense Finance & Accounting SVC
Defense Accounting Office
Drawer P
Fort Huachuca, AZ 85613-6000

Fixed Fee:

Fixed Fee Due (21% X $35,671.00)	$7,490.91
Less Fixed Fee Billed	6,420.78
Fixed Fee To Be Billed	$1,070.13

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

US DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION DEFENSE ACCOUNTING OFFICE DFAS-IN/EM-TP FORT HUACHUCA, AZ	DTE VOU PREP 94/12/13 CONTRACT NO AND DATE DABT63-94C0017 REQUISITION NO & DATE	SCHEDULE NUM PAID BY M.E. BELZA, MAJ,FC FORT HUACHUCA 94/12/13 6424

VOUCHER NUM 206226

PAYEE'S NAME AND ADDRESS: BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMA
P.O BX 4340
BOSTON MA 02211

DISCOUNT TERMS

PAYEE'S ACCOUNT NUMBER

INVOICE NO: 7C

NUM & DT ORD	ARTICLES OR SERVICES	QTY CST	UNIT PRICE PER	AMOUNT
000001		1.00	22534.210000	22534.

9434608560ZCAPS

TOTAL 22534.21

PAYMENT
_ PROVISIONAL
_ COMPLETE
X PARTIAL
_ FINAL
_ PROGRESS
_ ADVANCE

APPROVED BY

BY

TITLE

EXCHANGE RATE DIFF
=$1.00

AMT VER CORRECT 22534.21

SIGNATURE OR INITIALS: VE: 76 PMT NO: 008

AUT-CER: REEVES

PPA: 76

I CERTIFY THIS VOUCHER CORRECT AND PROPER FOR CHECK PAYMENT

94/12/13 M.E. BELZA DEFENSE ACCOUNTING OFFICER

DATE AUTHORIZED CERTIFYING OFFICER TITLE

ACCOUNTING CLASSIFICATION

9740400.1301 00-5005 P4T10A8 2594 002086 US JWC900 00JWC9 HJ150040060552

ACCOUNTING AMOUNT: 22534.21

CHECK NUMBER 02402725

SF 1034-EDP PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

DEPARTMENT OF THE ARMY
DRAWER P
FT HUACHUCA, AZ 85613-6000

VOUCHER NO.

DATE PREPARED 12/09/94

CONTRACT NO./DATE DABT63-94-C-0017 04/05/94

P A I D B Y
Account of:
DSSN 6424

TAX ID
PAYEE'S NAME BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
ADDRESS P.O BX 4340
BOSTON MA 02211

FT HUACHUCA, AZ 85613-6000

DATE INVOICE RECV'D 11/17/94 FOB:
DISCOUNT TERMS NET 30 DAYS DEST

NO./DATE OF ORDER	INV DATE	DATE OF PERFORMANCE INVRCV'D	MDSE DEL	MDSE ACPT	FREIGHT	MERCHANDISE
7C	11/10/94	11/17/94	10/31/94	11/14/94	0.00	22534.21

TOTAL: MDSE+ 22534.21

AMOUNT VERIFIED CORRECT FOR $$ 22534.21
SIGNATURE OR INITIALS: 76/

PAYMENT: 8PARTIAL 12/19/94

PURSUANT TO THE AUTHORITY VESTED IN ME, I CERTIFY THAT THIS VOUCHER IS CORRECT AND PROPER FOR PAYMENT.

AUTHORIZED CERTIFYING OFFICER DATE: 12/09/94
FOR: For M.E.BELZA, MAJOR
DEFENSE ACCOUNTING OFFICER
Finance and Accounting Officer

ACCOUNTING CLASSIFICATIONS
97404001300100050O5P4T10A8410 2594 S02086 US JWC900 00JWC9 HJ150040060552 22534.2

PAYEE: BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
P.O BX 4340
BOSTON MA 02211

CHECK AMT $$ 22534.2

CHECK NO.: ON US TREASURY DATE:

Standard Form 1034
Revised January 1980
Department of the Treasury
I TFRM 4-2000
1034-120

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

VOUCHER NO. 7C

U.S. DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION
D.C.A.A.
WALTHAM BRANCH
424 TRAPELLO RD
WALTHAM, MA 02154-6397

DATE VOUCHER PREPARED: 10 November 1994

SCHEDULE NO. 950706

CONTRACT NUMBER AND DATE: DABT63-94-C-0017

REQUISITION NUMBER AND DATE:

PAID BY

PAYEE'S NAME AND ADDRESS

BBN SYSTEMS AND TECHNOLOGIES
A Division of Bolt Beranek & Newman, Inc.
P.O. BOX 4340
BOSTON, MA 02211

Point of contact: Deb Veino @ (617) 873-2426

DATE INVOICE RECEIVED

DISCOUNT TERMS

PAYEE'S ACCOUNT NUMBER: 11592 1.1/10186

SHIPPED FROM | TO | WEIGHT | GOVERNMENT B/L NUMBER

NUMBER AND DATE OF ORDER	DATE OF DELIVERY OR SERVICE	ARTICLES OR SERVICES (Enter description, item number of contract or Federal supply schedule, and other information deemed necessary)	QUANTITY	UNIT PRICE COST	UNIT PRICE PER	AMOUNT (1)
	01 Oct thru 31 Oct 1994	For detail, see SF 1035 continuation sheet. Total amount claimed transferred from Page 2, SF 1035 COST REIMBURSABLE PROVISIONAL PAYMENT				$22,534.21

(Use continuation sheet(s) if necessary) **(Payee must NOT use the space below)** TOTAL $22,534.21

PAYMENT:
- ☐ PROVISIONAL
- ☐ COMPLETE
- ☐ PARTIAL
- ☐ FINAL
- ☐ PROGRESS
- ☐ ADVANCE

APPROVED FOR: Provisional Payment Subject to Later Audit

EXCHANGE RATE: =$1.00

DIFFERENCES

BY [2]: A. Reynolds

TITLE: Auditor, Defense Contract Audit Agency

Amount verified; correct for

(Signature or initials)

Pursuant to authority vested in me, I certify that this voucher is correct and proper for payment.

(Date) | (Authorized Certifying Officer)[2] | (Title)

ACCOUNTING CLASSIFICATION

PAID BY

CHECK NUMBER | ON ACCOUNT OF U.S. TREASURY | CHECK NUMBER | ON (Name of bank)

CASH $ | DATE | PAYEE [3]

[1] When stated in foreign currency, insert name of currency.
[2] If the ability to certify and authority to approve are combined in one person, one signature only is necessary; otherwise the approving officer will sign in the space provided, over his official title.
[3] When a voucher is receipted in the name of a company or corporation, the name of the person writing the company or corporate name, as well as the capacity in which he signs, must appear. For example: "John Doe Company, per John Smith, Secretary", or "Treasurer", as the case may be.

PER

TITLE

Previous edition usable

★U.S.GPO:1987-0-181-247/40205

NSN 7540-00-634-4206

PK

PRIVACY ACT STATEMENT
The information requested on this form is required under the provisions of 31 U.S.C. 82b and 82c, for the purpose of disbursing Federal money. The information requested is to identify the particular creditor and the amounts to be paid. Failure to furnish this information will hinder discharge of the payment obligation.

FORM 1035

CONTRACT NO. # DBAT63-94-C-0017

BBN REF. # 11592 1.1
BBN INVOICE # 950706
SHEET NO. # 2 OF 3
VOUCHER #7C

BBN Systems and Technologies
A Division of Bolt Beranek and Newman, Inc.
P.O. Box 4340
Boston, MA 02211

Target/Estimated Cost	$448,013.00
Target/Fixed Fee	35,671.00
Total	$483,684.00
85% Fixed Fee	$30,320.35

Disbursing Office: Defense Finance & Accounting SVC
Defense Accounting Office
Drawer P
Fort Huachuca, AZ 85613-6000

Withholding Clause:
BBN Withholding:

Analysis of Current and Cumulative Costs and Fee Earned:

Major Cost Elements:	Amount for Current Period Billed	Cumulative Amounts From Inception to Date of This Billing
Direct Labor	$7,922.82	$41,072.56
Overhead	9,135.01	48,357.28
Travel	394.00	1,514.00
Material	514.46	1,581.58
Procurement Charge	25.72	102.38
Equipment/Software Rental	0.00	436.25
Books & Subscriptions	0.00	30.00
Postage & Express Mail	0.00	9.00
Training Conference	0.00	150.00
General Administration	4,439.28	22,642.29
Total Cost	$22,431.29	$115,895.34
CAS414	102.92	534.15
TOTAL	$22,534.21	$116,429.49

Continuation Sheet - Page # 3
BBN Reference # 11592 1.1
Bureau Voucher # 7C
Invoice # 950706

Direct Labor:

FY	Pool	Hours	Direct Labor	Overhead	Overhead Rate	G&A	G&A Rate
95	10	199.5	$7,922.82	$9,135.01	115.3%	$4,332.68	25.4%

Other Direct Costs:

Value Added Costs:

FY	Pool	Direct Costs			
95	0	$419.72		$106.60	25.4%
			Total G&A	$4,439.28	

Non Value Added Costs:

FY	Direct Costs
95	$514.46

1034-EDP PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

RTMENT OF THE ARMY
ER P
JACHUCA, AZ 85613-6000

VOUCHER NO.

DATE PREPARED 09/02/94

RACT NO./DATE DABT63-94-C-0017 04/05/94

PAID BY
Account of:
DSSN 6424

ID
E'S BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
ESS P.O BX 4340
BOSTON MA 02211

FT HUACHUCA, AZ 85613-6000

INVOICE RECV'D 08/10/94
OUNT TERMS NET 30 DAYS

FOB:
DEST

DATE ORDER	DATE OF PERFORMANCE INV DATE	INVRCV'D	MDSE DEL	MDSE ACPT	AMOUNT
3C	08/05/94	08/10/94	08/05/94	08/05/94	15112.76
4C	08/18/94	08/10/94	07/01/94	07/31/94	25347.93

TOTAL: MDSE+ 40460.69

AMOUNT VERIFIED CORRECT FOR $$ 40460.69
SIGNATURE OR INITIALS: 90/

ENT: 4PARTIAL 09/09/94

UANT TO THE AUTHORITY VESTED IN ME, I CERTIFY THAT THIS VOUCHER IS CORRECT
PROPER FOR PAYMENT.

IORIZED CERTIFYING OFFICER DATE: 09/02/94
FOR: M.E.BELZA
DEFENSE ACCOUNTING OFFICER
Finance and Accounting Officer

OUNTING CLASSIFICATIONS

400130010005005P4T10A8410	2594	S02086	US	JWC900	00JWC9	HJ1500400060552	40460.69

EE: BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
P.O BX 4340
BOSTON MA 02211

CHECK AMT $$ 40460.69

CK NO.: ON US TREASURY DATE:

ATZS-RMP

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

US DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION DEFENSE ACCOUNTING OFFICE DFAS-IN/FM-TP FORT HUACHUCA, AZ	DATE VOU PREP 04/09/2006 CONTRACT NO AND DATE DABT03-94C0017 REQUISITION NO & DATE	SCHED NUM DUE DISC PAY VOUCHER NUM 2004263 Y EFT PAY ITEM JA74CCA CS

PAYEE'S NAME AND ADDRESS: BRN SYSTEMS & TECHNOLOGIES DIV OF RELT ERANKR S NEWMA P.O BX 4040 BOSTON MA 02211

ACCOUNT TERMS

PAYEE'S ACCOUNT NUMBER

ITEM & SUBORD NO	ARTICLES OR SERVICES	QTY	UNIT COST	PRICE PER	AMOUNT
0001		1.00	40		

9124090404 APS

TOTAL

PAYMENT
PROVISIONAL
COMPLETE
X PARTIAL
FINAL
PROGRESS
ADVANCE

APPROVED BY

EXCHANGE RATE

TITLE

SIGNATURE OR INITIALS: V/C 90 PMT NO: 004 CORRECT

AUT-CER: REEVES

PFAC: 90

I CERTIFY THIS VOUCHER CORRECT AND PROPER FOR PAYMENT
04/09/06 M.E. BELZA DEFENSE ACCOUNTING OFFICER

DATE AUTHORIZED CERTIFYING OFFICER TITLE

ACCOUNTING CLASSIFICATION

9740400.1301 00-5005 P4T10A8 2594 002098 US 000000 0000000 S15004A06CB

ACCOUNTING AMOUNT:

CHECK NUMBER 02462407

SF 1034

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

US DEPARTMENT, BUREAU, OR
ESTABLISHMENT AND LOCATION
DEFENSE ACCOUNTING OFFICE
DFAS-IN/EM-TP
FORT HUACHUCA, AZ

DTE VOU PREP: 94/10/13
SCHEDULE NUM:
VOUCHER NUM: 201241
CONTRACT NO AND DATE: DABT63-94C0017
REQUISITION NO & DATE:

PAID BY
M.E. BELZA, MAJ,FC
FORT HUACHUCA
94/10/13
6424

PAYEE'S NAME AND ADDRESS: BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMA
P.O BX 4340
BOSTON MA 02211

DISCOUNT TERMS

PAYEE'S ACCOUNT NUMBER

NUM & DT ORD	ARTICLES OR SERVICES	QTY CST	UNIT PRICE PER	AMOUNT
000001		1.00	14889.050000	14889.

94276090529CAPS

TOTAL 14889.05

PAYMENT
_ PROVISIONAL
_ COMPLETE
X PARTIAL
_ FINAL
_ PROGRESS
_ ADVANCE

APPROVED BY
BY
TITLE

EXCHANGE RATE DIFF
=$1.00

AMT VER CORRECT 14889.05

SIGNATURE OR INITIALS: VE: 92 PMT NO: 005
AUT-CER: REEVES

PPA: 92

I CERTIFY THIS VOUCHER CORRECT AND PROPER FOR PAYMENT
94/10/13 M.E. BELZA
DEFENSE ACCOUNTING OFFICER

DATE AUTHORIZED CERTIFYING OFFICER TITLE

ACCOUNTING CLASSIFICATION

9740400.1301 00-5005 P4T10A8 2594 002086 US JWC900 00JWC9 HJ150040060552
ACCOUNTING AMOUNT: 14889.05

CHECK NUMBER 02470552

SF 1034

SF 1034-EDF PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

DEPARTMENT OF THE ARMY
DRAWER P
FT HUACHUCA, AZ 85613-6000

VOUCHER NO.

DATE PREPARED 09/30/94

CONTRACT NO./DATE DABT63-94-C-0017 04/05/94

P A I D B Y
Account of:
DSSN 6424

TAX ID
PAYEE'S NAME BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
ADDRESS P.O BX 4340
BOSTON MA 02211

FT HUACHUCA, AZ 85613-6000

DATE INVOICE RECV'D 09/19/94
DISCOUNT TERMS NET 30 DAYS

FOB:
DEST

NO./DATE OF ORDER	DATE OF PERFORMANCE INV DATE	INVRCV'D	MDSE DEL	MDSE ACPT	AMOUNT
5C	09/14/94	09/19/94	09/19/94	09/19/94	13818.92
5F	09/14/94	09/20/94	09/20/94	09/20/94	1070.13

TOTAL: MDSE+ 14889.05

AMOUNT VERIFIED CORRECT FOR $$ 14889.05
SIGNATURE OR INITIALS: 92/

PAYMENT: 5PARTIAL 10/19/94

PURSUANT TO THE AUTHORITY VESTED IN ME, I CERTIFY THAT THIS VOUCHER IS CORRECT AND PROPER FOR PAYMENT.

AUTHORIZED CERTIFYING OFFICER DATE: 09/30/94
FOR: M.E.BELZA
DEFENSE ACCOUNTING OFFICER
Finance and Accounting Officer

ACCOUNTING CLASSIFICATIONS
97404001300100050O5P4T10A8410 2594 S02086 US JWC900 00JWC9 HJ150040060552 14889.0

PAYEE: BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
P.O BX 4340
BOSTON MA 02211

CHECK AMT $$ 14889.0

CHECK NO.: ON US TREASURY DATE:

A

Standard Form 1034
Revised January 1980
Department of the Treasury
1 TFRM 4-2000
1034-120

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

VOUCHER NO. 5C

U.S. DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION
D.C.A.A.
WALTHAM BRANCH
424 TRAPELLO RD
WALTHAM, MA 02154-6397

DATE VOUCHER PREPARED: 14 September 1994

SCHEDULE NO. 950352

CONTRACT NUMBER AND DATE: DABT63-94-C-0017

REQUISITION NUMBER AND DATE:

PAID BY

PAYEE'S NAME AND ADDRESS

BBN SYSTEMS AND TECHNOLOGIES
A Division of Bolt Beranek & Newman, Inc.
P.O. BOX 4340
BOSTON, MA 02211

Point of contact: Deb Veino @ (617) 873-2426

DATE INVOICE RECEIVED

DISCOUNT TERMS: 11592 1.1/10186

PAYEE'S ACCOUNT NUMBER

SHIPPED FROM | TO | WEIGHT | GOVERNMENT B/L NUMBER

NUMBER AND DATE OF ORDER	DATE OF DELIVERY OR SERVICE	ARTICLES OR SERVICES (Enter description, item number of contract or Federal supply schedule, and other information deemed necessary)	QUANTITY	UNIT PRICE COST	UNIT PRICE PER	AMOUNT (1)
	01 Aug thru 31 Aug 1994	For detail, see SF 1035 continuation sheet. Total amount claimed transferred from Page 2, SF 1035 COST REIMBURSABLE PROVISIONAL PAYMENT				$13,818.92

(Use continuation sheet(s) if necessary) **(Payee must NOT use the space below)** TOTAL $13,818.92

PAYMENT:
- ☐ PROVISIONAL
- ☐ COMPLETE
- ☐ PARTIAL
- ☐ FINAL
- ☐ PROGRESS
- ☐ ADVANCE

APPROVED FOR: Provisional Payment Subject to Later Audit

EXCHANGE RATE = $1.00

BY [2]: A. Reynolds

TITLE: Auditor, Defense Contract Audit Agency

DIFFERENCES

Amount verified; correct for

(Signature or initials)

Pursuant to authority vested in me, I certify that this voucher is correct and proper for payment.

(Date) | (Authorized Certifying Officer)[2] | (Title)

ACCOUNTING CLASSIFICATION

PAID BY

CHECK NUMBER | ON ACCOUNT OF U.S. TREASURY | CHECK NUMBER | ON (Name of bank)

CASH $ | DATE | PAYEE [3]

[1] When stated in foreign currency, insert name of currency.
[2] If the ability to certify and authority to approve are combined in one person, one signature only is necessary; otherwise the approving officer will sign in the space provided, over his official title.
[3] When a voucher is receipted in the name of a company or corporation, the name of the person writing the company or corporate name, as well as the capacity in which he signs, must appear. For example: "John Doe Company, per John Smith, Secretary", or "Treasurer", as the case may be.

PER

TITLE

Previous edition usable

★U.S.GPO:1987-0-181-247/40205

NSN 7540-00-634-4206

PM

PRIVACY ACT STATEMENT
The information requested on this form is required under the provisions of 31 U.S.C. 82b and 82c, for the purpose of disbursing Federal money. The information requested is to identify the particular creditor and the amounts to be paid. Failure to furnish this information will hinder discharge of the payment obligation.

Standard Form 1034
Revised January 1980
Department of the Treasury
I TFRM 4-2000
1034-120

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

VOUCHER NO. 5C

U.S. DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION
D.C.A.A.
WALTHAM BRANCH
424 TRAPELLO RD
WALTHAM, MA 02154-6397

DATE VOUCHER PREPARED: 14 September 1994

CONTRACT NUMBER AND DATE: DABT63-94-C-0017

REQUISITION NUMBER AND DATE:

SCHEDULE NO. 950352

PAID BY

PAYEE'S NAME AND ADDRESS

BBN SYSTEMS AND TECHNOLOGIES
A Division of Bolt Beranek & Newman, Inc.
P.O. BOX 4340
BOSTON, MA 02211

Point of contact: Deb Veino @ (617) 873-2426

DATE INVOICE RECEIVED

DISCOUNT TERMS: 11592 1.1/10186

PAYEE'S ACCOUNT NUMBER

SHIPPED FROM | TO | WEIGHT

GOVERNMENT B/L NUMBER

NUMBER AND DATE OF ORDER	DATE OF DELIVERY OR SERVICE	ARTICLES OR SERVICES (Enter description, item number of contract or Federal supply schedule, and other information deemed necessary)	QUANTITY	UNIT PRICE COST	UNIT PRICE PER	AMOUNT (1)
	01 Aug thru 31 Aug 1994	For detail, see SF 1035 continuation sheet. Total amount claimed transferred from Page 2, SF 1035 COST REIMBURSABLE PROVISIONAL PAYMENT				$13,818.92

(Use continuation sheet(s) if necessary) **(Payee must NOT use the space below)** TOTAL $13,818.92

PAYMENT:
- ☐ PROVISIONAL
- ☐ COMPLETE
- ☐ PARTIAL
- ☐ FINAL
- ☐ PROGRESS
- ☐ ADVANCE

APPROVED FOR: Provisional Payment Subject to Later Audit $

EXCHANGE RATE = $1.00

BY [2]: A. Reynolds

TITLE: Auditor, Defense Contract Audit Agency

DIFFERENCES

Amount verified; correct for

(Signature or initials)

Pursuant to authority vested in me, I certify that this voucher is correct and proper for payment.

(Date) (Authorized Certifying Officer)[2] (Title)

ACCOUNTING CLASSIFICATION

PAID BY

CHECK NUMBER | ON ACCOUNT OF U.S. TREASURY | CHECK NUMBER | ON (Name of bank)

CASH $ | DATE | PAYEE [3]

[1] When stated in foreign currency, insert name of currency
[2] If the ability to certify and authority to approve are combined in one person, one signature only is necessary; otherwise the approving officer will sign in the space provided, over his official title.
[3] When a voucher is receipted in the name of a company or corporation, the name of the person writing the company or corporate name, as well as the capacity in which he signs, must appear. For example: "John Doe Company, per John Smith, Secretary", or "Treasurer", as the case may be.

PER

TITLE

Previous edition usable

*U.S.GPO:1987-0-181-247/40205

NSN 7540-00-634-4206

PM

PRIVACY ACT STATEMENT
The information requested on this form is required under the provisions of 31 U.S.C. 82b and 82c, for the purpose of disbursing Federal money. The information requested is to identify the particular creditor and the amounts to be paid. Failure to furnish this information will hinder discharge of the payment obligation.

FORM 1035

CONTRACT NO. # DBAT63-94-C-0017

BBN REF. # 11592 1.1
BBN INVOICE # 950352
SHEET NO. # 2 OF 3
VOUCHER #5C

BBN Systems and Technologies
A Division of Bolt Beranek and Newman, Inc.
P.O. Box 4340
Boston, MA 02211

Target/Estimated Cost	$448,013.00
Target/Fixed Fee	35,671.00
Total	$483,684.00
85% Fixed Fee	$30,320.35

Disbursing Office: Defense Finance & Accounting SVC
Defense Accounting Office
Drawer P
Fort Huachuca, AZ 85613-6000

Withholding Clause:
BBN Withholding:

Analysis of Current and Cumulative Costs and Fee Earned:

Major Cost Elements:	Amount for Current Period Billed	Cumulative Amounts From Inception to Date of This Billing
Direct Labor	$4,742.16	$29,423.87
Overhead	5,467.72	34,926.34
Travel	735.00	1,120.00
Procurement Charge	1.50	1.50
Books & Subscriptions	30.00	30.00
Postage & Express Mail	0.00	9.00
Training Conference	0.00	150.00
General Administration	2,780.37	16,146.40
Total Cost	$13,756.75	$81,807.11
CAS414	62.17	382.92
TOTAL	$13,818.92	$82,190.03

Continuation Sheet - Page # 3
BBN Reference # 11592 1.1
Bureau Voucher # 5C
Invoice # 950352

Direct Labor:

FY	Pool	Hours	Direct Labor	Overhead	Overhead Rate	G&A	G&A Rate
95	10	111.0	$4,742.16	$5,467.72	115.3%	$2,593.30	25.4%
		111.0	$4,742.16	$5,467.72			

Other Direct Costs:

Value Added Costs:

FY	Pool	Direct Costs			
95	0	$736.50		$187.07	25.4%
		$736.50	Total G&A	$2,780.37	

Non Value Added Costs:

FY	Direct Costs
95	$30.00
	$30.00

Standard Form 1034
Revised January 1980
Department of the Treasury
1 TFRM 4-2000
1034-120

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

VOUCHER NO. 5F

U.S. DEPARTMENT, BUREAU, OR ESTABLISHMENT AND LOCATION
Defense Finance & Accounting SVC
Defense Accounting Office
Drawer P
Fort Huachuca, AZ 85613-6000

DATE VOUCHER PREPARED: 14 September 1994

CONTRACT NUMBER AND DATE: DABT63-94-C-0017

REQUISITION NUMBER AND DATE:

SCHEDULE NO. 950352

PAID BY

PAYEE'S NAME AND ADDRESS

BBN SYSTEMS AND TECHNOLOGIES
A Division of Bolt Beranek & Newman, Inc.
P.O. BOX 4340
BOSTON, MA 02211

Point of contact: Deb Veino @ (617) 873-2426

DATE INVOICE RECEIVED

DISCOUNT TERMS: 11592 1.1/10186

PAYEE'S ACCOUNT NUMBER

SHIPPED FROM | TO | WEIGHT | GOVERNMENT B/L NUMBER

NUMBER AND DATE OF ORDER	DATE OF DELIVERY OR SERVICE	ARTICLES OR SERVICES (Enter description, item number of contract or Federal supply schedule, and other information deemed necessary)	QUANTITY	UNIT PRICE COST	UNIT PRICE PER	AMOUNT (1)
	01 Aug thru 31 Aug 1994	Total Fee for 01 August thru 31 August, 1994 Based on 18% completion X $35,671.00 Less Total Fee invoiced to date				$6,420.78 5,350.65
		Total Amount Due This Invoice COST REIMBURSABLE PROVISIONAL PAYMENT				**$1,070.13**

(Use continuation sheet(s) if necessary) **(Payee must NOT use the space below)** **TOTAL**

PAYMENT:
- ☐ PROVISIONAL
- ☐ COMPLETE
- ☐ PARTIAL
- ☐ FINAL
- ☐ PROGRESS
- ☐ ADVANCE

APPROVED FOR: Provisional Payment Subject to Later Audit

EXCHANGE RATE = $1.00

DIFFERENCES

BY [2]

Amount verified; correct for

TITLE

(Signature or initials)

Pursuant to authority vested in me, I certify that this voucher is correct and proper for payment.

(Date) | (Authorized Certifying Officer)[2] | (Title)

ACCOUNTING CLASSIFICATION

APPROVED FOR PAYMENT: $ 1070.13

I certify acceptance of the Supplies or Services hereon on _____

PAYEE

Contracting Officer — Date 20 Sep 94

PAID BY

CHECK NUMBER — ON ACCOUNT OF — ON (Name of bank)

CASH — DATE

$

[1] When stated in foreign currency, insert name of currency.
[2] If the ability to certify and authority to approve are combined in one person, one signature only is necessary; otherwise the approving officer will sign in the space provided, over his official title.
[3] When a voucher is receipted in the name of a company or corporation, the name of the person writing the company or corporate name, as well as the capacity in which he signs, must appear. For example: "John Doe Company, per John Smith, Secretary", or "Treasurer", as the case may be.

PER

TITLE

Previous edition usable

★U.S.GPO:1987-0-181-247/40205

NSN 7540-00-634-4206

PM

PRIVACY ACT STATEMENT
The information requested on this form is required under the provisions of 31 U.S.C. 82b and 82c, for the purpose of disbursing Federal money. The information requested is to identify the particular creditor and the amounts to be paid. Failure to furnish this information will hinder discharge of the payment obligation.

FORM 1035

CONTRACT NO. # DBAT63-94-C-0017

BBN REF. # 11592 1.1
BBN INVOICE # 950352
SHEET NO. # 2 OF 2
VOUCHER #5F

BBN Systems and Technologies
A Division of Bolt Beranek and Newman, Inc.
P.O. Box 4340
Boston, MA 02211

Target/Estimated Cost	$448,013.00
Target/Fixed Fee	35,671.00
Total	$483,684.00
85% Fixed Fee	$30,320.35

Disbursing Office: Defense Finance & Accounting SVC
Defense Accounting Office
Drawer P
Fort Huachuca, AZ 85613-6000

Fixed Fee:

Fixed Fee Due (18% X $35,671.00)	$6,420.78
Less Fixed Fee Billed	5,350.65
Fixed Fee To Be Billed	$1,070.13

SF 1034-EDF PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

DEFENSE FINANCE AND ACCOUNTING
DRAWER P
FT HUACHUCA, AZ 85613-6000

VOUCHER NO.

DATE PREPARED 10/26/95

CONTRACT NO./DATE DABT63-94-C-0017 04/05/94

P A I D B Y
Account of:
DSSN 6424

TAX ID
PAYEE'S NAME BBN SYSTEMS & TECHNOLOGIES
DIV OF BOLT BERANEK & NEWMAN
ADDRESS P.O BX 4340
BOSTON MA 02211

FT HUACHUCA, AZ 85613-6000

DATE INVOICE RECV'D 09/26/95
DISCOUNT TERMS NET 30 DAYS

FOB:
DEST

NO./DATE OF ORDER	DATE OF PERFORMANCE INV DATE	INVRCV'D	MDSE DEL	MDSE ACPT	FREIGHT	MERCHANDISE
16C	09/15/95	09/26/95	09/20/95	09/20/95	0.00	1791.37

TOTAL: MDSE: 1791.37

AMOUNT VERIFIED CORRECT FOR $$ 1791.37
SIGNATURE OR INITIALS: 94/

PAYMENT: 21PARTIAL 10/26/95

PURSUANT TO THE AUTHORITY VESTED IN ME, I CERTIFY THAT THIS VOUCHER IS CORRECT AND PROPER FOR PAYMENT.

AUTHORIZED CERTIFYING OFFICER DATE: 10/26/95
FOR: For M. E. BELZA
MAJ, FC
DEFENSE ACCOUNTING OFFICER

ACCOUNTING CLASSIFICATIONS
97404001301000500SP4T10A64104 2594 S02086 US JWC900 00JWC9 HJ150040060552 1791.37

PAYEE: BBN SYSTEMS & TECHNOLOGIES
DIV BOLT BERANEK & NEWMAN INC
P.O. BOX 4340
BOSTON MA 02211

CHECK AMT $$ 1791.37

CHECK NO.: ON US TREASURY DATE:

ATTS DFRMS

PUBLIC VOUCHER FOR PURCHASES AND SERVICES OTHER THAN PERSONAL

US DEPARTMENT, BUREAU, OR
ESTABLISHMENT AND LOCATION
DEFENSE ACCOUNTING OFFICE
DFAS-IN/EM-TP
FORT HUACHUCA, AZ

DTE VOU PREP: 95/10/27
SCHEDULE NO:
VOUCHER NUM: 202367
CONTRACT NO AND DATE: DABT63-94C0017
PAID BY: M.E. BELZA, MAJ,FC
FORT HUACHUCA
REQUISITION NO & DATE: 95/10/27
-24

PAYEE'S NAME AND ADDRESS: BBN SYSTEMS & TECHNOLOGIES
DIV BOLT BERANEK & NEWMAN I
P.O. BOX 4340
BOSTON MA 02211

DISCOUNT TERMS

INVOICE NO	INT/(DISC) AMT	LATE/TERMS	RATE
16C	0.00	0	0.0000%

NUM & DT ORD	ARTICLES OR SERVICES	QTY ISS	UNIT PRICE	AMOUNT
000001		1.00	1791.3700	1791.37

95300083322CAPS

TOTAL 1791.37

PAYMENT
_ PROVISIONAL
_ COMPLETE
X PARTIAL
_ FINAL
_ PROGRESS
_ ADVANCE

APPROVED BY

BY

TITLE

EXCHANGE RATE DIFF
=$1.00

AMT VER CORRECT 1791.37

SIGNATURE OR INITIALS: VE: 94 PMT NO: 021

AUT-CER: PALMER

PFA: 94

I CERTIFY THIS VOUCHER CORRECT AND PROPER FOR CHECK PAYMENT
95/10/27 M.E. BELZA
DEFENSE ACCOUNTING OFFICER

DATE AUTHORIZED CERTIFYING OFFICER TITLE

CHECK NUMBER 02564453

SF 1034

SF 1034 (CONTINUED) VOUCHER NUMBER: 20236 PAGE: 2

ACCOUNTING CLASSIFICATION

9740400.1301 00-5005 P4T10A8 2594 002086 US JWC900 00J[illegible]9 HJ1500400660552
ACCOUNTING AMOUNT: 1791.3[illegible]